Preliminary

OKI Semiconductor

This version: Nov. 1997
Previous version: Jul. 1996

MSM9200-xx

5 × 7 Dot Character × 16-Digit Display Controller/Driver with Character RAM

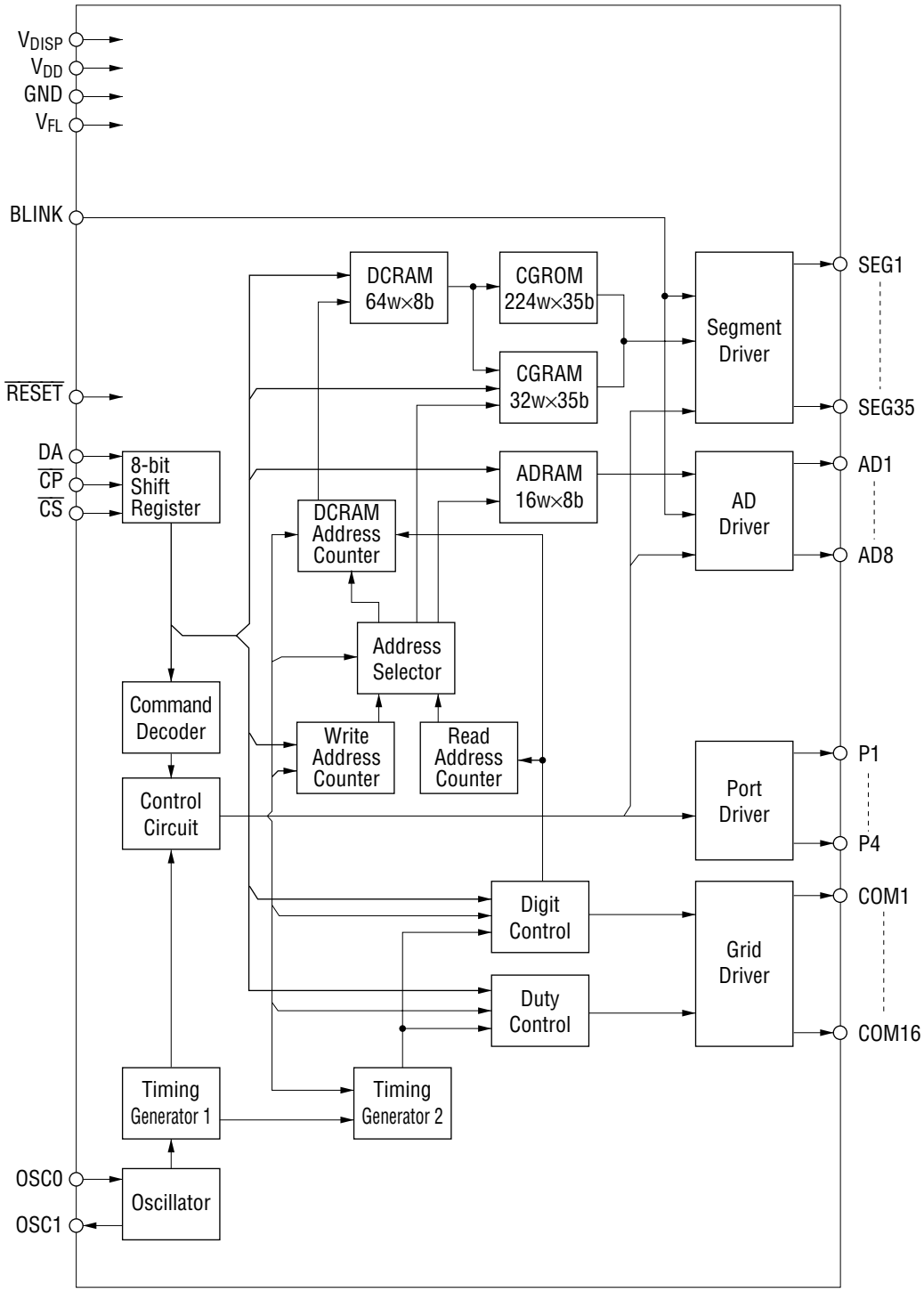
GENERAL DESCRIPTION

The MSM9200-xx is a dot matrix vacuum fluorescent display tube controller driver IC which displays characters, numerics and symbols.
Dot matrix vacuum fluorescent display tube drive signals are generated by serial data sent from a microcontroller. A display system is easily realized by internal ROM and RAM for character display.
The MSM9200-xx has low power consumption because it is munufactured in CMOS process technology.
-01 and -02 are available as general codes.
Custom codes are provided if necessary.

FEATURES

- Logic power supply (V_{DD}) : 3.3 V±10%/5.0 V±10%
- Fluorescent display tube drive power supply (V_{DISP}) : 3.3 V±10%/5.0 V±10%
- Fluorescent display tube drive power supply (V_{FL}) : –20 to –60 V
- VFD driver output current
  (VFD driver output can directly be connected to the fluorescent display tube. No pull-down resistor is required.)
  - Segment driver (SEG1 to SEG35) : –5 mA (V_{FL}=–60V)
  - Segment driver (AD1 to AD8) : –10 mA (V_{FL}=–60V)
  - Grid driver (COM1 to COM16) : –30 mA (V_{FL}=–60V)
- General output port output current
  - Output driver (P1-4) : ±1 mA (V_{DD}=3.3V±10%)
    ±2 mA (V_{DD}=5.0V±10%)
- Content of display
  - CGROM 5×7 dots, 224 types (character data)
  - CGRAM 5×7 dots, 32 types (character data)
  - ADRAM 16 (display digit) ×8 bits (symbol data)
  - DCRAM 64 (stored digit) ×8 bits (register for character data display)
  - General output port 4 bits (static mode)
- Display control function
  - Display digit : 1 to 16 digits
  - Display duty (contrast adjustment) : 16 stages
  - Display blink position specification : Blinking time is input externally
  - Display shift (left and right) : Can be set only for SEG output
  - All lights ON/OFF
- 4 interfaces with microcontroller : DA, $\overline{CS}$, $\overline{CP}$, and BLINK (5 interfaces when $\overline{RESET}$ is added)
- 1 byte instruction execution (excluding data write to RAM and display blink position specification)
- Oscillation circuit included (external C and R)
- Package:
  80-pin plastic QFP (QFP80-P-1414-0.65-K) (Product name: MSM9200-xxGS-K)
  xx indicated the code number.

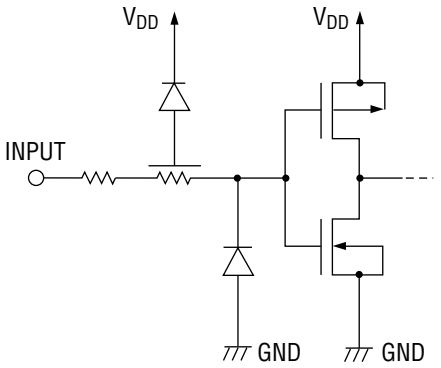
BLOCK DIAGRAM



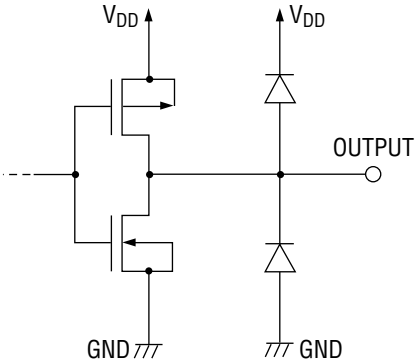
INPUT AND OUTPUT CONFIGURATION

Schematic Diagrams of Logic Portion Input and Output Circuits

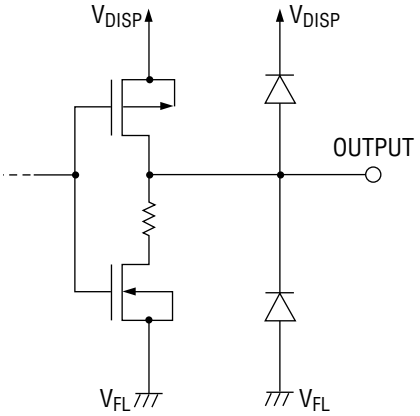
Input Pin



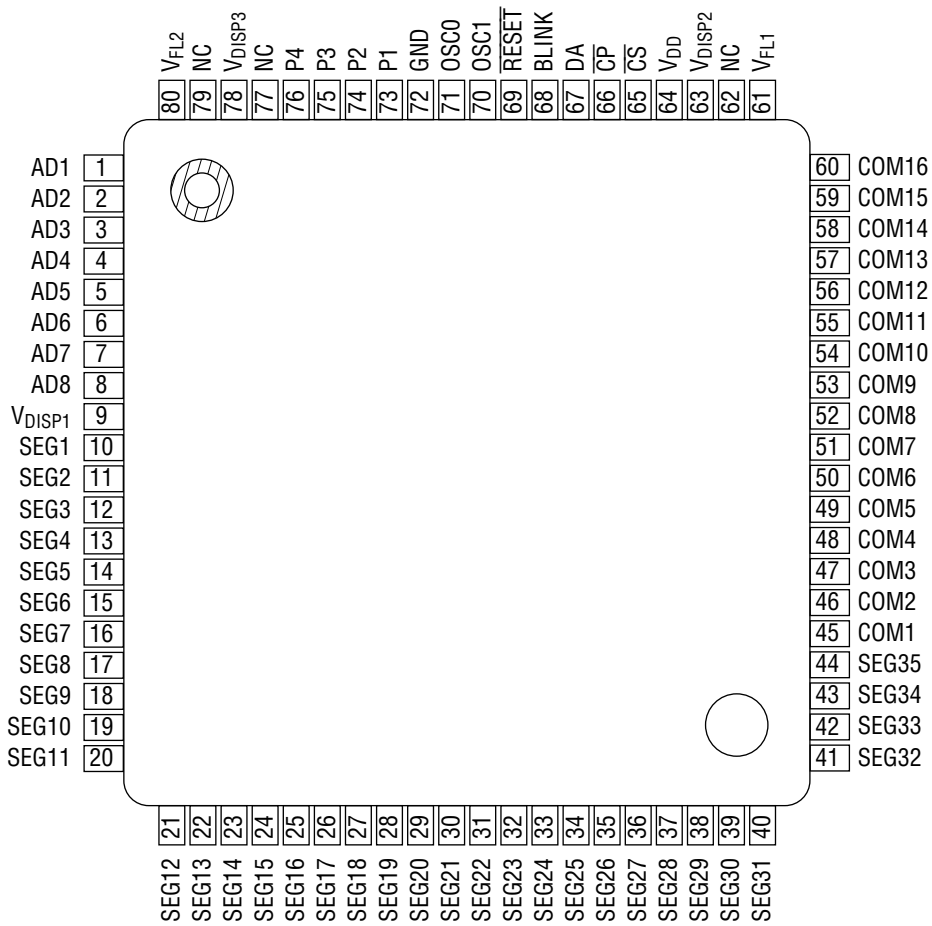
Output Pin



Schematic Diagram of Driver Output Circuit



PIN CONFIGURATION (TOP VIEW)

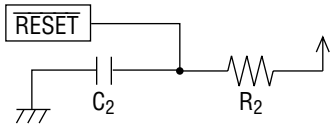
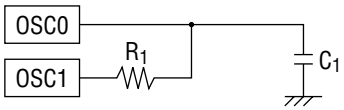


NC: No connection

80-Pin Plastic QFP

PIN DESCRIPTION

Pin	Symbol	Type	Connects to:	Description
10 to 44	SEG1-35	O	Fluorescent tube grid electrode	Fluorescent display tube anode electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH}>–5 mA
45 to 60	COM1-16	O	Fluorescent tube grid electrode	Fluorescent display tube grid electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH}>–30 mA
1 to 8	AD1-8	O	Fluorescent tube grid electrode	Fluorescent display tube grid electrode drive output. Directly connected to fluorescent display tube and a pull-down resistor is not necessary. I_{OH}>–10 mA
73 to 76	P1-4	O	LED drive control terminals	General port output. Output of these pins in static mode, so control for LED driving is performed through these pins.
64	V_{DD}	—	Power supply	V_{DD}-GND are power supplies for internal logic. V_{DISP}-V_{FL} are power supplies for driving fluorescent tubes. Use the same power supply for V_{DD} and V_{DISP}. Apply V_{FL} after V_{DD} and V_{DISP} are applied.
9, 63, 78	$V_{DISP1-3}$	—		
72	GND	—		
61, 80	V_{FL1-2}	—		
67	DA	I	Micro-controller	Serial data input (positive logic). Input from LSB.
66	$\overline{CP}$	I	Micro-controller	Shift clock input. Serial data is shifted on the rising edge of $\overline{CP}$.
65	$\overline{CS}$	I	Micro-controller	Chip select input. "H" disables serial data transfer.
68	BLINK	I	Micro-controller	Display blink frequency input (square wave). Only the position specified by the display blink position set command is validated. The time of "High" (light ON) and "Low" (light OFF) level of the signal frequency to be input to BLINK is the blink time. Fix BLINK pin to the V_{DD} or GND pin when the display blink control is not used.

Pin	Symbol	Type	Connects to:	Description
69	$\overline{\text{RESET}}$	I	Micro-controller or C_2, R_2	Reset input (pull-up resistor included). "Low" initializes all the functions. Initial status is as follows. • Address of each RAM ..... address "00"H • Data of each RAM ..... Content is undefined • Display digit ..... 16 digits • Contrast adjusment ..... 0/16 • Display blink ..... Blinking is disabled for all outputs • All lights ON or OFF ..... OFF mode • All outputs ..... "Low" level  (Circuit when R and C are connected externally) See Application Circuit.
71	OSC0	I	C_1, R_1	External RC pin for RC oscillation. Connect R and C externally. The RC time constant depends on the V_{DD} voltage used. Set the target oscillation frequency to 2 MHz.  (RC oscillation circuit) See Application Circuit.
70	OSC1	O		

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage 1	V_{DD}	(*1)	–0.3 to 6.5	V
	V_{DISP}	(*1)	–0.3 to 6.5	V
Supply Voltage 2	V_{FL}	—	–80 to V_{DISP}+0.3	V
Input Voltage	V_{IN}	—	–80 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta≤25°C	565	mW
Storage Temperature	T_{STG}	—	–55 to 150	°C
Output Current	I_{O1}	COM1-COM16	–40 to 0.0	mA
	I_{O2}	AD1-AD8	–20 to 0.0	
	I_{O3}	SEG1-SEG35	–10 to 0.0	
	I_{O4}	P1-P4	–4.0 to 4.0	

*1 Use the same power supply for V_{DD} and V_{DISP}.

RECOMMENDED OPERATING CONDITIONS-1

When the power supply voltage is 5V (typ).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage 1	V_{DD} V_{DISP}	—	4.5	5.0	5.5	V
Supply Voltage 2	V_{FL}	—	–60	—	–20	V
High Level Input Voltage	V_{IH}	All input pins excluding OSC0 pin	0.7V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All input pins excluding OSC0 pin	—	—	0.3V_{DD}	V
$\overline{CP}$ Frequency	f_C	—	—	—	1.0	MHz
Oscillation Frequency	f_{OSC}	R_1=3.3kΩ, C_1=47pF	1.5	2.0	2.5	MHz
Frame Frequency	f_{FR}	DIGIT=1–16, R_1=3.3kΩ, C_1=47pF	183	244	305	Hz
$\overline{RESET}$ Input Time	t_{RSON}	R_2=1.0kΩ, C_2=0.1PF	0	—	200	µs
Operating Temperature	T_{OP}	—	–40	—	85	°C

RECOMMENDED OPERATING CONDITIONS-2

When the power supply voltage is 3.3V (typ).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage 1	V_{DD} V_{DISP}	—	3.0	3.3	3.6	V
Supply Voltage 2	V_{FL}	—	–60	—	–20	V
High Level Input Voltage	V_{IH}	All input pins excluding OSC0 pin	$0.8V_{DD}$	—	—	V
Low Level Input Voltage	V_{IL}	All input pins excluding OSC0 pin	—	—	$0.2V_{DD}$	V
$\overline{CP}$ Frequency	f_C	—	—	—	1.0	MHz
Oscillation Frequency	f_{OSC}	R_1=3.3kΩ, C_1=39pF	1.5	2.0	2.5	MHz
Frame Frequency	f_{FR}	DIGIT=1–16, R_1=3.3kΩ, C_1=39pF	183	244	305	Hz
$\overline{RESET}$ Input Time	t_{RSON}	R_2=1.0kΩ, C_2=0.1µF	0	—	200	µs
Operating Temperature	T_{OP}	—	–40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics-1

(V_{DD}=V_{DISP}=5.0V±10%, V_{FL}=–60V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{CP}$, BLINK, DA, $\overline{RESET}$	—		0.7V_{DD}	—	V
Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{CP}$, BLINK, DA, $\overline{RESET}$	—		—	0.3V_{DD}	V
High Level Input Current	I_{IH}	$\overline{CS}$, $\overline{CP}$, BLINK, DA, $\overline{RESET}$	V_{IH}=V_{DD}		–1.0	1.0	µA
Low Level Input Current	I_{IL}	$\overline{CS}$, $\overline{CP}$, BLINK, DA, $\overline{RESET}$	V_{IL}=0.0V		–1.0	1.0	µA
High Level Output Voltage	V_{OH1}	COM1-16	I_{OH1}=–30mA		V_{DISP}–1.5	—	V
	V_{OH2}	AD1-8	I_{OH2}=–10mA		V_{DISP}–1.5	—	V
	V_{OH3}	SEG1-35	I_{OH3}=–5mA		V_{DISP}–1.5	—	V
	V_{OH4}	P1-4	I_{OH4}=–2mA		V_{DD}–1.0	—	V
Low Level Output Voltage	V_{OL1}	COM1-16 AD1-8 SEG1-35	—		—	V_{FL}+1.0	V
	V_{OL2}	P1-4	I_{OL1}=2mA		—	1.0	V
Current Consumption	I_{DD1}	V_{DD}, V_{DISP}	f_{OSC}= 2MHz no load	Duty=15/16 Digit=1–16 All output lights ON	—	4	mA
	I_{DD2}			Duty=8/16 Digit=1–9 All output lights OFF	—	3	mA

DC Characteristics-2

(V_{DD}=V_{DISP}=3.3V±10%, V_{FL}=–60V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{CP}$, BLINK, DA, $\overline{RESET}$	—		0.8V_{DD}	—	V
Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{CP}$, BLINK, DA, $\overline{RESET}$	—		0.0	0.2V_{DD}	V
High Level Input Current	I_{IH}	$\overline{CS}$, $\overline{CP}$, BLINK, DA, $\overline{RESET}$	V_{IH}=V_{DD}		–1.0	1.0	µA
Low Level Input Current	I_{IL}	$\overline{CS}$, $\overline{CP}$, BLINK, DA, $\overline{RESET}$	V_{IL}=0.0V		–1.0	1.0	µA
High Level Output Voltage	V_{OH1}	COM1-16	I_{OH1}=–30mA		V_{DISP}–1.5	—	V
	V_{OH2}	AD1-8	I_{OH2}=–10mA		V_{DISP}–1.5	—	V
	V_{OH3}	SEG1-35	I_{OH3}=–5mA		V_{DISP}–1.5	—	V
	V_{OH4}	P1-4	I_{OH4}=–1mA		V_{DD}–1.0	—	V
Low Level Output Voltage	V_{OL1}	COM1-16 AD1-8 SEG1-35	—		—	V_{FL}+1.0	V
	V_{OL2}	P1-4	I_{OL1}=1mA		—	1.0	V
Current Consumption	I_{DD1}	V_{DD}, V_{DISP}	f_{OSC}= 2MHz no load	Duty=15/16 Digit=1–16 All output lights ON	—	3	mA
	I_{DD2}			Duty=8/16 Digit=1–9 All output lights OFF	—	2	mA

AC Characteristics-1

(V_{DD}, V_{DISP}=5.0V±10%, V_{FL}=–60V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequncy	f_C	—		—	1.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		300	—	ns
DA Setup Time	t_{DS}	—		300	—	ns
DA Hold Time	t_{DH}	—		300	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		300	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	R_1=3.3kΩ, C_1=47PF		16	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		300	—	ns
Data Processing Time	t_{DOFF}	R_1=3.3kΩ, C_1=47PF		8	—	µs
$\overline{RESET}$ Pulse Width	t_{RSON}	When $\overline{RESET}$ signal is input externally		300	—	ns
Waite DA Time	t_{RSOFF}	—		300	—	µs
All Output Slow Rate	t_R	C_l=100pF	t_R=20% to 80%	—	4.0	µs
	t_F		t_F=80% to 20%	—	4.0	µs
V_{DD} Rise Time	t_{PRZ}	When mounted in the unit		—	100	µs
V_{DD} Off Time	t_{POF}	When mounted in the unit, V_{DD}=0.0V		5.0	—	ms

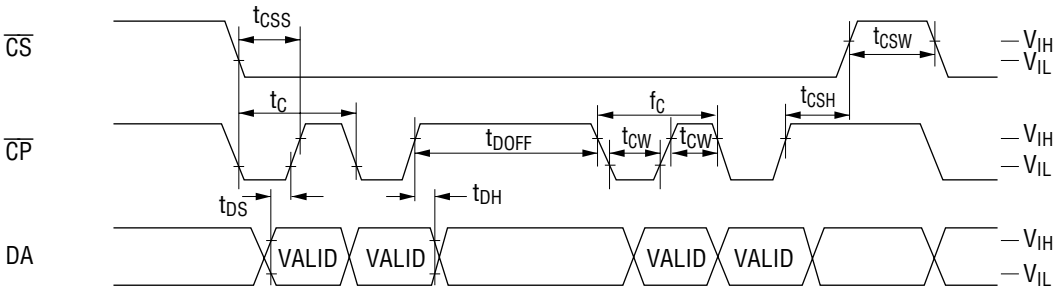
AC Characteristics-2

(V_{DD}, V_{DISP}=3.3V±10%, V_{FL}=–60V, Ta=–40 to +85°C, unless otherwise specified)

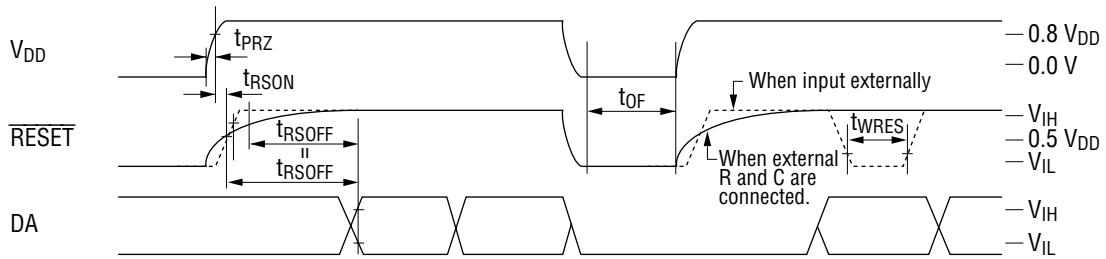
Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequncy	f_C	—		—	1.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		300	—	ns
DA Setup Time	t_{DS}	—		300	—	ns
DA Hold Time	t_{DH}	—		300	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		300	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	R_1=3.3kΩ, C_1=39PF		16	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		300	—	ns
Data Processing Time	t_{DOFF}	R_1=3.3kΩ, C_1=39PF		8	—	µs
$\overline{RESET}$ Pulse Width	t_{WRES}	When $\overline{RESET}$ signal is input externally		300	—	ns
DA Wait Time	t_{RSOFF}	—		300	—	µs
All Output Slew Rate	t_R	C_l=100pF	t_R=20% to 80%	—	4.0	µs
	t_F		t_F=80% to 20%	—	4.0	µs
V_{DD} Rise Time	t_{PRZ}	When mounted in the unit		—	100	µs
V_{DD} Off Time	t_{POF}	When mounted in the unit, V_{DD}=0.0V		5.0	—	ms

TIMING DIAGRAM

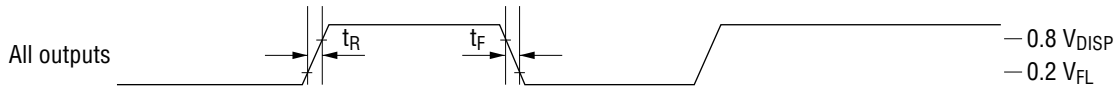
• Data Timing



• Reset Timing



• Output Timing



Symbol	V_{DD}=3.3V±10%	V_{DD}=5.0V±10%
V_{IH}	0.8 V_{DD}	0.7 V_{DD}
V_{IL}	0.2 V_{DD}	0.3 V_{DD}

FUNCTIONAL DESCRIPTION

Command List

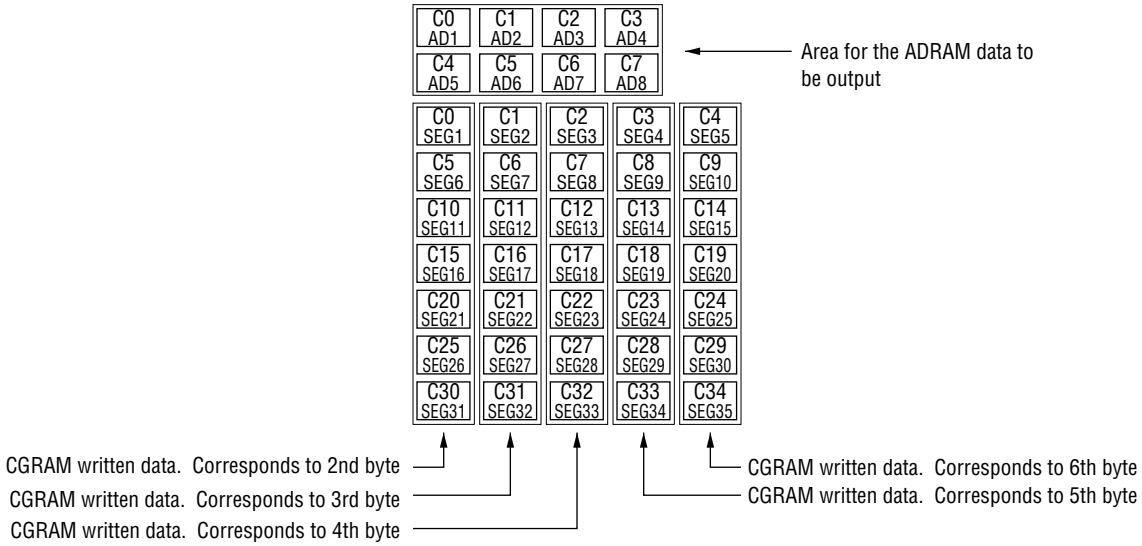
	Command	1st byte LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	2nd byte LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1	DCRAM data write 1	X0	X1	X2	X3	1	0	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
2	DCRAM data write 2	X0	X1	X2	X3	0	1	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
3	DCRAM data write 3	X0	X1	X2	X3	1	1	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
4	DCRAM data write 4	X0	X1	X2	X3	0	0	1	0	C0	C1	C2	C3	C4	C5	C6	C7	
5	CGRAM data write 1	X0	X1	X2	X3	1	0	1	0	C0	C5	C10	C15	C20	C25	C30	*	2nd byte
										C1	C6	C11	C16	C21	C26	C31	*	3rd byte
										C2	C7	C12	C17	C22	C27	C32	*	4th byte
										C3	C8	C13	C18	C23	C28	C33	*	5th byte
										C4	C9	C14	C19	C24	C29	C34	*	6th byte
6	CGRAM data write 2	X0	X1	X2	X3	0	1	1	0	C0	C5	C10	C15	C20	C25	C30	*	2nd byte
										C1	C6	C11	C16	C21	C26	C31	*	3rd byte
										C2	C7	C12	C17	C22	C27	C32	*	4th byte
										C3	C8	C13	C18	C23	C28	C33	*	5th byte
										C4	C9	C14	C19	C24	C29	C34	*	6th byte
7	ADRAM data write	X0	X1	X2	X3	1	1	1	0	C0	C1	C2	C3	C4	C5	C6	C7	
8	Display blink position set	SG	AD	*	*	0	0	0	1	G1	G2	G3	G4	G5	G6	G7	G8	2nd byte
										G9	G10	G11	G12	G13	G14	G15	G16	3rd byte
9	DCRAM address shift	S	*	*	*	1	0	0	1									
A	DCRAM address reset	*	*	*	*	0	1	0	1									
B	General output port set	P1	P2	P3	P4	1	1	0	1									
C	Display duty set	D0	D1	D2	D3	0	0	1	1									
D	Number of digits set	K0	K1	K2	K3	1	0	1	1									
E	All lights ON/OFF	L	H	*	*	0	1	1	1									
	Test mode																	

When data is written to RAM (DCRAM, CGRAM, ADRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Note: The test mode is used for inspection before shipment.
It is not a user function.

* : Don't care
Xn : Address specification for each RAM
Cn : Character code specification for each RAM
SG : SEG display area specification
AD : AD display area specification
Gn : Display blink position specification
S : Left and right display shift specification
Pn : General output port status specification
Dn : Display duty specification
Kn : Number of digits specification
H : All lights ON instruction
L : All lights OFF instruction

Positional Relationship Between SEGn and ADn (one digit)

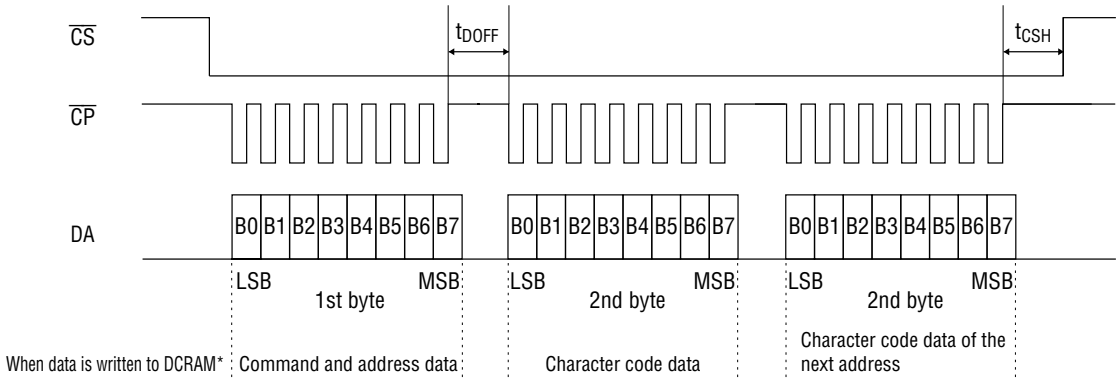


Data Transfer System and Command Write System

Display control command and data are written by an 8-bit serial transfer.
Write timing is shown in the figure below.

Setting the $\overline{CS}$ pin to "Low" level enables a data transfer.
Data is 8 bits and is sequentially input into the DA pin from LSB (LSB first).
As shown in the figure below, data is read by the shift register at the rising edge of the shift clock, which is input into the $\overline{CP}$ pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.
Therefore it is not necessary to input load signals from the outside.

Setting the $\overline{CS}$ pin to "High" disables data transfer. Data input from the point when the $\overline{CS}$ pin changes from "High" to "Low" is recognized in 8-bit units.



* When data is written to RAM (DCRAM, ADRAM, CGRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Reset Function

Reset is executed when the $\overline{RESET}$ pin is set to "L", (when turning power on, for example,) and initializes all functions.
Initial status is as follows.

- Address of each RAM ..... address "00"H
- Data of each RAM ..... All contents are undefined
- Display blink ..... Blinking is disabled for all outputs
- General output port ..... All general output ports go "Low"
- Display digit ..... 16 digits
- Contrast adjustment 0/16
- All display lights ON or OFF ..... OFF mode
- Segment output ..... All segment outputs go "Low"
- AD output ..... All AD outputs go "Low"

Reset again according to "Initial Setting Flowchart" after reset.

Description of Commands and Functions

1. DCRAM data write 1
   (Specifies the address (00H to 0FH) of DCRAM and writes the character code of CGROM and CGRAM.)
2. DCRAM data write 2
   (Specifies the address (10H to 1FH) of DCRAM and writes the character code of CGROM and CGRAM.)
3. DCRAM data write 3
   (Specifies the address (20H to 2FH) of DCRAM and writes the character code of CGROM and CGRAM.)
4. DCRAM data write 4
   (Specifies the address (30H to 3FH) of DCRAM and writes the character code of CGROM and CGRAM.)

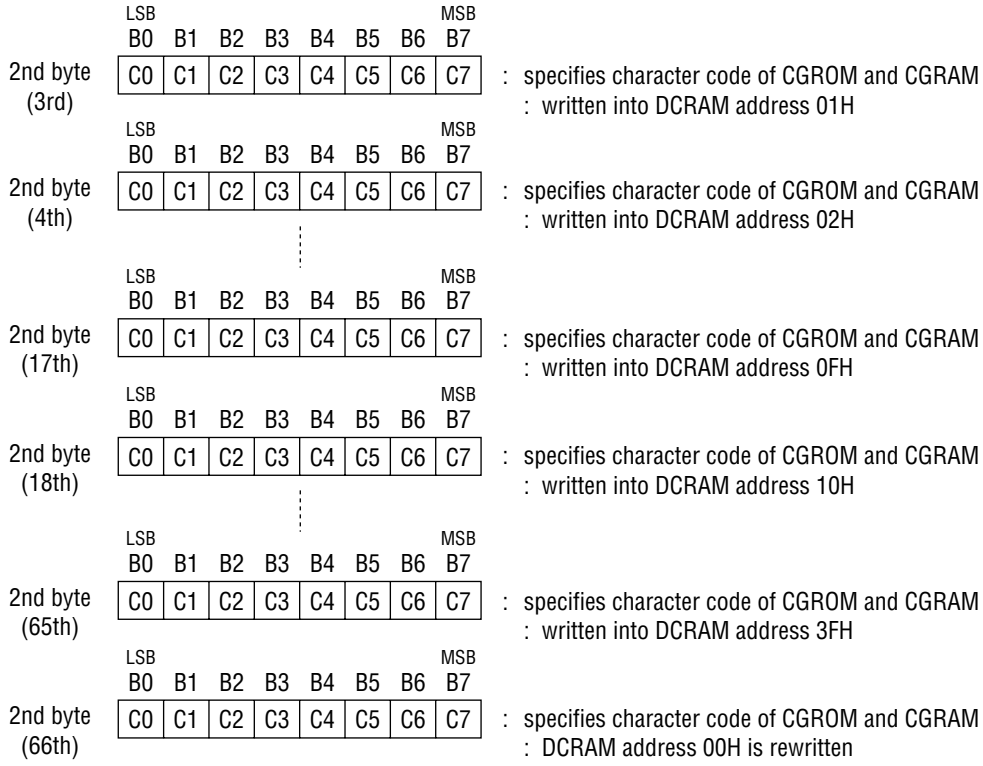
DCRAM (Data Control RAM) has a 6-bit address to store character code of CGROM and CGRAM. (4 bits can be set by the user and the 2 bits on the MSB side are automatically set.)
The character code specified by DCRAM is converted to a 5×7 dot matrix character pattern via CGROM or CGRAM.
The capacity is 64×8 bits, which can store 64 characters.

Note: The addresses 00H to 3FH of DCRAM are automatically incremented.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	X0	X1	X2	X3	1	0	0	0	: selects DCRAM data write mode and specifies DCRAM address (Ex: Specifies DCRAM address 00H)
	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
2nd byte (2nd)	C0	C1	C2	C3	C4	C5	C6	C7	: specifies character code of CGROM and CGRAM : written into DCRAM address 00H

To specify the character code of CGROM and CGRAM continuously to the next address, specify only character code as follows.
The addresses of DCRAM are automatically incremented. Specification of an address is unnecessary.



X0 (LSB) to X3 (MSB): DCRAM addresses (4 bits: 16 characters)
Note: A total of 64 characters for the four specifications
C0 (LSB) to C7 (MSB): Character code of CGROM and CGRAM (8 bits: 256 character)

[COM positions and set DCRAM addresses]

The states when $\overline{\text{RESET}}$ is input and DCRAM address reset commands are executed

Command No.	HEX	K0	K1	K2	K3	COM position	Command No.	HEX	K0	K1	K2	K3	COM position
1	00	0	0	0	0	COM1	3	20	0	0	0	0	
	01	1	0	0	0	COM2		21	1	0	0	0	
	⋮					⋮		⋮					⋮
	0E	1	1	1	1	COM15		2E	1	1	1	1	
	0F	1	1	1	1	COM16		2F	1	1	1	1	
2	10	0	0	0	0		4	30	0	0	0	0	
	11	1	0	0	0			31	1	0	0	0	
	⋮					⋮		⋮					⋮
	1E	0	1	1	1			3E	0	1	1	1	
	1F	1	1	1	1			3F	1	1	1	1	

5. CGRAM data write 1
   (Specifies the addresses 00H to 0FH of CGRAM and writes character pattern data.)
6. CGRAM data write 2
   (Specifies the addresses 10H to 1FH of CGRAM and writes character pattern data.)

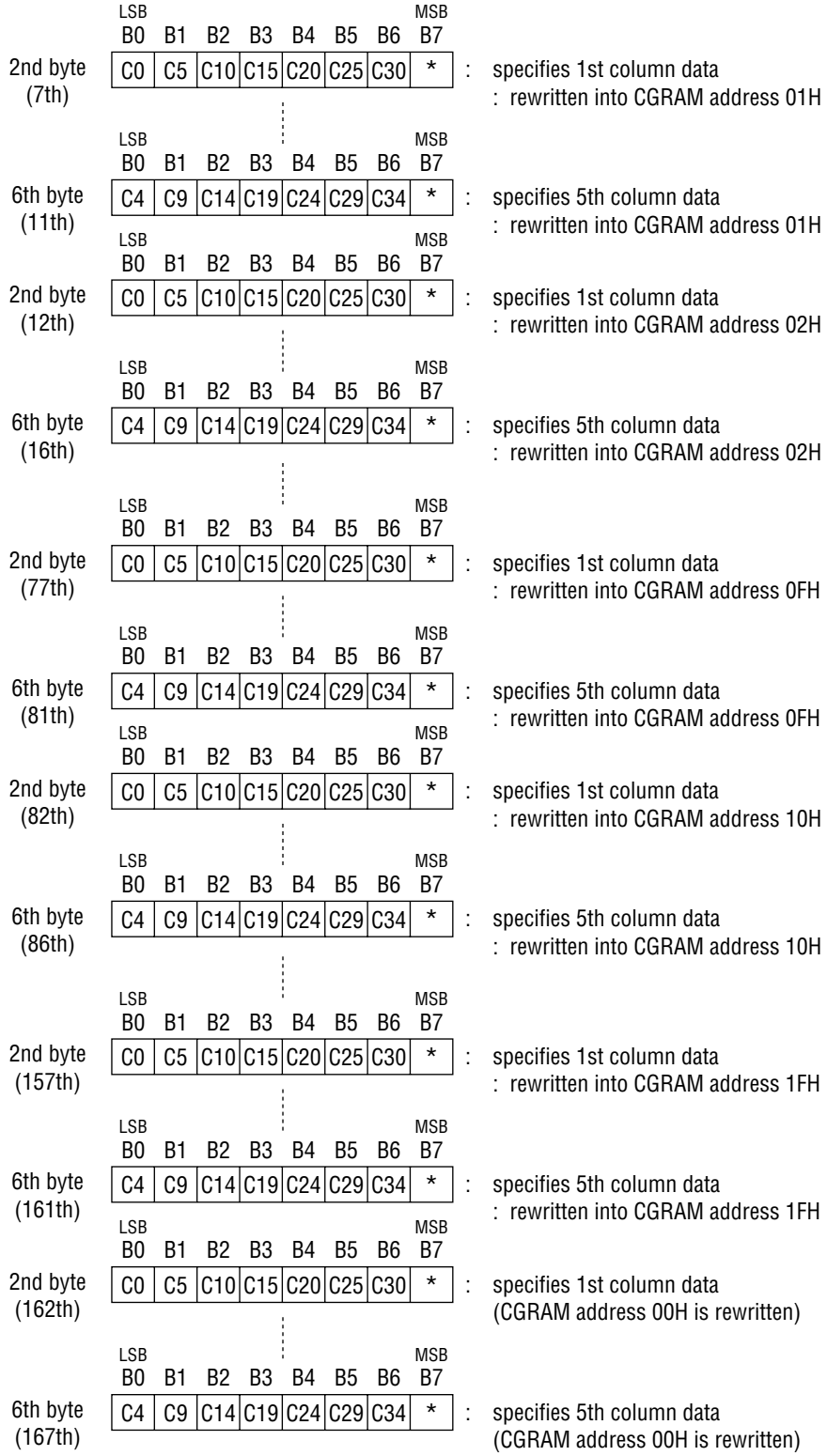
CGRAM (Character Generator RAM) has a 5-bit address to store 5×7 dot matrix character patterns. (4 bits can be set by the user and the 1 bit on the MSB is automatically set.)
A character pattern stored in CGRAM can be displayed by specifying the character code (address) by DCRAM.
The address of CGRAM is assigned to 00H to 1FH. (All the other addresses are the CGROM addresses.)
Capacity is (16×2)×35×8 bits, which can store 32 types of character patterns.

Note: The addresses 00H to 1FH of CGRAM are automatically incremented.

[Command format]

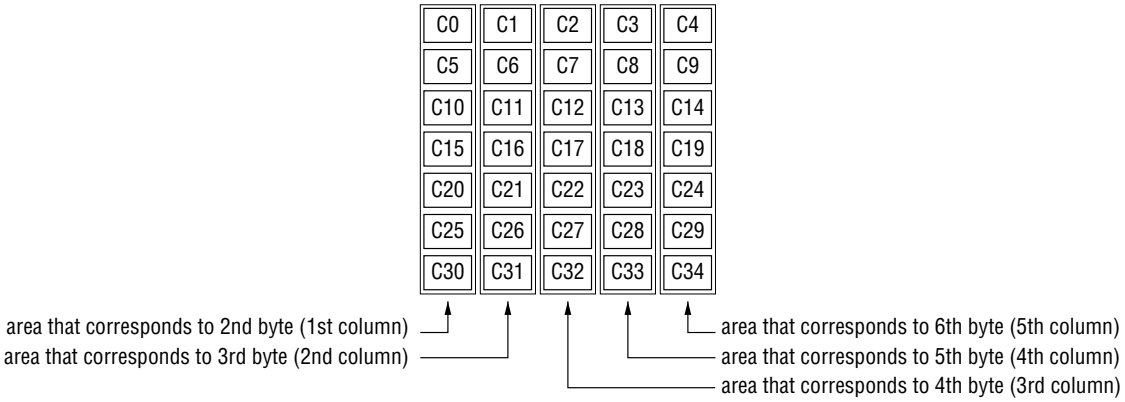
	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	X0	X1	X2	X3	1	0	1	0	: selects CGRAM data write mode and specifies CGRAM address. (Ex: specifies CGRAM address 00H)
2nd byte (2nd)	C0	C5	C10	C15	C20	C25	C30	*	: specifies 1st column data : rewritten into CGRAM address 00H
3rd byte (3rd)	C1	C6	C11	C16	C21	C26	C31	*	: specifies 2nd column data : rewritten into CGRAM address 00H
4th byte (4th)	C2	C7	C12	C17	C22	C27	C32	*	: specifies 3rd column data : rewritten into CGRAM address 00H
5th byte (5th)	C3	C8	C13	C18	C23	C28	C33	*	: specifies 4th column data : rewritten into CGRAM address 00H
6th byte (6th)	C4	C9	C14	C19	C24	C29	C34	*	: specifies 5th column data : rewritten into CGRAM address 00H

To specify character pattern data continuously to the next address, specify only character pattern data as follows.
The addresses of CGRAM are automatically incremented. Specification of an address is therefore unnecessary.
The 2nd to 6th byte (character pattern data) are regarded as one data item, so 300 ns is sufficient for t_{DOFF} time between bytes.



X0 (LSB) to X3 (MSB): CGRAM addresses (4 bits: 16 characters)
Note: A total of 32 characters for the two specifications.
C0 (LSB) to C34 (MSB): Character pattern data (35 bits: 35 outputs per digit)

Positional relationship between the output area of CGROM and that of CGRAM



Note: CGROM (Character Generator ROM) has an 8-bit address to generate 5×7 dot matrix character patterns.
The capacity is 224×35×8 bits, which can store 224 types of character patterns.
2 types of general-purpose code are availble (see ROM CODE list) and custom codes are provided on customer's request.

[CGROM addresses and set CGRAM addresses]

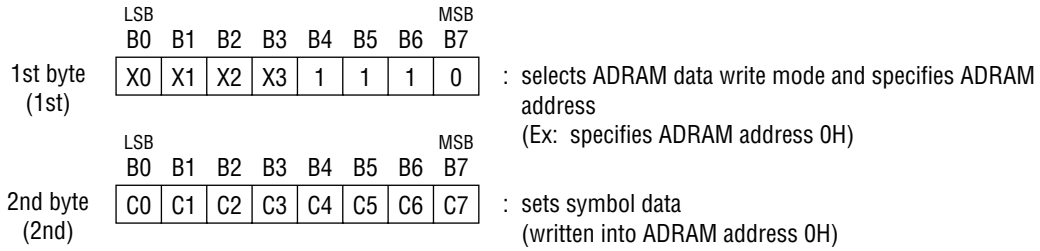
Refer to ROMCODE table

Command No.	HEX	K0	K1	K2	K3	CGROM address	Command No.	HEX	K0	K1	K2	K3	CGROM address
2	00	0	0	0	0	RAM00(00000000B)	4	10	0	0	0	0	RAM10(00010000B)
	01	1	0	0	0	RAM01(00000001B)		11	1	0	0	0	RAM11(00010001B)
	02	0	1	0	0	RAM02(00000010B)		12	0	1	0	0	RAM12(00010010B)
	03	1	1	0	0	RAM03(00000011B)		13	1	1	0	0	RAM13(00010011B)
	04	0	0	1	0	RAM04(00000100B)		14	0	0	1	0	RAM14(00010100B)
	05	1	0	1	0	RAM05(00000101B)		15	1	0	1	0	RAM15(00010101B)
	06	0	1	1	0	RAM06(00000110B)		16	0	1	1	0	RAM16(00010110B)
	07	1	1	1	0	RAM07(00000111B)		17	1	1	1	0	RAM17(00010011B)
	08	0	0	0	1	RAM08(00001000B)		18	0	0	0	1	RAM18(00011000B)
	09	1	0	0	1	RAM09(00001001B)		19	1	0	0	1	RAM19(00011001B)
	0A	0	1	0	1	RAM0A(00001010B)		1A	0	1	0	1	RAM1A(00011010B)
	0B	1	1	0	1	RAM0B(00001011B)		1B	1	1	0	1	RAM1B(00011011B)
	0C	0	0	1	1	RAM0C(00001100B)		1C	0	0	1	1	RAM1C(00011100B)
	0D	1	0	1	1	RAM0D(00001101B)		1D	1	0	1	1	RAM1D(00011101B)
	0E	0	1	1	1	RAM0E(00001110B)		1E	0	1	1	1	RAM1E(00011110B)
	0F	1	1	1	1	RAM0F(00001111B)		1F	1	1	1	1	RAM1F(00011111B)

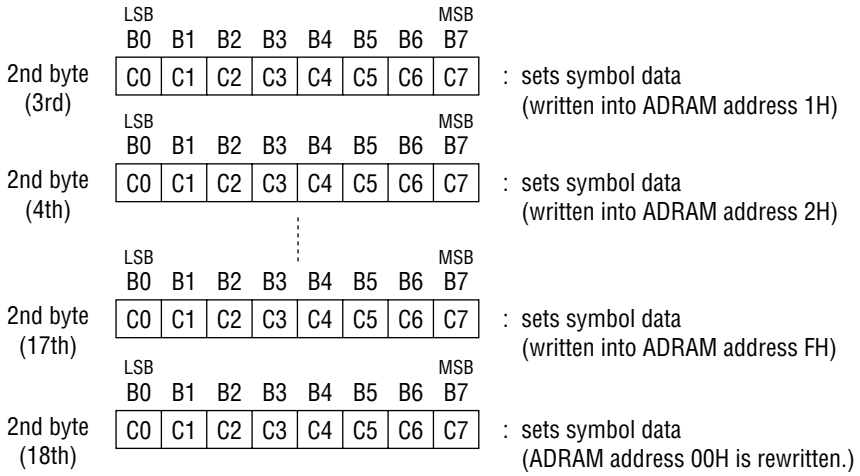
7. ADRAM data write
(specifies address of ADRAM and writes symbol data)

ADRAM (Additional Data RAM) has a 4-bit address to store symbol data.
Symbol data specified by ADRAM is directly output without CGROM and CGRAM.
The capacity is 8×16 bits, which can store 8 types of symbol patterns for each digit.
The terminal to which the contents of ADRAM are output can be used as a cursor.

[Command format]



To specify symbol data continuously to the next address, specify only symbol data as follows. The address of ADRAM is automatically incremented. Specification of addresses is therefore unnecessary.



X0 (LSB) to X3 (MSB): ADRAM addresses (4 bits: 16 characters)
C0 (LSB) to C7 (MSB): Symbol data (8-symbol data per digit)

[COM positions and ADRAM addresses]

HEX	D0	D1	D2	D3	COM position	HEX	D0	D1	D2	D3	COM position
0	0	0	0	0	COM1	8	0	0	0	1	COM9
1	1	0	0	0	COM2	9	1	0	0	1	COM10
2	0	1	0	0	COM3	A	0	1	0	1	COM11
3	1	1	1	0	COM4	B	1	1	0	1	COM12
4	0	0	1	0	COM5	C	0	0	1	1	COM13
5	1	0	1	0	COM6	D	1	0	1	1	COM14
6	0	1	1	0	COM7	E	0	1	1	1	COM15
7	1	1	1	0	COM8	F	1	1	1	1	COM16

8. Display blink position set
(sets the blink position for the SEG area or AD area in COMn.

Display blink position can be set separately for the SEG area and AD area. In this case, select by command in which COMn the SEG area or AD area is made blink.
The blink disabled state is entered for this setting when power is turned on or when a $\overline{\text{RESET}}$ signal is input. The display blink cycle is determined by the frequency to be input to the BLINK pin.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	SG	AD	*	*	0	0	0	1	: selects either the AD output area or the segment output area and specifies digit
2nd byte (2nd)	G1	G2	G3	G4	G5	G6	G7	G8	: specifies blink position to COM1 to COM8
3rd byte (3rd)	G9	G10	G11	G12	G13	G14	G15	G16	: specifies blink position to COM9 to COM16

The 2nd and 3rd bytes (COM1 to COM16 position specification) are regarded as one data item, so 300 ns is sufficient for t_{DOFF} time between bytes.

SG: Specifies SEG area
AD: Specifies AD area
Gn: Specifies blinks

[SEG and AD display and set data]

SG/AD	Gn	SEG and AD display
0	0	Does not blink (current state)
0	1	Does not bilnk (current state)
1	0	Specified positions do not blink
1	1	Specified positions blink

(The state when power is applied or when $\overline{\text{RESET}}$ is input)

Note: If both SG and AD are set to "1" by command, both the SEG area and the AD area are specified.

9. DCRAM address shift
(Shifts SEG output left or right.)

DCRAM address shift shifts SEG output 1 digit to the left or right using 1 bit data. AD output cannot be shifted.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	SG	*	*	*	1	0	0	1	: selects DCRAM address shift and sets shift value (left, right)

S: Specifies the direction of shift

[Set data and shift direction of display]

S	Shift direction of display
0	Shift to left
1	Shift to right

[DCRAM address shift and COM positions]

When S=0 (shift to left) is performed from the initial state.

Command No.	HEX	K0	K1	K2	K3	COM position	Command No.	HEX	K0	K1	K2	K3	COM position
1	00	0	0	0	0	COM2	3	20	0	0	0	0	
	01	1	0	0	0	COM3		21	1	0	0	0	
	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	0E	0	1	1	1	COM16		2E	0	1	1	1	
	0F	1	1	1	1			2F	1	1	1	1	
2	10	0	0	0	0		4	30	0	0	0	0	
	11	1	0	0	0			31	1	0	0	0	
	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	1E	0	1	1	1			3E	0	1	1	1	
	1F	1	1	1	1			3F	1	1	1	1	COM1

When S=1 (shift to right) is performed from the initial state.

Command No.	HEX	K0	K1	K2	K3	COM position	Command No.	HEX	K0	K1	K2	K3	COM position
1	00	0	0	0	0		3	20	0	0	0	0	
	01	1	0	0	0	COM1		21	1	0	0	0	
	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	0E	0	1	1	1	COM14		2E	0	1	1	1	
	0F	1	1	1	1	COM15		2F	1	1	1	1	
2	10	0	0	0	0	COM16	4	30	0	0	0	0	
	11	1	0	0	0			31	1	0	0	0	
	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	1E	0	1	1	1			3E	0	1	1	1	
	1F	1	1	1	1			3F	1	1	1	1	

A. DCRAM address reset
(returns display status to initial setting status)

The DCRAM address reset returns the status where a DCRAM address shift is executed to initial status.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	*	*	*	*	0	1	0	1	: selects DCRAM address reset

Relation between the DCRAM address shifts and the COM outputs

Initial status or the status where display address reset executed (DCRAM address is 00H)

COM output	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DCRAM address (HEX)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

When left shift is executed in the initial status

COM output	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DCRAM address (HEX)	3F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

When right shift is executed in the initial status

COM output	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DCRAM address (HEX)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10

B. General output port set
(specifies the general output port status)

The general output port is an output for 4-bit static operation.
It is used to control other I/O devices and turn on LED.
When at the "High" level, this output becomes the V_{DD} voltage, and when at the "Low" level, it becomes the ground potential. Therefore, the fluorescent display tube cannot be driven.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	P1	P2	P3	P4	1	1	0	1	: selects a general output port and specifies the output status

P1-P4: general output port

[Set data and set state of general output port]

Pn	Display state of general output port
0	Sets to the output to Low
1	Sets to the output to High

(The state when power is applied or when $\overline{\text{RESET}}$ is input.)

C. Display duty set
(writes display duty value to duty cycle register)

Display duty adjusts contrast in 16 stages using 4-bit data.
When power is turned on or when the $\overline{\text{RESET}}$ signal is input, the duty cycle register value is "0". Always execute this instruction before turning the display on, then set a desired duty value.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	D0	D1	D2	D3	0	0	1	1	: selects display duty set mode and sets duty value

D0 (LSB) to D3 (MSB): display duty data (4 bits: 16 stages)

[Relation between setup data and controlled COM duty]

HEX	D3	D2	D1	D0	COM duty	HEX	D3	D2	D1	D0	COM duty
* 0	0	0	0	0	0/16	8	1	0	0	0	8/16
1	0	0	0	1	1/16	9	1	0	0	1	9/16
2	0	0	1	0	2/16	A	1	0	1	0	10/16
3	0	0	1	1	3/16	B	1	0	1	1	11/16
4	0	1	0	0	4/16	C	1	1	0	0	12/16
5	0	1	0	1	5/16	D	1	1	0	1	13/16
6	0	1	1	0	6/16	E	1	1	1	0	14/16
7	0	1	1	1	7/16	F	1	1	1	1	15/16

* The state when powered on or when $\overline{\text{RESET}}$ signal inputs.

D. Number of digits set
(writes the number of display digits to the display digit register)

The number of digits set can display a maximum of 16 digits using 4-bit data.
When power is turned on or when a $\overline{\text{RESET}}$ signal is input, the number of digit register value is "0". Always execute this instruction to change the number of digits before turning the dispaly on.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	K0	K1	K2	K3	1	0	1	1	: selects the number of digit set mode and specifies the number of digit value

K0 (LSB) to K3 (MSB): number of digit data (4 bits: 16 digits)

[Relation between setup data and controlled COM]

HEX	K3	K2	K1	K0	Number of digits of COM	HEX	K3	K2	K1	K0	Number of digits of COM
0	0	0	0	0	COM1-16	8	1	0	0	0	COM1-8
1	0	0	0	1	COM1-1	9	1	0	0	1	COM1-9
2	0	0	1	0	COM1-2	A	1	0	1	0	COM1-10
3	0	0	1	1	COM1-3	B	1	0	1	1	COM1-11
4	0	1	0	0	COM1-4	C	1	1	0	0	COM1-12
5	0	1	0	1	COM1-5	D	1	1	0	1	COM1-13
6	0	1	1	0	COM1-6	E	1	1	1	0	COM1-14
7	0	1	1	1	COM1-7	F	1	1	1	1	COM1-15

E. All display lights ON/OFF set
(turns all dispaly lights ON or OFF)

All display lights ON is used primarily for display testing.
All display lights OFF is primarily used to prevent malfunction when power is turned on.

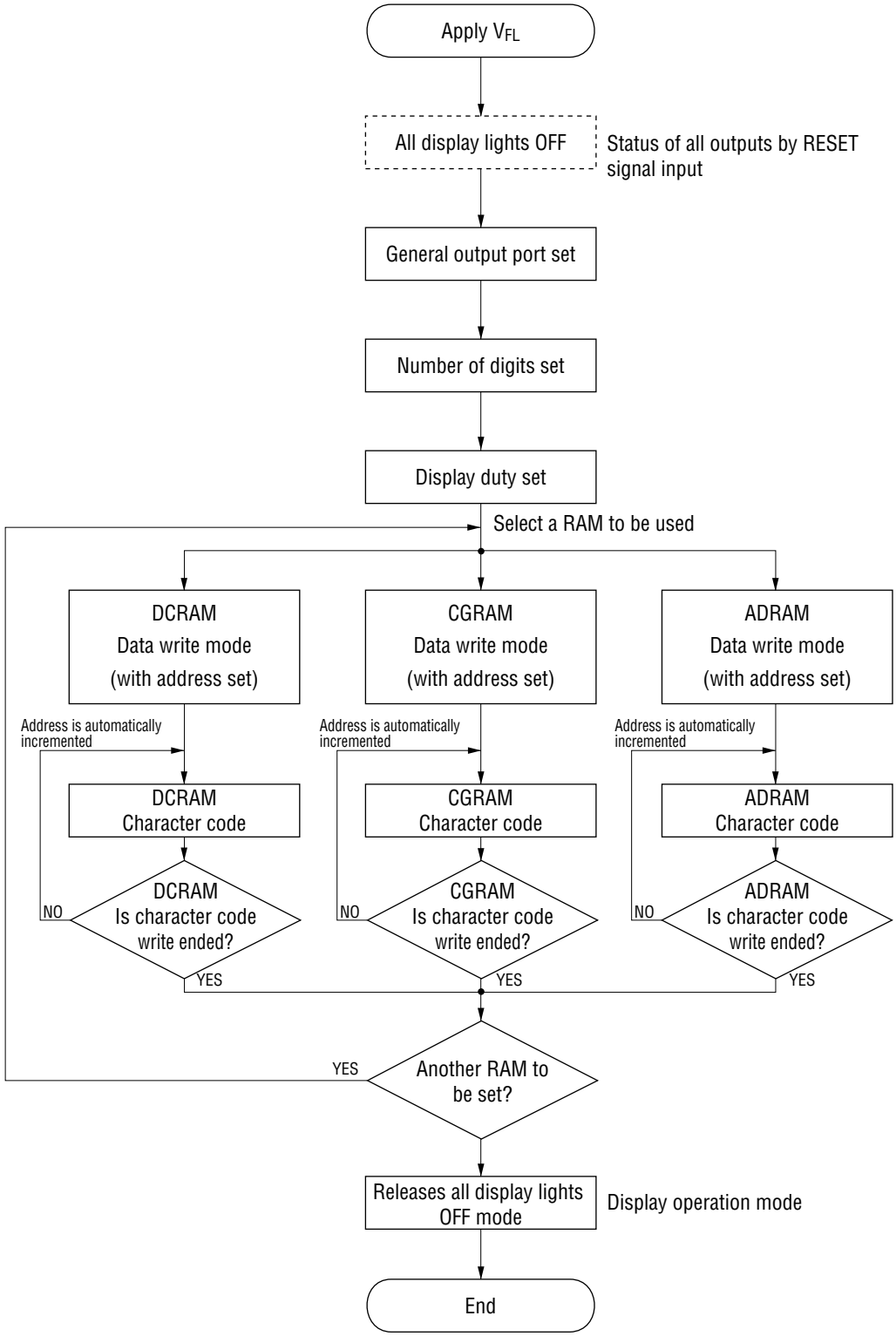
[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	L	H	*	*	0	1	1	1	: selects all display lights ON or OFF mode and sets all lights ON or OFF value

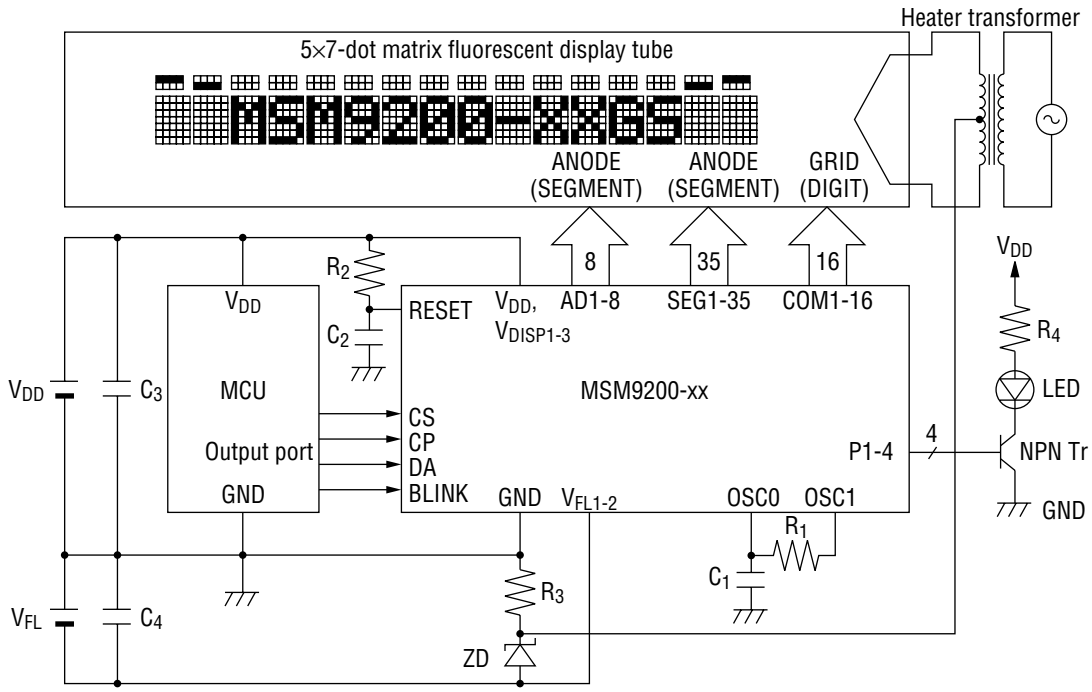
[Set data and display state of SEG and AD]

L	H	Display state of SEG and AD	
0	0	All outputs maintain current states	
1	0	Sets all outputs to Low	(The state when power is applied or when $\overline{\text{RESET}}$ is input.)
0	1	Sets all outputs to High	
1	1	Sets all outputs to High	(All lights ON mode has priority.)

Initial Setting Flowchart



APPLICATION CIRCUIT

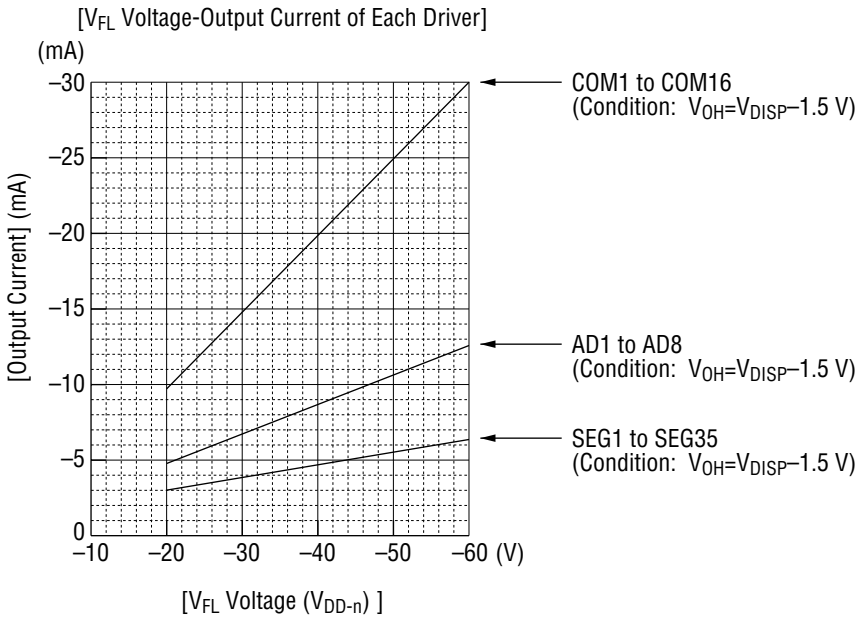


Notes: 1. The V_{DD} value depends on the power supply voltage of the microcontroller used. Adjust the values of the constants R_1, R_2, R_4, C_1, and C_2 to the power supply voltage used.

2. The V_{FL} value depends on the fluorescent display tube used. Adjust the values of the constants R_3 and ZD to the power supply voltage used.

Reference data

The figure below shows the relationship between the V_{FL} voltage and the output current of each driver.
Take care that the total power consumtion to be used does not exceed the power dissipation.



MSM9200-01 ROM Code

00000000B (00H) to 00011111B (1FH) are the CGRAM addresses.

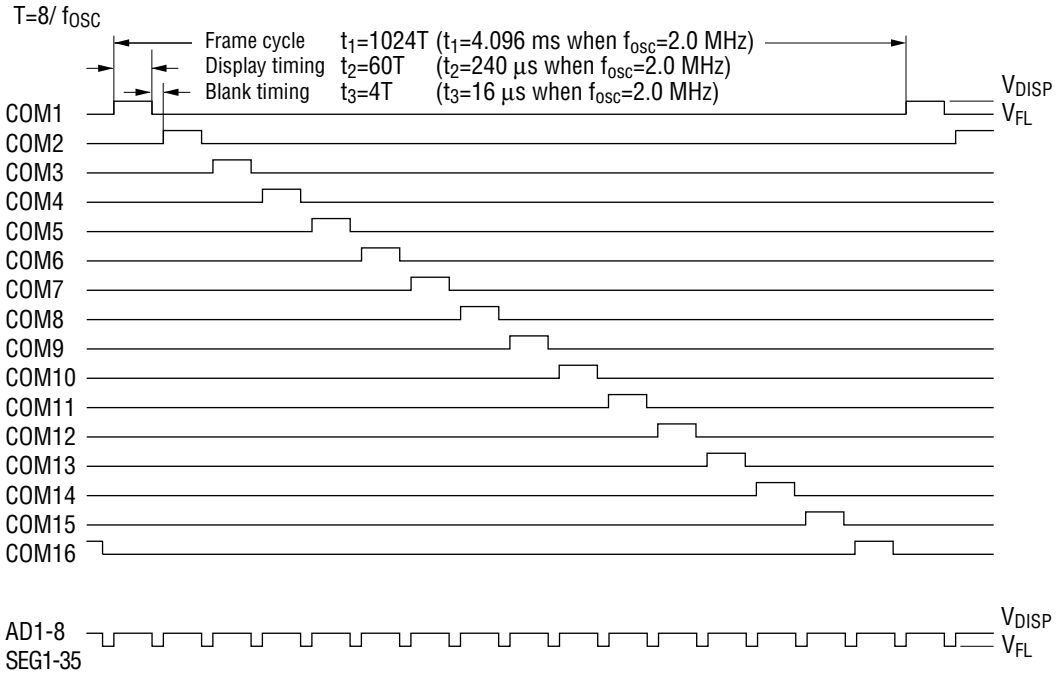
MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM00	RAM10														
0001	RAM01	RAM11														
0010	RAM02	RAM12														
0011	RAM03	RAM13														
0100	RAM04	RAM14														
0101	RAM05	RAM15														
0110	RAM06	RAM16														
0111	RAM07	RAM17														
1000	RAM08	RAM18														
1001	RAM09	RAM19														
1010	RAM0A	RAM1A														
1011	RAM0B	RAM1B														
1100	RAM0C	RAM1C														
1101	RAM0D	RAM1D														
1101	RAM0E	RAM1E														
1111	RAM0F	RAM1F														

MSM9200-02 ROM Code

00000000B (00H) to 00011111B (1FH) are the CGRAM addresses.

MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM00	RAM10														
0001	RAM01	RAM11														
0010	RAM02	RAM12														
0011	RAM03	RAM13														
0100	RAM04	RAM14														
0101	RAM05	RAM15														
0110	RAM06	RAM16														
0111	RAM07	RAM17														
1000	RAM08	RAM18														
1001	RAM09	RAM19														
1010	RAM0A	RAM1A														
1011	RAM0B	RAM1B														
1100	RAM0C	RAM1C														
1101	RAM0D	RAM1D														
1101	RAM0E	RAM1E														
1111	RAM0F	RAM1F														

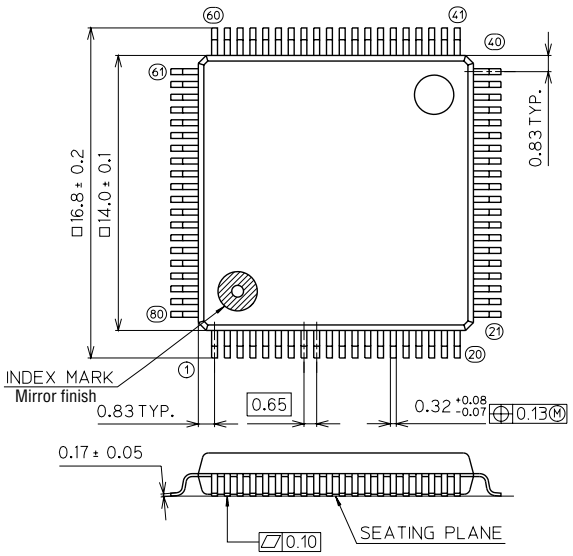
Digit Output Timing (for 16-digit display, at a duty of 15/16)

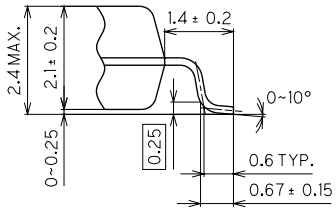


PACKAGE DIMENSIONS

(Unit : mm)

QFP80-P-1414-0.65-K





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.85 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).