OKI

MSM9405

Application Manual

IrDA Controller LSI

SECOND EDITION

ISSUE DATE: Jul. 2000

FEAL9405-02

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1. General Description

The MSM9405 is a communication controller conforming to the physical specification ver1.1 of IrDA, the international standard for infrared data communication.
By combining the MSM9405 with another microcontroller, a protocol stack, and an infrared transceiver module, equipment provided with IrDA-compliant communication function can be configured.
The MSM9405 is provided with a unique Extended-SIR mode to insert or remove BOF, EOF, and CRC by hardware. They were inserted or removed only by software before.
With the Extended-SIR mode, it is possibe to cut down the software development cost, to speed up the processing, and to reduce the ROM capacity.
Since the input and I/O pins except the XIN pin are composed of 5 V tolerant buffers, the MSM9405 can interface with 5 V systems.

1.1 Features

- Data transfer rates
  2400, 9600 bps; 19.2, 38.4, 57.6, 115.2 kbps; 0.576, 1.152, 4 Mbps
- Extended-SIR mode to support some functions of protocol

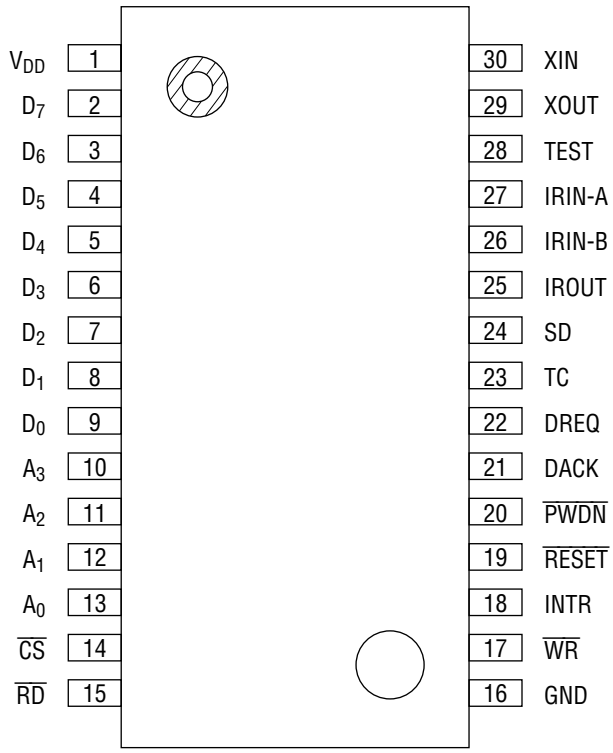
Mode	Transfer rate	Insert or remove BOF	Insert or remove CRC	Insert or remove EOF	Insert or remove CE	Insert or remove "0"	Insert or remove Preamble
SIR	2.4 to 115.2 kbps	SW	SW	SW	SW	—	—
Extended-SIR	2.4 to 115.2 kbps	HW	HW	HW	HW	—	—
MIR	0.576 M, 1.152 Mbps	HW	HW	HW	—	HW	—
FIR	4 Mbps	HW	HW	HW	—	—	HW

CE: Control Escape Byte
SW: Supported by software (microcontroller)
HW: Supported by hardware (MSM9405)

- Host interface
  8-bit data bus : D0 to D7
  DMA transfer : DREQ, DACK, TC
  Interrupt : INTR
  Address : A_0 to A_3
  Control signal : $\overline{CS}$, $\overline{RD}$, $\overline{WR}$
- Infrared transceiver module control signal : SD
- Built-in 32-byte transmit-receive FIFOs
- Power down mode
- Built-in oscillator circuit
- Crystal oscillation frequency : 18.432 MHz (other than 4 Mbps data rate)
  : 48 MHz (up to 4 Mbps data rate)
- Operating voltage (V_{DD}) : 2.7 to 3.6 V
- Package:
  30-pin plastic SSOP (SSOP30-P-56-0.65-K) (Product name : MSM9405MB)

1.2 Pin Configuration & Pin Descriptions

Pin Configuration (Top View)



30-Pin Plastic SSOP

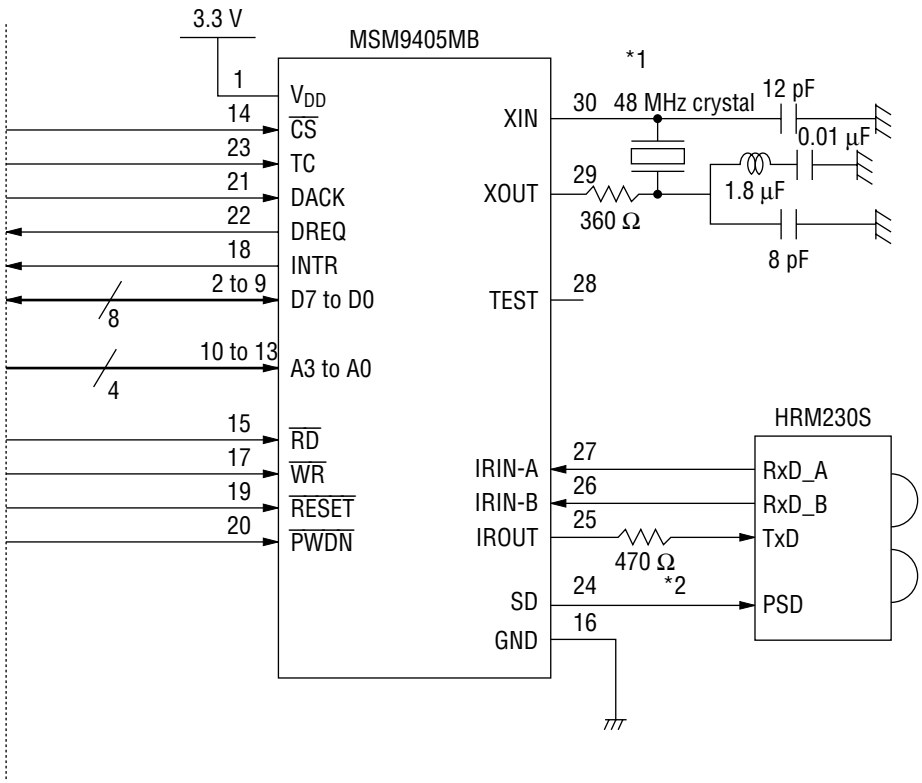
Pin Descriptions

Function	Pin	Symbol	Type	Description
Infrared Transceiver Module Interface	27	IRIN-A	I	Receive signal input A. (2.4 kbps to 4 Mbps) *1
	26	IRIN-B	I	Receive signal input B. (0.576 to 4 Mbps) When connecting this device to an infrared transceiver module, tie this pin high or low if the number of the receive signal output pins that the module has is only one. *1
	25	IROUT	O	Transmit signal output. Active high.
	24	SD	O	Infrared transceiver module control signal output. Becomes active when $\overline{PWDN}$ is set low. *1 This pin must be left open if connecting this device to an infrared transceiver module having no shutdown pins.
Microcontroller Interface	2-9	D_7-D_0	I/O	Data input-output.
	10-13	A_3-A_0	I	Register address inputs.
	14	$\overline{CS}$	I	Chip select input. Active low. When low, read and write signals are enabled.
	15	$\overline{RD}$	I	Read signal input. Active low.
	17	$\overline{WR}$	I	Write signal input. Active low.
	18	INTR	O	Interrupt request signal output. *1
DMA Controller Interface	22	DREQ	O	DMA Request signal output. *1
	21	DACK	I	DMA acknowledge signal input. *1
	23	TC	I	DMA transfer end signal input. *1
Others	20	$\overline{PWDN}$	I	Power down control. Active low. When set low, oscillation stops and the device enters power down (low supply current) mode.
	19	$\overline{RESET}$	I	System reset input. Active low. When set low, the internal registers are initialized.
	28	TEST	O	Test. Must be left open.
	30	XIN	I	Crystal connect.
	29	XOUT	O	Crystal connect.
	1	V_{DD}	—	Power supply.
	16	GND	—	Ground.

*1 Either active high or active low can be selected depending on the register setting.

1.3 External Connection Example

Microcontroller interface



*1: Crystal units manufactured by MEIDENSHA CORP. are recommended. For details, refer to section 3.2, "Selecting the Crystal Unit."

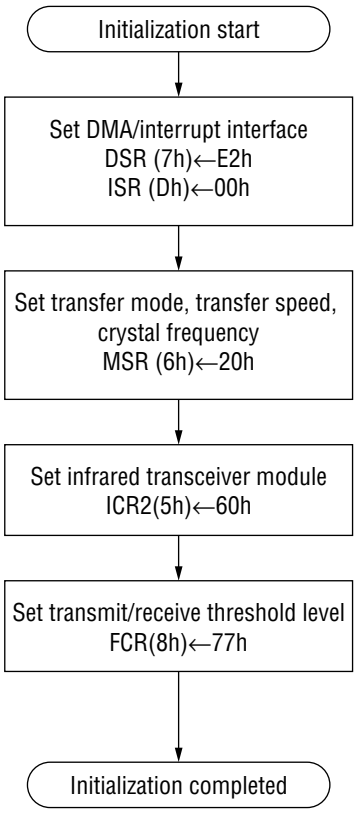
*2: The value of this resistor is the reference value for connection to a HRM230S device manufactured by Stanley Electric Co., Ltd. Consult with individual module manufacturers regarding peripheral components for each infrared transceiver module.

Note: Since the input and I/O pins except the XIN pin are composed of 5 V tolerant buffers, the MSM9405 can interface with 5 V systems.
The I/O pins should not be pulled up to 5 V supply.

2. Transmit/Receive Procedure Examples

2.1 Initialization Procedure Example

Transfer mode: SIR
Transfer speed: 9600 bps
Crystal: 48 MHz
Infrared transceiver module: HRM230S
(manufactured by Stanley Electric Co., Ltd.)
DMA controller: 8237 type
(DMA transfer is disabled)



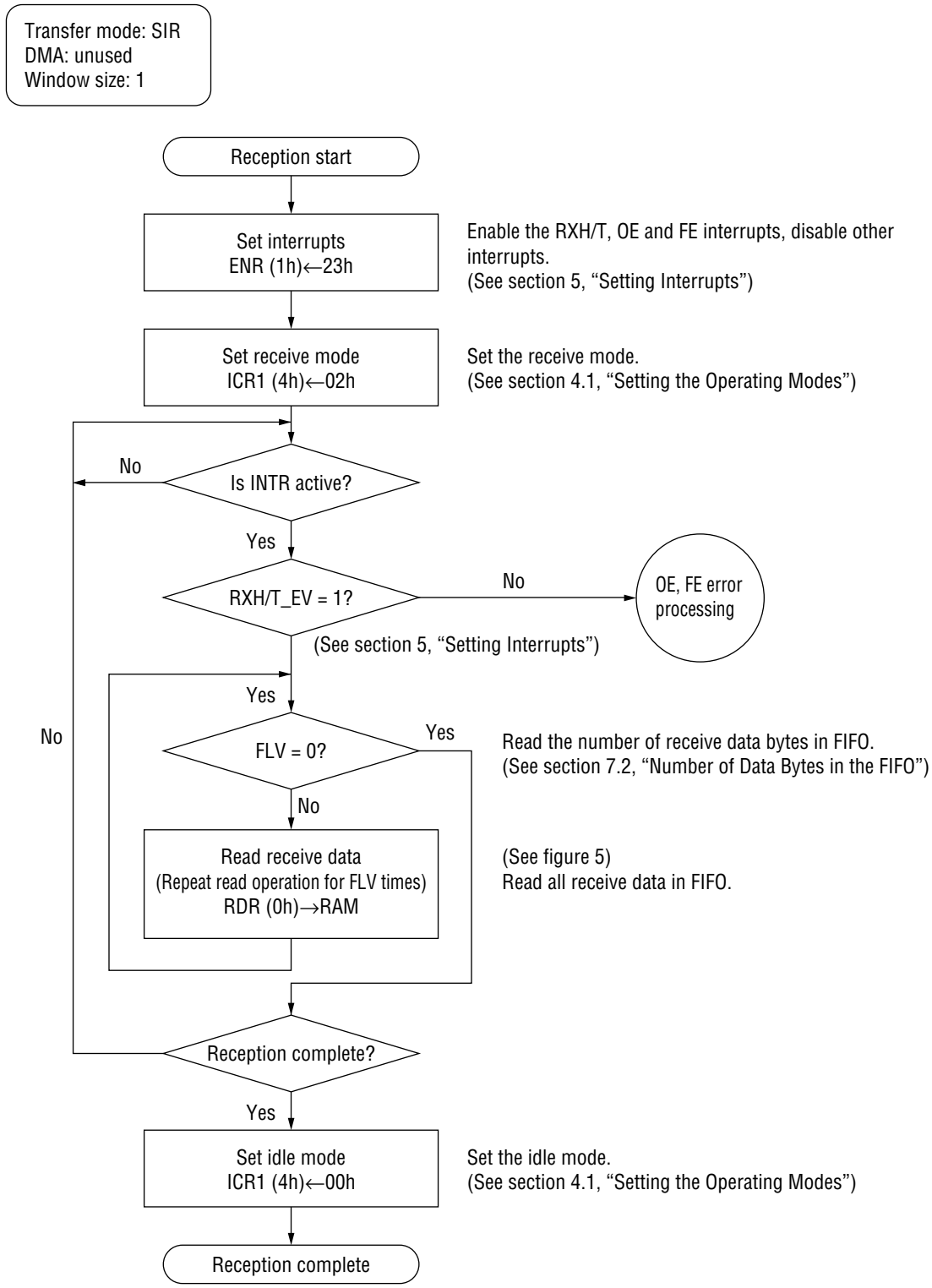
Set the DMA interface according to the 8237 type.
(Set DREQ = Active High; DACK = Active Low; TC = Active High; DMA threshold during transmission = 32, during reception = 0; DMA transfer mode = single; disable DMA transfer)
(See section 3.3, “Setting the DMAC Interface”)
Set INTR = Active Low.
(See section 3.4, “Setting the Interrupt Interface”)

Set transfer mode to SIR, transfer speed to 9600 bps, and crystal frequency to 48 MHz.
(See section 3.2, “Selecting the Crystal Unit”, section 4.2, “Setting the Transfer Mode”, and section 4.3, “Setting the Transfer Speed”)

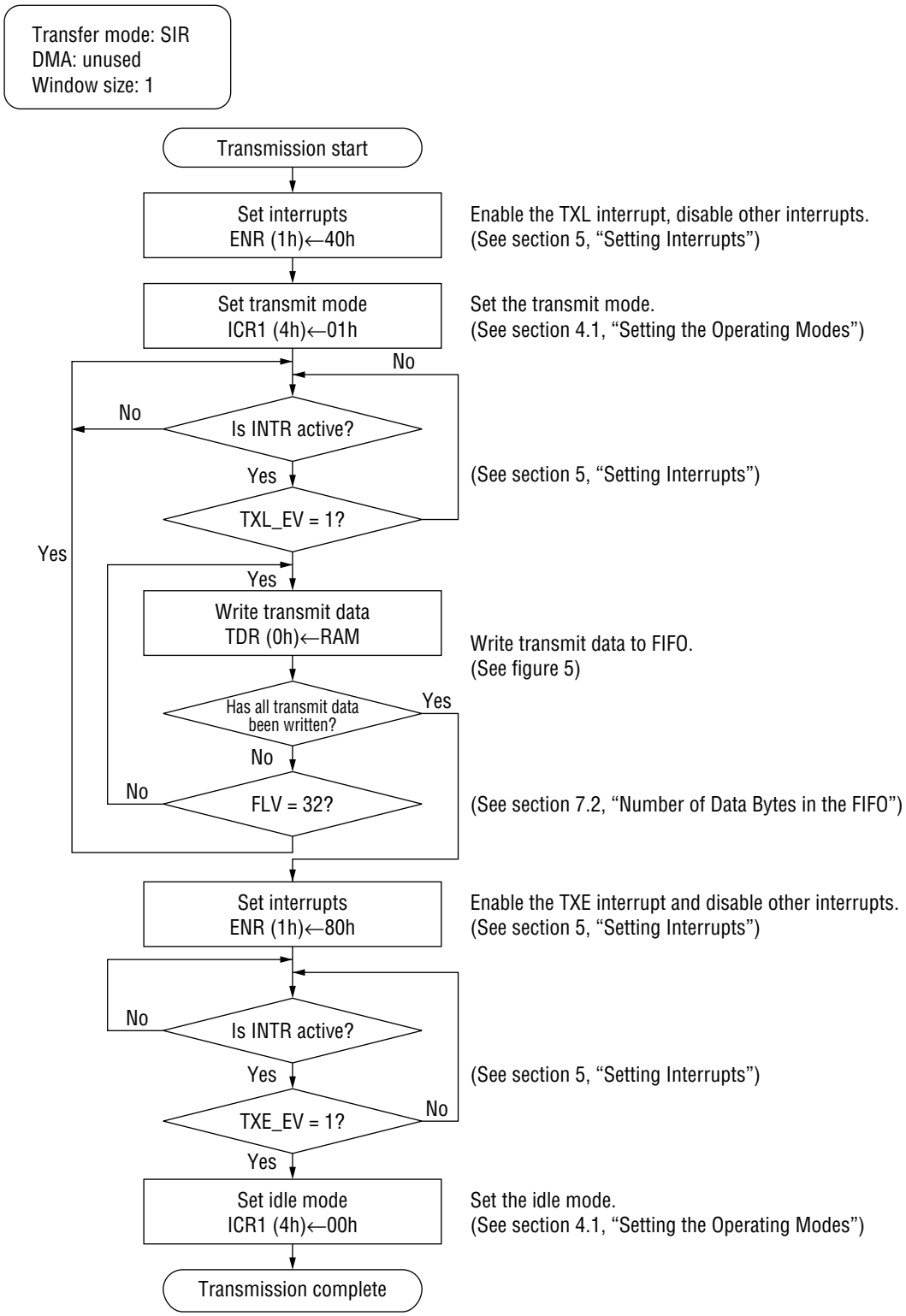
Set shutdown signal polarity and receive pulse polarity to the HRM230S polarity, set the receive pin setting to 2 pins.
(See section 3.1, “Setting the Infrared Transceiver Module Interface”)

Set the threshold level for both transmit and receive to “14”.
(See section 7.1, “Setting the Transmit/Receive Threshold Levels”)

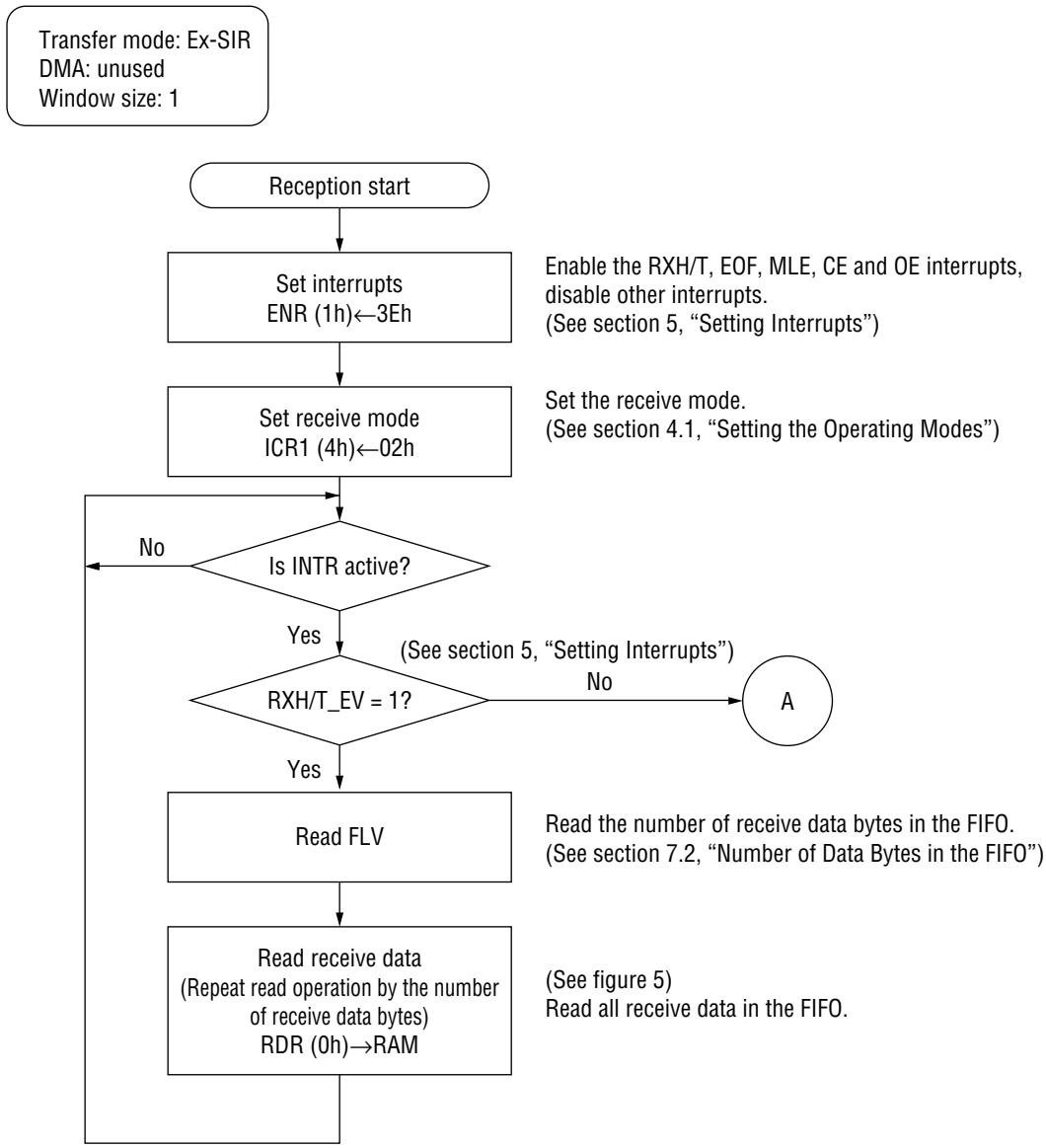
2.2 Receive Procedure Example: SIR



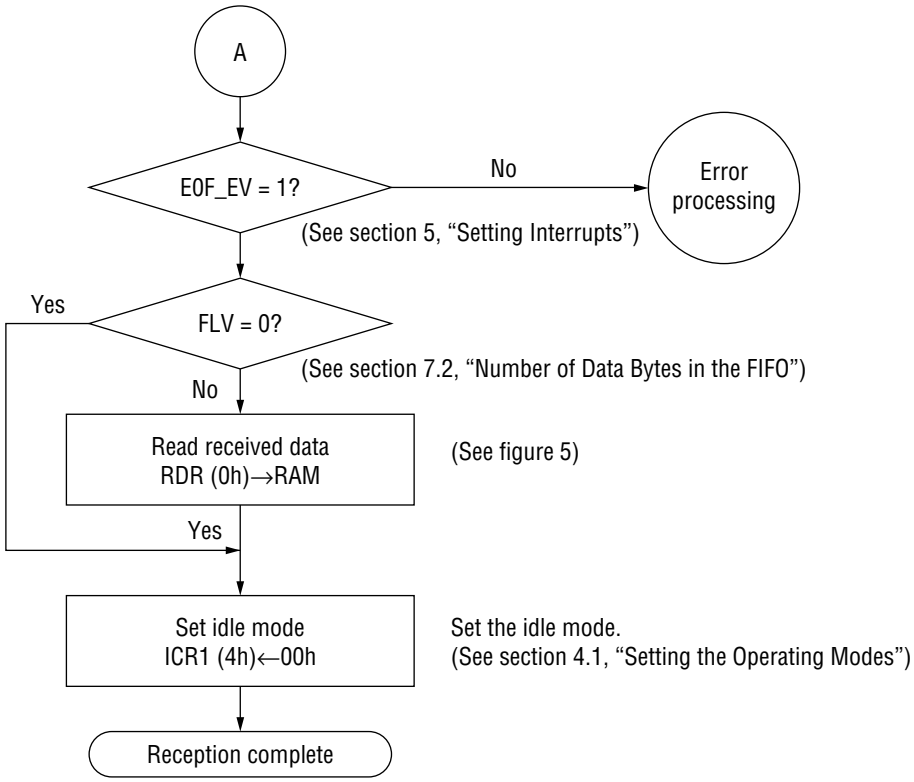
2.3 Transmit Procedure Example: SIR



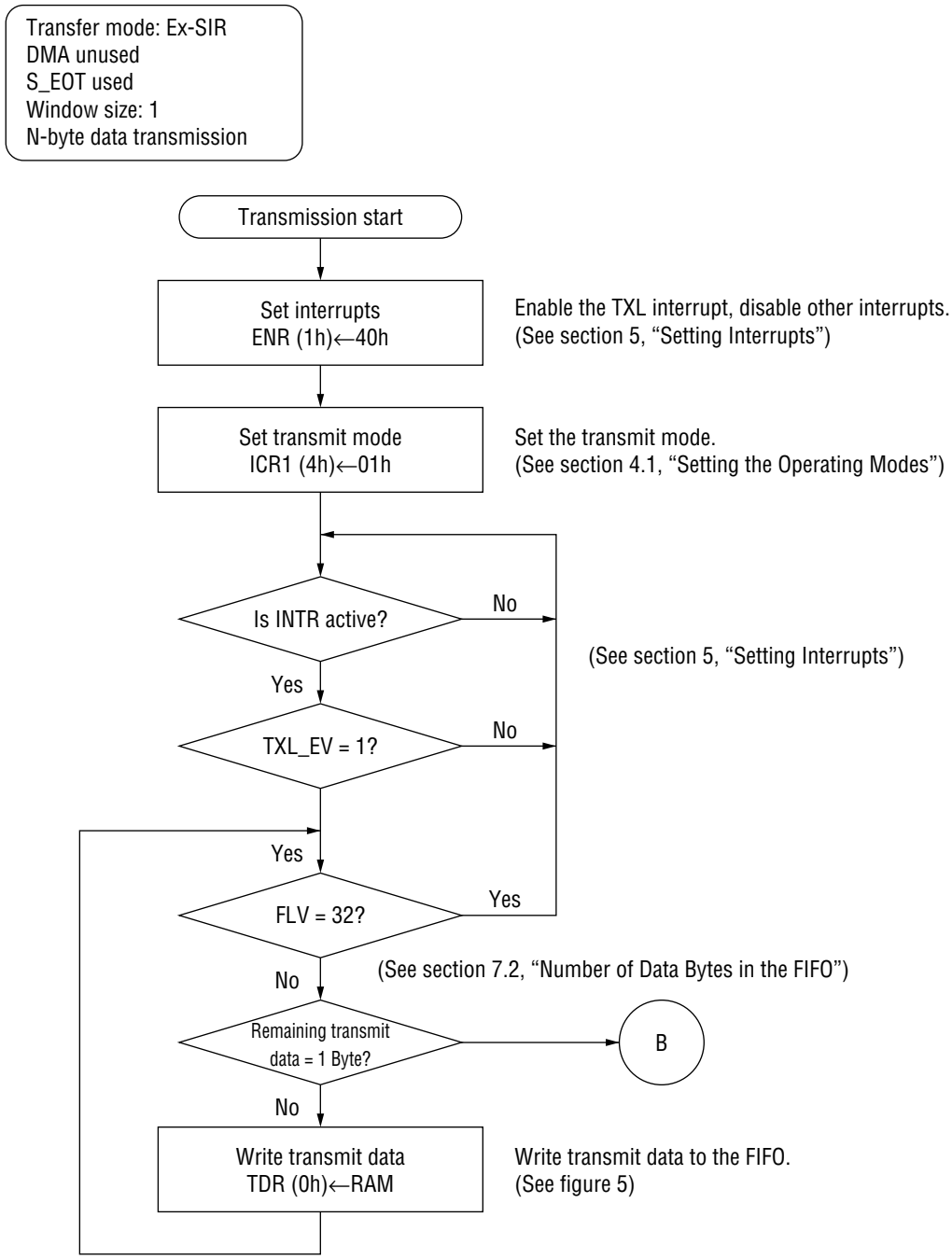
2.4 Receive Procedure Example: Ex-SIR



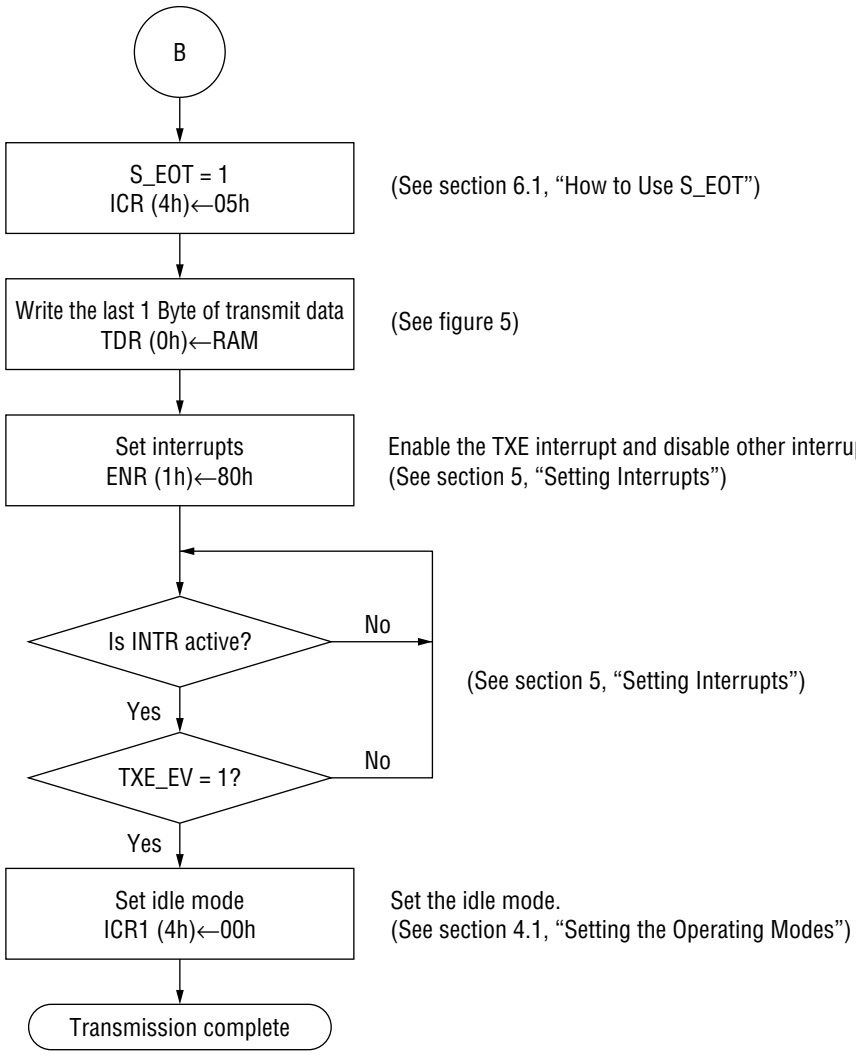
Receive Procedure Example: Ex-SIR (continued)



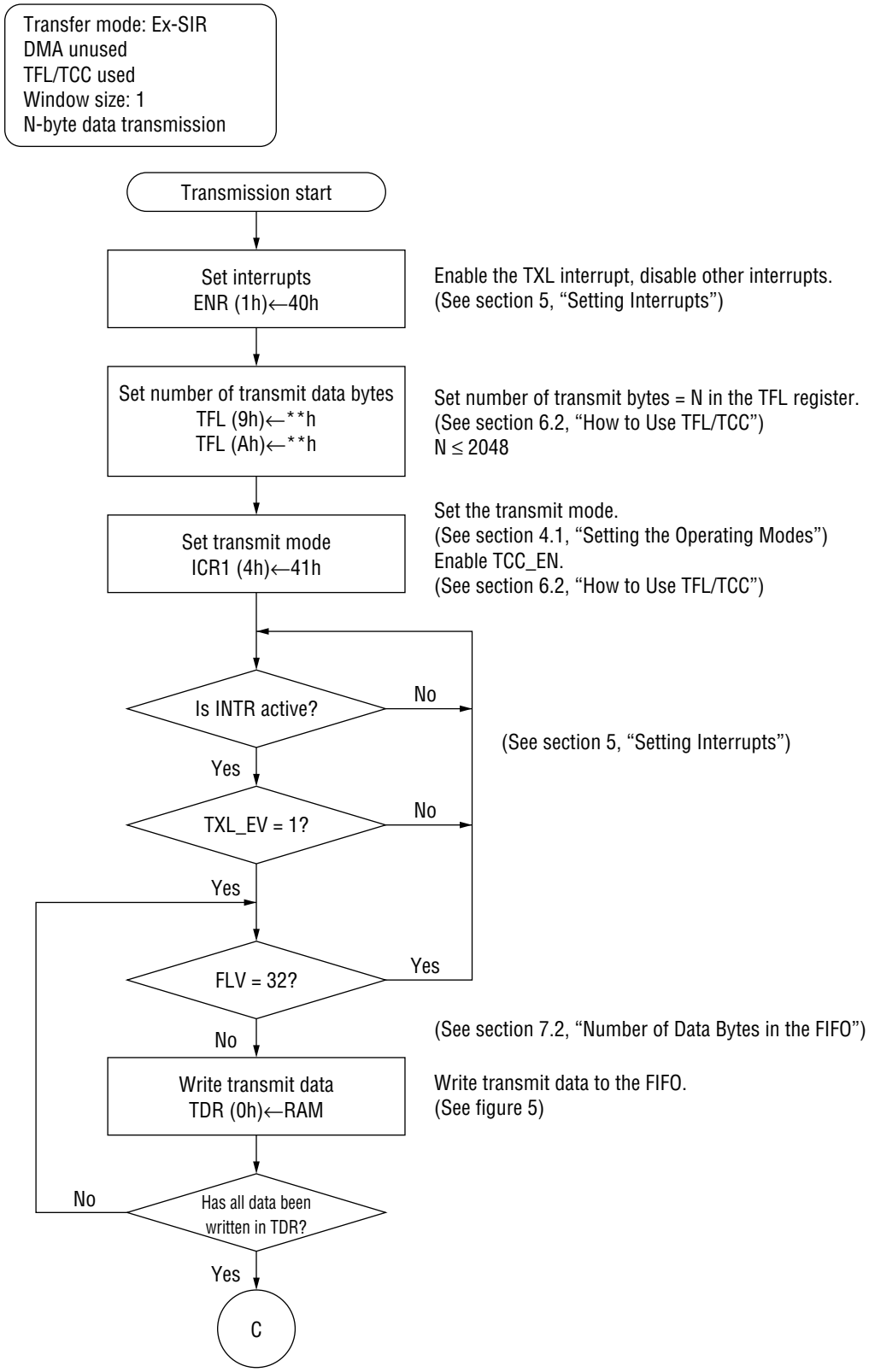
2.5 Transmit Procedure Example: Ex-SIR (S_EOT is used)



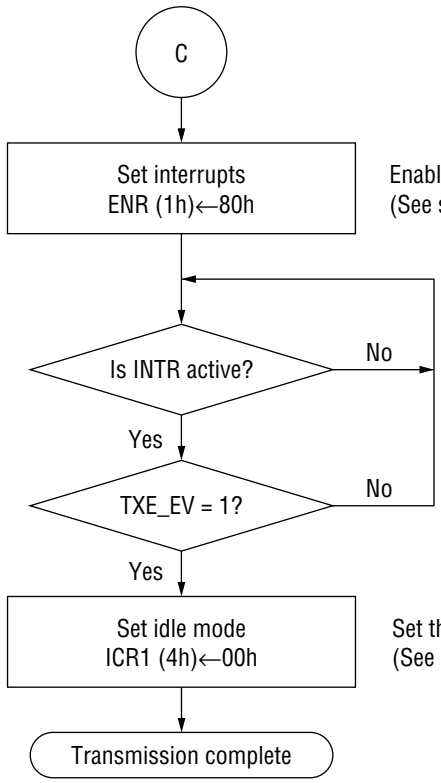
Transmit Procedure Example: Ex-SIR (S_EOT is used) (continued)



2.6 Transmit Procedure Example: Ex-SIR (TFL/TCC are used)



Transmit Procedure Example: Ex-SIR (TFL/TCC are used) (continued)

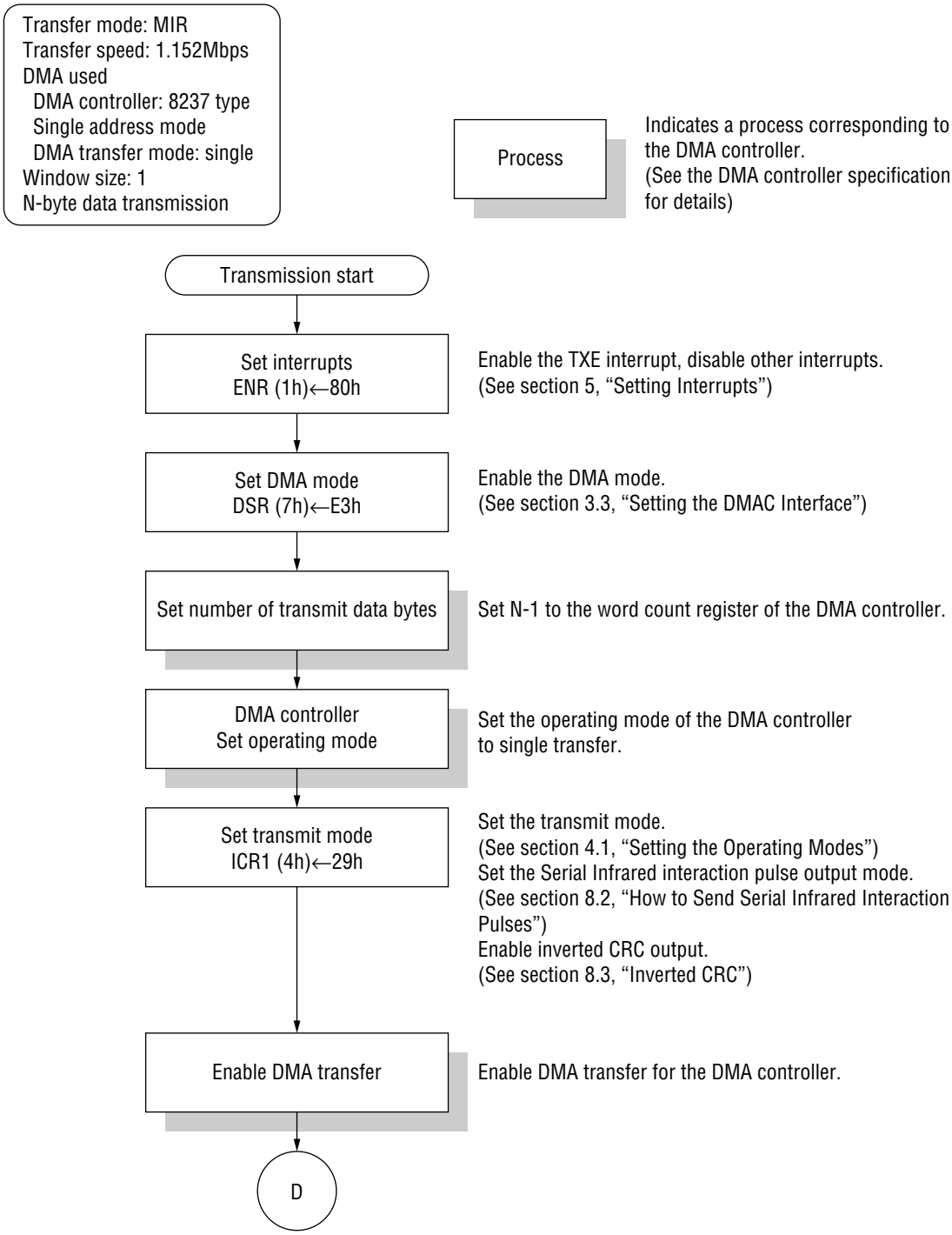


Enable the TXE interrupt and disable other interrupts.
(See section 5, "Setting Interrupts")

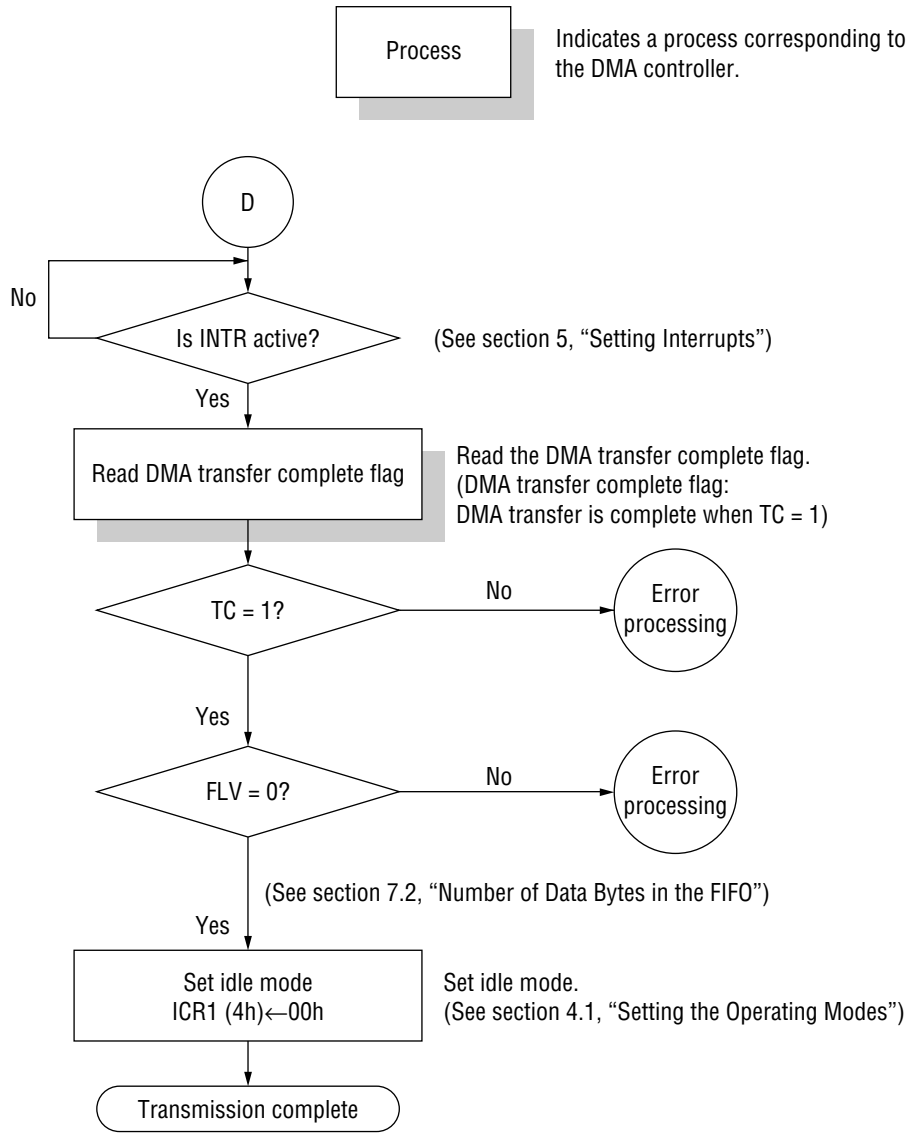
(See section 5, "Setting Interrupts")

Set the idle mode.
(See section 4.1, "Setting the Operating Modes")

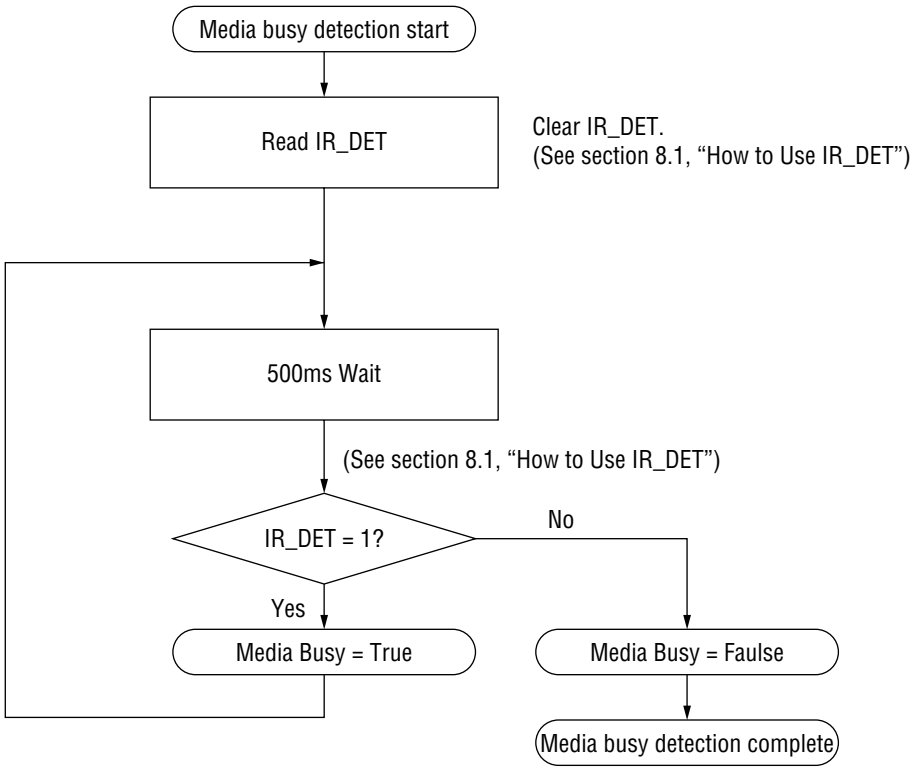
2.7 Transmit Procedure Example: MIR



Transmit Procedure Example: MIR (continued)



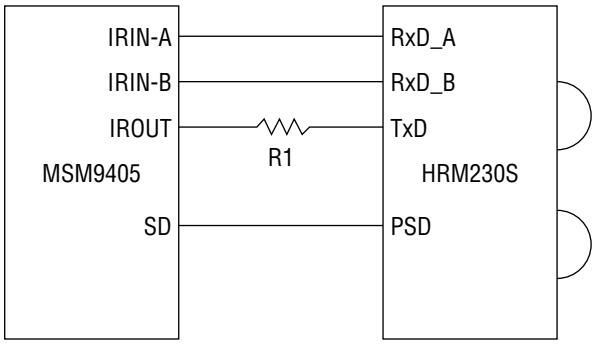
2.8 Media Busy Detection Procedure Example



3. External Interface Settings

3.1 Setting the Infrared Transceiver Module Interface

The MSM9405 contains the following 4 pins for interfacing to an infrared transceiver: IRIN-A, IRIN-B, IROUT, and SD. Selection of receive pins (IRIN-A, IRIN-B) and selection of polarity for IRIN-A, IRIN-B, and SD pins are performed by bit 6 (SD_INV), bit 5 (IRIN_SL), and bit 4 (RXINV) of the ICR2 register (address 5h). These pins and settings allow connection to various types of infrared transceiver modules. An example showing the connection to the HRM230S infrared transceiver module (manufactured by Stanley Electric Co., Ltd.) is shown in figure 1.



R1 = 470 Ω (reference value)
Figure 1

3.1.1 SD_INV

The SD pin (pin 24) is linked to the input signal of the $\overline{\text{PWDN}}$ pin (pin 20).
If connecting to a infrared transceiver module that has an active-low power-down pin (shuts down when at a low level), set SD_INV to 1. In this state, if a low level is input to the $\overline{\text{PWDN}}$ pin of the MSM9405, the SD pin of the MSM9405 will output a low level and the infrared transceiver module will enter the shut down state. (The MSM9405 will enter the power-down mode.)
If connecting to a transceiver module that has an active-high power-down pin (shuts down when at a high level), set SD_INV to 0. In this state, if a low level is input to the $\overline{\text{PWDN}}$ pin of the MSM9405, the SD pin of the MSM9405 will output a high level and the infrared transceiver module will enter the shut down state. (The MSM9405 will enter the power-down mode.)
If the infrared transceiver module to be connected does not contain a shut down pin, leave the SD pin of the MSM9405 open (unconnected) and SD_INV can be set to either 0 or 1.

3.1.2 IRIN_SL

The MSM9405 has two receive signal input pins, IRIN-A and IRIN-B.
If IRIN_SL is set to 1, the input signal will be received from IRIN-A when the transfer speed is ≤ 115.2 kbps, and from IRIN-B when the transfer speed is ≥ 0.576 Mbps.
If IRIN_SL is set to 0, the input signal will be received only from IRIN-A, regardless of the transfer speed.
Set IRIN_SL to 1 when connecting to an infrared transceiver module that contains 2 receive signal output pins. Set IRIN_SL to 0 when connecting to an infrared transceiver module that contains 1 receive signal output pin.

3.1.3 RXINV

The RXINV setting selects polarity of the receive signal.
If RXINV is set to 0, the IRIN-A (or IRIN-B) polarity is active low. If set to 1, the polarity is active high.
Set RXINV to 0 when connecting to an infrared transceiver module that will output a high level when there is no signal and a low level pulse when an infrared pulse is received. Set RXINV to 1 when connecting to an infrared transceiver module that will output a low level when there is no signal and a high level pulse when an infrared pulse is received.

3.1.4 MS_EN

MS_EN (bit 7 of the ICR1 register) is utilized when an infrared transceiver module (Note) is used that requires the mode to be set externally. If a "1" is written to this bit, the MSM9405 will operate as follows corresponding to the transfer mode. After operation is complete, MS_EN is automatically reset to "0."

When the MSM9405 is in the FIR mode:

1. The SD pin is set to a high level *2, and the IROUT pin is set to a high level.
2. After approximately 300 ns, set the SD pin to a low level *2
3. Approximately 300 ns after step 2 (above), set the IROUT pin to a low level

When the MSM9405 is in the SIR, Ex-SIR, and MIR modes:

1. The SD pin is set to a high level *2 and the IROUT pin is set to a low level
2. After approximately 300 ns, set the SD pin to a low level *2
3. Maintain the IROUT pin at a low level from approximately 300 ns after step 2 (above)

MS_EN cannot be used when a 18.432 MHz crystal is used (XT_SL = 1, see section 3.2, "Selecting the Crystal Unit")

Note: *1 For methods to set the modes of infrared transceiver modules, refer to the data sheet for each module.
*2 When the SD pin is active high.
When the SD pin is active low, the level is inverted.

3.2 Selecting the Crystal Unit

A 48 MHz or 18.432 MHz external crystal Unit can be connected to the MSM9405.
If an 18.432 MHz unit is used, the transfer speed will be up to 1.152 Mbps.
Selection of the crystal unit is performed by bit 4 (XT_SL) of the MSR register (address 6h).
Set XT_SL to 0 if a 48 MHz crystal unit is to be used, and set XT_SL to 1 if an 18.432 MHz crystal unit is to be used.

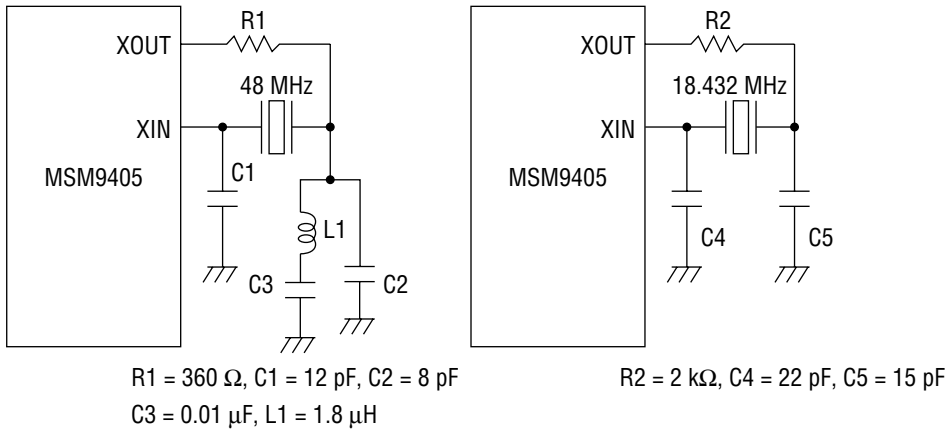


Figure 2

The following crystal units manufactured by MEIDENSHA Corp. are recommended. Depending upon the crystal or usage conditions, appropriate R, L, and C values will differ. Please consult with the crystal manufacturer.
48 MHz: 49U3H 48 MHz, MS-3H 48 MHz
18.432 MHz: 49U3H 18.432 MHz, MS-3H 18.432 MHz

3.3 Setting the DMAC Interface

The DSR register (address 7h) performs various settings related to DMA transfer.

3.3.1 DMA_EN

DMA_EN (bit 0) enables or disables the DMA transfer. DMA transfer is disabled when DMA_EN is "0" and transfer is enabled when DMA_EN is "1."

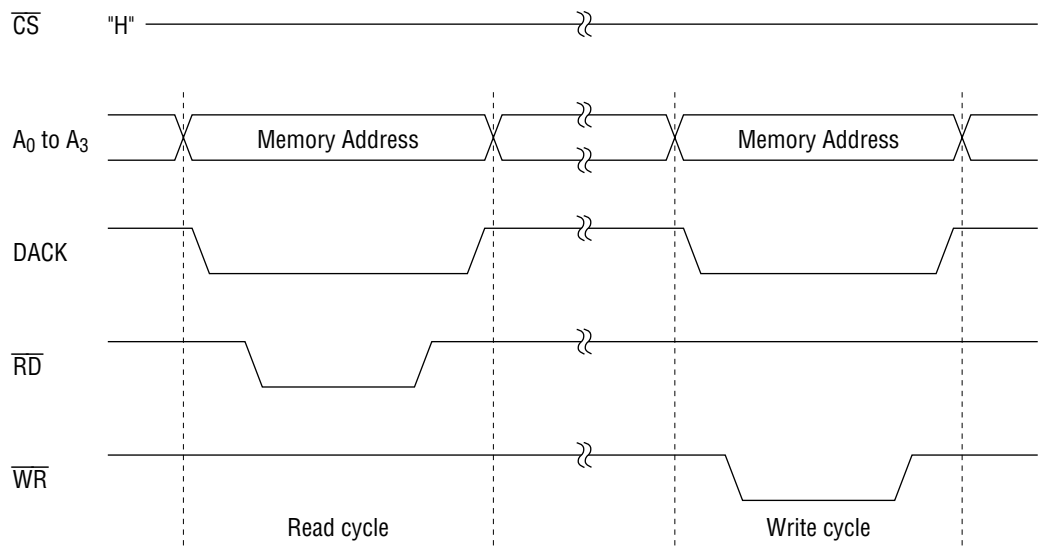
3.3.2 DMA_SL1, DMA_SL0

DMA_SL1 and DMA_SL0 (bits 2 and 1) select the DMA transfer mode. Modes can be selected as follows. (See Figure 3 and Figure 4)

DMA_SL_1	DMA_SL_0	Function
0	0	Supports single address mode DMA transfer If the $\overline{RD}$ signal is asserted while DACK is active, a read cycle*1 begins. If the $\overline{WR}$ signal is asserted while DACK is active, a write cycle*2 begins. When DACK is active, access address 0h (TDR/RDR) independently of A0 to A3.
0	1	Supports single address mode DMA transfer If the $\overline{WR}$ signal is asserted while DACK is active, a read cycle*1 begins. If the $\overline{RD}$ signal is asserted while DACK is active, a write cycle*2 begins. When DACK is active, access address 0h (TDR/RDR) independently of A0 to A3.
1	0	Supports dual address mode DMA transfer Access TDR/RDR via $\overline{CS}$ and A0 to A3.
1	1	Reserved

*1 Read cycle: Memory→MSM9405
*2 Write cycle: MSM9405→Memory

• Single address mode (DMA_SL1 = 0, DMA_SL0 = 0, DACK: active low)



• Single address mode (DMA_SL1 = 0, DMA_SL0 = 1, DACK: active low)

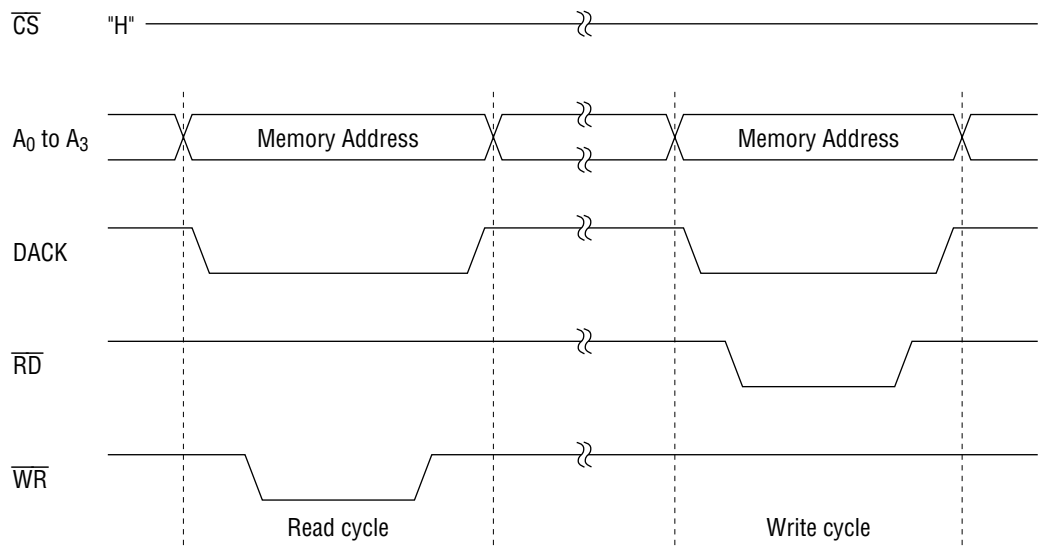
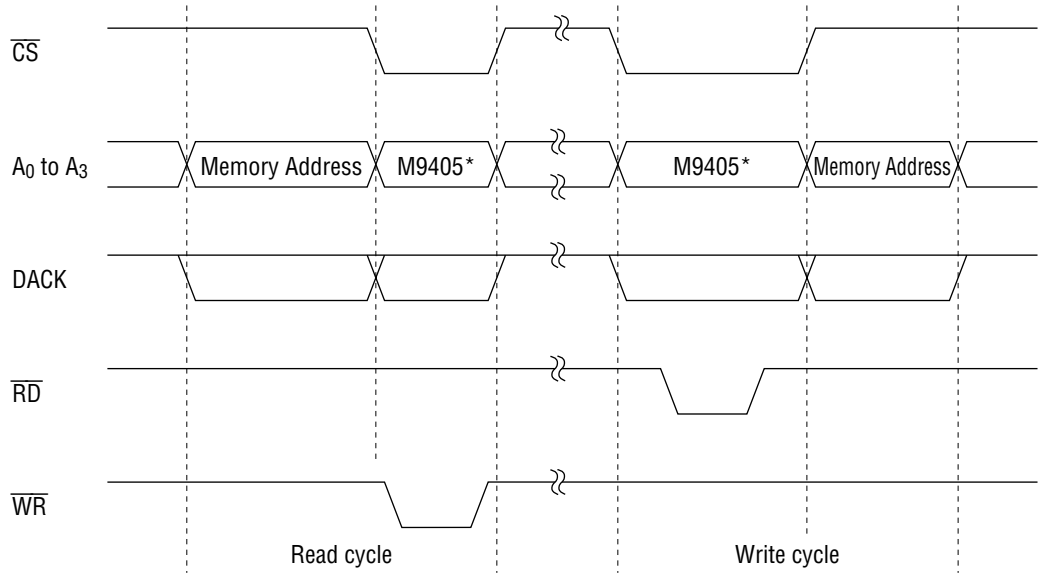


Figure 3

• Dual address mode (DMA_SL1 = 1, DMA_SL0 = 0, DACK: active low)



* Specify TDR/RDR (address 0h).

Figure 4

3.3.3 DMATH1, DMATH0

DMATH1 and DMATH0 (bits 4 and 3) determine the threshold level at which the DREQ signal is deasserted.
When DMA is enabled during reception, the DREQ signal is asserted when the number of receive data bytes in FIFO is equal to or greater than the receive threshold level set in the FCR register. (See section 7.1, "Setting the Transmit/Receive Threshold Levels")
And when data is read from FIFO and the number of data bytes in FIFO is equal to the value set by DMATH, the DREQ signal is deasserted.
When DMA is enabled during transmission, the DREQ signal is asserted when the number of transmit data bytes in FIFO is smaller than the transmit threshold level set in the FCR register. (See section 7.1, "Setting the Transmit/Receive Threshold Levels")
And when data is written in FIFO and the number of data bytes in FIFO is equal to the value set by DMATH, the DREQ signal is deasserted.
A value greater than TXTH (see section 7.1, "Setting the Transmit/Receive Threshold Levels") should be set to DMATH during transmission, and a value smaller than RXTH should be set to DMATH during reception.

$DMATH_1$	$DMATH_0$	During transmission	During reception
0	0	32	0
0	1	30	2
1	0	28	4
1	1	24	8

3.3.4 TC_INV, DACK_INV, DREQ_INV

TC_INV (bit 5) sets the polarity of the TC signal. When TC_INV is "0", the TC signal is active low and when TC_INV is "1", the TC signal is active high.
DACK_INV (bit 6) sets the polarity of the DACK signal. When DACK_INV is "0", the DACK signal is active high and when DACK_INV is "1", the DACK signal is active low.
DREQ_INV (bit 7) sets the polarity of the DREQ signal. When DREQ _INV is "0", the DREQ signal is active low and when DREQ _INV is "1", the DREQ signal is active high.
When the DMA transfer function is not used, the DREQ pin should be open and the DACK and TC pins should be connected to V_{DD} or GND.
DREQ_INV may be set to either "0" or "1". However, DACK_INV and TC_INV should be set so that the DACK and TC pins become inactive.

3.4 Setting the Interrupt Interface

ISR (address Dh) sets the interrupt interface.
INTR_INV (bit 0) sets the polarity of the INTR signal. When INTR _INV is "0", the INTR signal is active low and when INTR _INV is "1", the INTR signal is active high.
When the interrupt function is not used, the INTR pin should be open and INTR-INV can be set to either "0" or "1".
Bit 7 through bit 1 are reserved for future use.

4. Communication Mode Settings

4.1 Setting the Operating Modes

The MSM9405 has the following four operating modes. Operation in any of the modes may be directly controlled externally via a microcontroller or other device. If the $\overline{\text{PWDN}}$ pin is pulled to a low-level, the MSM9405 enters the power-down mode. Or, with a high-level applied to the $\overline{\text{PWDN}}$ pin, bits 1 and 0 (RX_EN and TX_EN) of the ICR1 register can set the receive or transmit modes.

$\overline{\text{PWDN}}$	RX_EN	TX_EN	Operating Mode
L	X	X	Power-down
H	0	0	Idle
H	0	1	Transmit
H	1	X	Receive

X: Don't care

4.1.1 Power-Down Mode

In the power-down mode, the MSM9405 stops oscillation and enters a low supply current state. In this state, do not access the TDR/RDR register (address 0h). Other registers may be accessed (addresses 1h to Dh).
After the power-down mode is released, wait at least 20 ms before performing transmission or reception.

4.1.2 Idle Mode

In the idle mode, the MSM9405 does not perform transmission or reception. The register at address 0h operates as TDR, and transmit data can be written to the FIFO. The FIFO cannot be read.

4.1.3 Transmit Mode

In the transmit mode, the register at address 0h operates as TDR, and transmit data can be written to the FIFO. The FIFO cannot be read. Transmission automatically begins when there is data in the FIFO. Data written to the FIFO differs depending upon the transfer mode. Write data for the shaded sections of figure 5. The MSM9405 automatically adds sections outside the shaded areas. (See section 6, "How to Add FCS/EOF.")
In the Ex-SIR mode, a specific code (C0, C1, 7D) escape sequence (7D is inserted in front of the specific code and the 5th bit of the specific code is inverted) is automatically performed. In the MIR mode, 0 is inserted (if there are consecutive 1's at the 5th bit or after, 0 is inserted at the 6th bit).
When transmission is completed, after all transmit data has been written to the FIFO, TXE_EV has become "1", and after both FIFO and TSR (See APPENDIX-A "Block Diagram" for Transmitter Shift Register (TSR)) are empty, set TX_EN to 0. (See section 5, "Setting Interrupts.")

* To shift the receive mode to the transmit mode in the DMA mode, the following operations should be taken.
   1. Set the idle mode.
   2. Set the bits 3 to 0 (TXTH 3 to 0) of the FCR register (address 8h) to "0000".
   3. Write 1 byte of dummy data to FIFO.

4. Set the value of TXTH to an arbitrary value.
5. Write 1 byte of dummy data to FIFO again.
6. Clear the dummy data written to FIFO by using FCLR.
7. Start transmission.

4.1.4 Receive Mode

In the receive mode, the register at address 0h operates as RDR, and the FIFO can be read. Writing to the FIFO is not possible.
If BOF code (Note) is input to the IRIN-A (or IRIN-B) pin, reception will begin. Thereafter, serial pulse strings input to the IRIN-A (or IRIN-B) pin are transformed into 8-bit parallel data and are written to the FIFO.
Data written to the FIFO differs depending upon the transfer mode. This data is the shaded sections of figure 5.
The MSM9405 automatically deletes sections outside the shaded areas.
However, if in the Ex-SIR mode, MIR mode, and FIR mode, the MSM9405 cannot detect EOF (STO) due to errors after reception begins and the BOF code of the next frame is input, the MSM9405 will write the BOF code into the FIFO as data without identifying the BOF code as the begining of the frame.
In this case, setting RX_EN to "0" and then to "1" allows the MSM9405 to detect the BOF code that is input thereafter as the begining of the frame.
In the Ex-SIR mode, in contrast to a transmission, the specific code (C0, C1, 7D) is automatically reconstructed (7D in front of specific code is deleted and 5th bit of specific code is inverted). In the MIR mode, 0 is deleted (if there are consecutive 1s at the 5th bit or before, the 0 at the 6th bit is deleted).

Note : BOF code

SIR : BOF (C0h)
Ex-SIR : BOF (C0h)
MIR : STA (7Eh)
FIR : Preamble (1000000010101000) + STA (00001100000011000110000001100000)

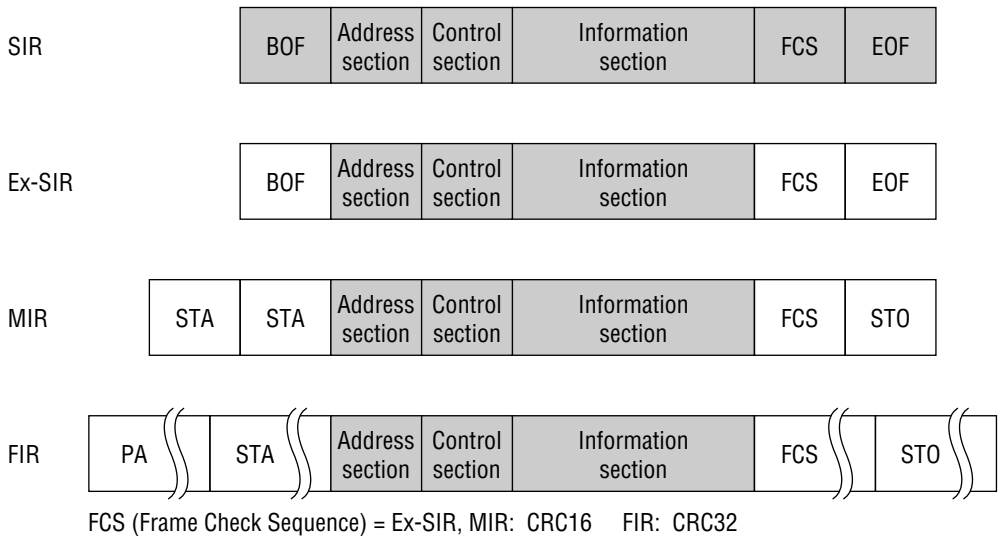


Figure 5

4.2 Setting the Transfer Mode

The MSM9405 can be set to one of the following 4 different transfer modes using bit 1 (IRSL1) and bit 0 (IRSL0) of the MSR register (at address 6h)

IRSL1	IRSL0	Mode	Transfer speed
0	0	SIR	2.4 to 115.2 kbps
0	1	Extended-SIR	2.4 to 115.2 kbps
1	0	MIR	0.576 to 1.152 Mbps
1	1	FIR	4 Mbps

4.3 Setting the Transfer Speed

The MSM9405 can select the transfer speed using bit 7 to bit 5 (DRS2 to 0) of the MSR register (at address 6h). There are different transfer speeds selectable for each transfer mode as shown below.

Bit 7 to bit 5	During SIR mode	During MIR mode	During FIR mode
000	2400 bps	0.576 Mbps	Reserved
001	9600 bps	1.152 Mbps	4 Mbps
010	19.2 kbps	Reserved	Reserved
011	38.4 kbps	Reserved	Reserved
100	57.6 kbps	Reserved	Reserved
101	115.2 kbps	Reserved	Reserved
110	Reserved	Reserved	Reserved
111	Reserved	Reserved	Reserved

4.4 Setting the Number of BOFs (STAs)

The MSM9405 can set the number of BOFs (STAs), that indicate the beginning of a frame during Ex-SIR mode or MIR mode, using bit 3 to bit 0 (SBF3 to 0 or MBF3 to 0) of the ICR2 register. The number of BOFs (STAs) set by SBF3 through SBF0 (or MBF3 to MBF0) are automatically appended in front of the data written to the FIFO, and then transmitted.
These bits are not used in the SIR and FIR modes.
During the FIR mode, 16 preambles of 16 chips and 1 STA of 32 chips are automatically appended in front of the data written to the FIFO. (See figure 5.)

ICR2 bit 3 to bit 0	During Ex-SIR mode	During MIR mode
0000	1	2
0001	2	3
0010	3	4
0011	4	5
0100	5	8
0101	7	12
0110	9	16
0111	13	24
1000	17	Reserved
1001	25	Reserved
1010	49	Reserved
1011	Reserved	Reserved
1100	Reserved	Reserved
1101	Reserved	Reserved
1110	Reserved	Reserved

5. Setting Interrupts

The MSM9405 has 9 factors of interrupts. Bit 7 (TXE_EV), bit 6 (TXL_EV), bit 5 (RXH/T_EV), bit 4 (EOF_EV), bit 3 (MLE_EV), bit 2 (CE_EV), bit 1 (OE_EV), bit 0 (FE_EV) of the EIR register (address 2h), and bit 0 (TOUT) of the LSR register (address 3h) indicate interrupts, and change to 1 when an interrupt occurs.
The ENR register (address 1h) can enable and disable each interrupt. All 8 bits correspond to the bit array of the interrupts indicated by the EIR register. Enable necessary interrupts by setting the corresponding bits to 1. Setting a bit to 0 disables the corresponding interrupt. Even if the corresponding bits in the ENR register are 0 (disabled) each bit of the EIR register will still change to 1 when an interrupt event occurs.

5.1 TXE_EV, TXE_IE

TXE_EV is set to 1 if all of the data written in the FIFO is transmitted and both the FIFO and TSR (Transmitter Shift Register: See APPENDIX-A "Block Diagram") become empty. If the EIR register is read, it is reset to 0. TXE_EV will be set to 1 if the FIFO and TSR become empty not only in the middle of a frame, but also after normal completion of a frame transfer.
The significance of TXE_EV differs depending upon the transfer mode and the generated timing. When in the MIR or FIR mode, if an interrupt occurs before 1 frame of data has been written to the FIFO, TXE_EV indicates that the transmit data write was not complete, and that the data is fragmented. In this case, data written hereafter to the FIFO will not be transmitted. To restart transmission, it is necessary to first reset TX_EN to 0 and then set TX_EN to 1.
In all the modes (SIR, Ex-SIR, MIR and FIR), if an interrupt occurs after 1 frame of data has been written to the FIFO, TXE_EV indicates that transmission of that frame is complete.
TXE_IE enables and disables the interrupt asserted by TXE_EV.
TXE_IE and TXE_EV are valid in all the modes (SIR, Ex-SIR, MIR and FIR).

5.2 TXL_EV, TXL_IE

During the transmit or idle mode, if the number of transmit data bytes in the FIFO is less than the transmit threshold level set by bits 3 through 0 (TXTH3 to TXTH0) of the FCR register (address 8h), then TXL_EV is set to 1 (See section 7.1, "Setting the Transmit/Receive Threshold Levels"). Transmit data is written to the FIFO and if the number of transmit data bytes in the FIFO is equal to or greater than the transmit threshold level, TXL_EV is set to 0.
In the receive mode, TXL_IE is always set to 0.
TXL_EV is a trigger to write the transmit data.
TXL_IE enables and disables the interrupt asserted by TXL_EV.
TXL_IE and TXL_EV are valid in all the modes (SIR, Ex-SIR, MIR and FIR).

5.3 RXH/T_EV, TOUT, RXH/T_IE

When in the receive mode, RXH/T_EV is set to 1 if the number of receive data bytes in the FIFO is equal or greater than the receive threshold level (See section 7.1, "Setting the Transmit/Receive Threshold Levels) set by bits 7 through 4 (RXTH3 to RXTH0) of the FCR register (address 8h) or if a timeout is generated. When a timeout is generated, bit 0 (TOUT) of the LSR register (address 3h) is also set to 1. If RXH/T_EV has been set to 1 because the received number of data bytes is equal or greater than the receive threshold level, the received data is read. And the number of received data bytes in the FIFO is less than the receive threshold level, RXH/T_EV is set to 0. If RXH/T_EV has been set to 1 due to generation of a timeout, RXH/T_EV will be reset to 0 when the received data is read. TOUT will also be reset to 0 when the received data is read.
In the transmit and idle modes, RXH/T_EV is always set to 0.
The condition causing timeout in the SIR and Ex-SIR modes:

At least 1 or more bytes of data are in the FIFO and time Tout has elapsed since the last data was written from the receiver shift register (RSR) to the FIFO. During this interval, FIFO data has not been read by the CPU or DMA controller.

Tout = $4 \times 8 \times 1$/baud rate baud rate: transfer speed (2.4 to 115.2 kbps)

The condition causing timeout in the MIR and FIR modes:

At least 1 or more bytes of data are in the FIFO and 69.5 µs has elapsed since the last data was written from the receiver shift register to the FIFO. During this interval, FIFO data has not been read by the CPU or DMA controller. RXH/T_IE enables and disables the interrupt asserted by RXH/T_EV.

RXH/T_EV is a trigger to read the receive data.
RXH/T_EV, RXH/T_IE, and TOUT are valid in all the modes (SIR, Ex-SIR, MIR and FIR).

5.4 EOF_EV, EOF_IE

During the receive mode, EOF_EV is set to 1 when the last byte of the information section of the receive frame reaches the bottom of the FIFO (= RDR). If the EIR register is read, EOF_EV is set to 0.
EOF_EV indicates that the next data to be read is the last data in the frame.
EOF_IE enables and disables the interrupt asserted by EOF_EV.
EOF_IE and EOF_EV are valid in the Ex-SIR, MIR and FIR modes.
In the SIR mode, set EOF_IE to 0 and do not use EOF_EV.

5.5 MLE_EV, MLE_IE

During the receive mode, MLE_EV is set to 1 when a frame is received whose length exceeds the maximum receive data size as set by the MDS(L) and MDS(H) registers (addresses Bh, Ch). If the EIR register is read, MLE_EV will be reset to 0.
MLE_IE enables and disables the interrupt asserted by MLE_EV.
MLE _IE and MLE _EV are valid in the Ex-SIR, MIR and FIR modes.
In the SIR mode, set MLE_IE to 0 and do not use MLE_EV.
The data size set in the MDS register does not include CE, FCS, BOF and EOF. (In the SIR mode, set MLE_IE to 0 and do not use MLE_EV.)
CE (Control Escape Byte) = 7D
FCS (Frame Check Sequence) = Ex-SIR, MIR: CRC16 FIR:CRC32

5.6 CE_EV, CE_IE

In the receive mode, a CRC check of the receive frame is performed and CE_EV is set to 1 when an error occurs.
If the EIR register is read, CE_EV will be reset to 0.
CE_EV indicates that there is an error in the received frame.
CE _IE enables and disables the interrupt asserted by CE _EV.
CE _IE and CE _EV are valid in the Ex-SIR, MIR and FIR modes.
In the SIR mode, set CE_IE to 0 and do not use CE_EV.

5.7 OE_EV, OE_IE

During the receive mode, OE_EV is set to 1 when the FIFO already full of 32 bytes of receive data, and the next receive data is completely received in the receiver shift register (RSR) (See Appendix-A, “Block Diagram”).
If the EIR register is read, OE_EV will be reset to 0.
When OE_EV is asserted, data in the RSR is not written to the FIFO. Data in the receiving shift register will be overwritten by the next receive data.
OE _EV indicates that the received data could not be read and a portion of the received data is lost.
Even if OE_EV is asserted, CE_EV will not be asserted.
OE _IE enables and disables the interrupt asserted by OE _EV.
OE _IE and OE _EV are valid in all the modes (SIR, Ex-SIR, MIR and FIR modes).

5.8 FE_EV, FE_IE

In the receive mode, FE_EV is set to 1 if there is no stop bit in the received data.
If the EIR register is read, FE_EV will be reset to 0.
FE _IE enables and disables the interrupt asserted by FE _EV.
FE _IE and FE _EV are valid in the SIR and Ex-SIR modes.
In the MIR and FIR modes, set FE_IE to 0 and do not use FE_EV.

6. How to Add FCS/EOF

FCS (Frame Check Sequence) = Ex-SIR, MIR: CRC16 FIR: CRC32

6.1 How to Use S_EOT

Disable TCC by setting bit 6 (TCC_EN) of the ICR1 (address 4h) register to 0 or set the value greater than the number of bytes (Note) of the frame to be transmitted to the TFL register (addresses 9h and Ah). Set the operating mode of the MSM9405 to transmit by setting the ICR1 register's bit 1 (RX_EN) to 0 and bit 0 (TX_EN) to 1. Write the transmit data to the TDR register. Just prior to writing the last data of the frame, write a 1 to bit 4 (S_EOF) of the ICR1 register. The MSM9405 will recognize data written to the TDR register as the last data of that frame, FCS and EOF (STO) are then added and the frame is transmitted. After EOF is transmitted, S_EOF is automatically reset to 0.

6.2 How to Use TFL/TCC

Enable TCC by setting bit 6 (TCC_EN) of the ICR1 register to 1 and set the number of bytes (Note) of the frame to be transmitted to the TFL register. Set the operating mode of the MSM9405 to the transmit mode by setting the ICR1 register's bit 1 (RX_EN) to 0 and bit 0 (TX_EN) to 1.
Write the transmit data to the TDR register. When 1 is written in TX_EN, the value of TFL previously set as a frame length is loaded into TCC.
TCC is a counter to count down the number of transmit data bytes.
The value of TCC is decremented by 1 each time when 1 Byte is transmitted.
When the value of TCC is zero, the MSM9405 recognizes that the last data byte of the frame has been transmitted and automatically transmits FCS and EOF together with it.
When BOF of the next frame is transmitted, the value of TFL is loaded into TCC again.
Set CTEST (bit 7 of the ICR2 register) to 1 to access TFL and set CTEST to 0 to read TCC.

6.3 How to Use TC

The TC signal can be used when writing data with a DMA controller that has a TC output. Disable TCC by setting bit 6 (TCC_EN) of the ICR1 register to 0 or set the value greater than the number of bytes (Note) of the frame to be transmitted to the TFL register. Set the operating mode of the MSM9405 to transmit by setting the ICR1 register's bit 1 (RX_EN) to 0 and bit 0 (TX_EN) to 1. Write the transmit data to the TDR register. When the TC signal is received from the DMA controller, the data written at that time will be recognized as the end of the frame, FCS and EOF (STO) will be added and the frame transmit.

Note : Number of bytes of the frame does not include CE, FCS, BOF (STA), and EOF (STO).

7. FIFO

7.1 Setting the Transmit/Receive Threshold Levels

The MSM9405 can set the receive threshold level with bits 7 to 4 (RXTH3 to RXTH0) of the FCR register (address 8h) and the transmit threshold level with bits 3 to 0 (TXTH3 to TXTH0) of the FCR register.
In the receive mode, if the number of receive data bytes in the FIFO is equal to or greater than the receive threshold level set in the FCR register, an RXH interrupt is generated and RXH/T_EV of the EIR register is set to 1. (If DMA has been enabled, the DREQ signal will be asserted.) In this state, the FIFO data is read, and if the number of data bytes in the FIFO becomes less than the receive threshold level, RXH/T_EV is set to 0. (The FIFO data is read and when the number of data bytes in the FIFO becomes the same as the value set by DMATH (See section 3.3, "Setting the DMAC Interface"), the DREQ signal will be deasserted.)
In the transmit mode, if the number of receive data bytes in the FIFO is less than the transmit threshold level set in the FCR register, a TXL interrupt is generated and TXL_EV of the EIR register is set to 1. (If DMA has been enabled, the DREQ signal will be asserted.) In this state, the data is written to the FIFO, and if the number of data bytes in the FIFO becomes equal or greater than the transmit threshold level, TXL_EV is set to 0. (Data is written to the FIFO and when the number of data bytes in the FIFO becomes the same as the value set by DMATH, the DREQ signal will be deasserted.)
When setting the transmit and receive threshold levels, a value smaller than the value set by DMATH should be set to TXTH during transmission, and a value greater than the value set by DMATH should be set to RXTH during reception.

bit 3 to bit 0 (bit 7 to bit 4 for reception)	TX Threshold Level	RX Threshold Level
0000	Reserved	Reserved
0001	02	02
0010	04	04
0011	06	06
0100	08	08
0101	10	10
0110	12	12
0111	14	14
1000	16	16
1001	18	18
1010	20	20
1011	22	22
1100	24	24
1101	26	26
1110	28	28
1111	30	30

7.2 Number of Data Bytes in the FIFO

When in the transmit mode, bits 7 to 2 (FLV5 to FLV0) of the LSR register (address 3h) indicate the number of transmit data bytes currently in the FIFO. When in the receive mode, these bits indicate the number of receive data bytes currently in the FIFO. Bit 7 indicates MSB, and bit 2 indicates LSB.
A maximum of 85ns (at original oscillation of 48MHz) is required from the time when FIFO data is accessed until the value of the LSR register changes. (When the original oscillation is 18.432MHz, the maximum time is 130ns.)
Data in the FIFO (including TDR and RDR) and FLV5 through FLV0 are cleared by writing 1 to bit 4 (FCLR) of the ICR1 register (address 4h). After data is cleared in the FIFO, FCLR is automatically set to 0.

7.3 FCLR

The MSM9405 can clear data in the FIFO by using FCLR (bit 4 of the ICR1).
Setting the FCLR to "1" clears the FIFO (including TDR and RDR) and sets the FLV to "0". The TSR and RSR (Transmitter Shift Register and Receive Shift Register: see Appendix-A, "Block Diagram") are not cleared. The FCLR is automatically set to "0".

* In the transmit mode or idle mode, in case the FCLR has cleared the FIFO when the number of data bytes is more than the transmit threshold level, the TXL_EV event does not occur and the INTR and DREQ pins do not become active.
When starting transmission after clearing the FIFO, the following operations should be performed.
1. Set the idle mode.
2. Write 1 byte of dummy data to FIFO.
3. Clear the dummy data written to FIFO by using FCLR.
4. Start transmission.

8. Other Functions

8.1 How to Use IR_DET

Infrared pulses can be detected by monitoring bit 1 (IR_DET) of the LSR register (address 3h). In the SIR and Ex-SIR modes, if a 0.9s (minimum value of SIR pulse width during reception) or longer pulse is input to IRIN-A pin, IR_DET will be set to 1. If IR_DET is read, it is reset to 0. IR_DET is not used in the MIR and FIR modes.
IR_DET is cleared by setting FCLR to 1.

8.2 How to Send Serial Infrared Interaction Pulses

Setting bit 3 (IR_PLS) of the ICR1 register (address 4h) to 1 causes a serial infrared interaction pulse to be output. After the interaction pulse is output, IR_PLS is automatically set to 0.
After IR_PLS is set to 1, a serial infrared interaction pulse is output immediately after the first STO that is output.
Serial infrared interaction pulses are only output in the MIR and FIR modes. Serial infrared interaction pulses are not output in the SIR and Ex-SIR modes.

In MIR mode

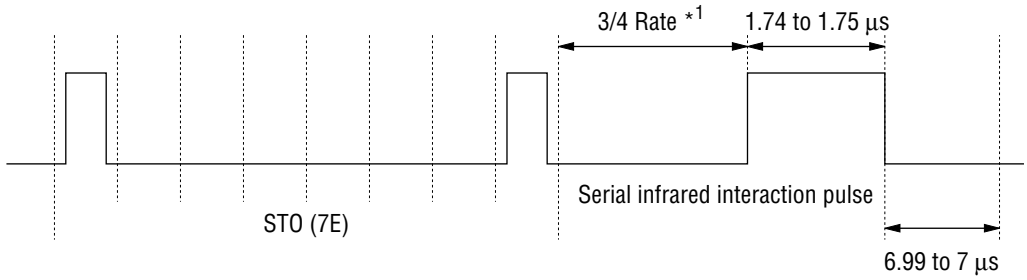


Figure 6

*1 Rate: 1/transfer speed

8.3 Inverted CRC

In the MIR and FIR modes, if TXE_EV is asserted during a frame transfer, the MSM9405 has a function to transmit inverted CRC (Note) and EOF, and to terminate subsequent data transmission. This function is enabled by setting bit 5 (CRC_INV) of the ICR1 register (address 4h) to 1, and is disabled by setting that bit to 0.
To restart data transmission that has been stopped by the assertion of TXE_EV, it is necessary to set bit 0 (TX_EN) of the ICR1 register to 0, and then set TX_EN to 1 again.
This function is invalid in the SIR and Ex-SIR modes.

Note : Inverted CRC is obtained by calculating the CRC of data transmitted before the TXE_EV event accurs, and then inverting all the calculated bits.

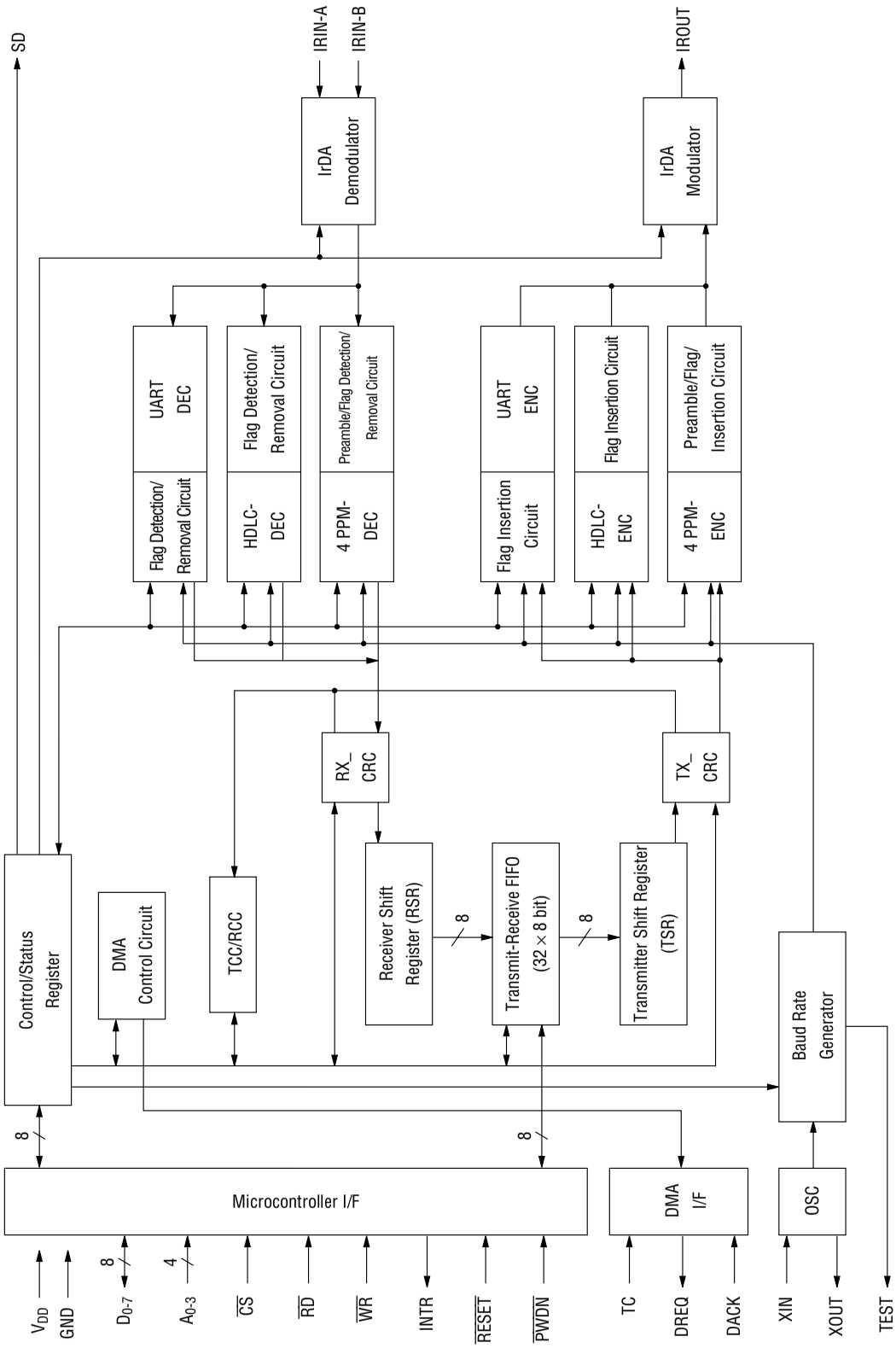
8.4 RST

The RST register (address Bh, Ch) is a register that stacks receive frame lengths. When one frame is completely received and EOF_EV (bit 4) of the EIR register (address 2h) has become 1, the receive frame length counted by the internal counter is pushed onto the RST register.
If the next frame is completely received and EOF_EV is set again to 1, the register value will be overwritten. If data from two or more frames is received together, read RST at every 1-frame reception.
Even if transmission and reception of the MSM9405 are switched, the RST value will be maintained.
RST can be read while bit 7 (CTEST) of the ICR2 register (address 5h) is 0. It is not possible to write to RST. While CTEST is 1, MDS will be read.
RST is valid in the Ex-SIR, MIR and FIR modes. RST is not used in the SIR mode.

Appendix A

Block Diagram

Appendix A Block Diagram



Appendix B

Electrical Characteristics

Appendix B Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	—	–0.5 to +4.6	V
Input Voltage	V_I	—	–0.5 to +6.0	V
Output Current	I_O	—	±10	mA
Power Dissipation	P_D	—	230	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	2.7 to 3.6	V
Operating Temperature	T_{op}	—	–20 to +70	°C
Crystal Oscillation Frequency	f_{OSC}	—	18.432 MHz ±200 ppm or 48 MHz ±100 ppm	—

DC Characteristics

(V_{DD} = 2.7 to 3.6 V, Ta = –20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
"H" Input Voltage	V_{IH1}	—	2.1	—	5.5	V	IRIN-A, IRIN-B, $\overline{PWDN}$
"L" Input Voltage	V_{IL1}	—	0	—	0.8		A_0 to A_3, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$,
Input Leakage Current	I_{LI1}	$V_I = V_{DD}$/0 V	—	—	±10	µA	TC, $\overline{RESET}$, DACK
"H" Input Voltage	V_{IH2}	—	2.1	—	5.5	V	D_0 to D_7
"L" Input Voltage	V_{IL2}	—	0	—	0.8		
Input Leakage Current	I_{LI2}	$V_I = V_{DD}$/0 V	—	—	±10	µA	
"H" Output Voltage	V_{OH1}	I_O = –4 mA	2.2*1	—	V_{DD}	V	
"L" Output Voltage	V_{OL1}	I_O = 4 mA	—	—	0.4		
"H" Output Voltage	V_{OH2}	I_O = –4 mA	2.2*1	—	V_{DD}	V	IROUT, INTR, DREQ, SD
"L" Output Voltage	V_{OL2}	I_O = 4 mA	—	—	0.4		
Supply Current	I_{DD}	—	—	—	30	mA	V_{DD}

*1 2.4 V when V_{DD} = 3.0 to 3.6 V

AC Characteristics

(V_{DD} = 2.7 to 3.6 V, Ta = –20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Read Pulse Width	t_{rpw}	—	120/70	—	—	ns	*1
Read Data Delay Time	t_{rdd}	—	—	—	60	ns	*3, *5
Read Data Hold Time	t_{rdh}	—	0	—	—	ns	*4, *6
Data Bus Open Time	t_{hz}	—	—	—	25	ns	
Read/Write Recovery Time	t_{rcv}	—	60	—	—	ns	
CS Setup Time	t_{css}	—	60	—	—	ns	
CS Hold Time	t_{csh}	—	0	—	—	ns	
Write Address Hold Time	t_{wah}	—	0	—	—	ns	
Write Pulse Width	t_{wpw}	—	120/70	—	—	ns	*1
Write Data Setup Time	t_{wds}	—	60	—	—	ns	*7
Write Data Hold Time	t_{wdh}	—	–10	—	—	ns	*7
Write Address Setup Time	t_{was}	—	–10	—	—	ns	
Interrupt Clear Time	t_{intr}	—	—	—	135/95	ns	*2
DACK Setup Time	t_{acs}	—	60	—	—	ns	
DREQ Clear Time	t_{drqr}	—	—	—	80	ns	*8
DACK Hold Time (during Read)	t_{achr}	—	60	—	—	ns	
DACK Hold Time (during Write)	t_{achw}	—	60	—	—	ns	
TC Pulse Width	t_{tcw}	—	25	—	—	ns	
TC Setup Time	t_{tcs}	—	15	—	—	ns	
TC Hold Time	t_{tch}	—	15	—	—	ns	
SIR Pulse Width	t_{spw}	Transmitter	—	1.63	—	µs	
		Receiver	0.9	—	—	µs	
SIR Data Rate Tolerance	SDRT	Transmitter	—	—	±0.87	%	
		Receiver	—	—	±1.0	%	
MIR Pulse width	t_{mpw}	Transmitter	—	218	—	ns	
		Receiver	100	—	—	ns	
MIR Data Rate Tolerance	MDRT	Transmitter	—	—	±0.1	%	
		Receiver	—	—	±0.2	%	
FIR Single Pulse Width	t_{fpw}	Transmitter	—	125	—	ns	
		Receiver	70	—	165	ns	
FIR Data Rate Tolerance	FDRT	Transmitter	—	—	±0.01	%	
		Receiver	—	—	±0.1	%	
FIR Double Pulse Width	t_{fdpw}	Transmitter	—	250	—	ns	
		Receiver	195	—	285	ns	
Reset Pulse Width	t_{rstw}	—	70	—	—	ns	

*1 120 ns when the master oscillation frequency is 18.432 MHz, and 70 ns when it is 48 MHz.
*2 135 ns when the master oscillation frequency is 18.432 MHz, and 95 ns when it is 48 MHz.
*3 That which occurs latest of the following is to be used for the data delay time (t_{rdd}): the change from A_0-A_3 invalid to valid, the change from $\overline{CS}$ high to low, and the change from $\overline{RD}$ high to low (in the PIO mode).

*4 That which occurs first of the following is to be used for the read data hold time (t_{rdh}): the change from A_0-A_3 valid to invalid, the change from $\overline{CS}$ low to high, and the change from $\overline{RD}$ low to high.

*5 That which occurs latest of the following is to be used for the data delay time (t_{rdd}): the change from DACK inactive to active and the change from $\overline{RD}$ high to low (in the DMA mode).

*6 That which occurs first of the following is to be used for the read data hold time (t_{rdd}): the change from DACK active to inactive and the change from $\overline{RD}$ low to high (in the DMA mode).

*7 That which occurs first of the following is to be used for the write data setup time and write data hold time (t_{wds} and t_{wdh}): the change from DACK active to inactive and the change from $\overline{WR}$ low to high.

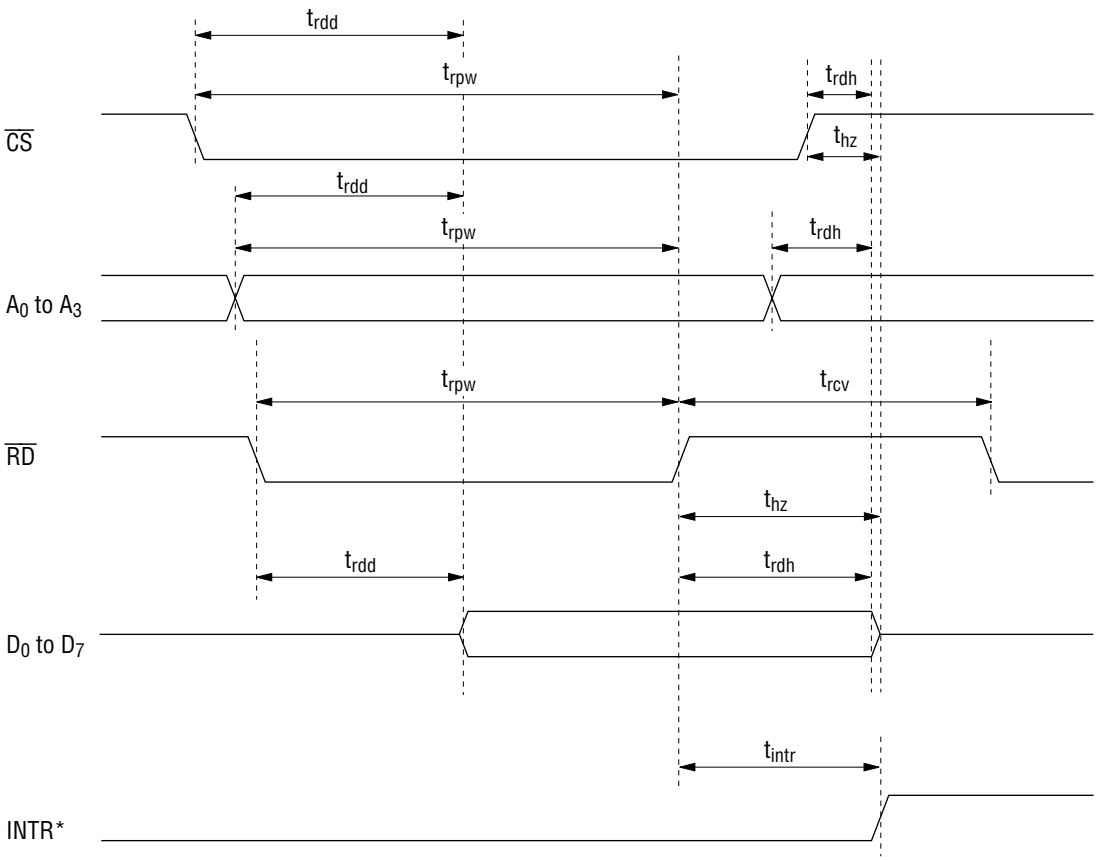
*8 That which occurs latest of the following is to be used for the DREQ clear time (t_{drqr}): the change from DACK low to high and the change from $\overline{WR}$ (or $\overline{RD}$) high to low.

Appendix C

Timing Diagram

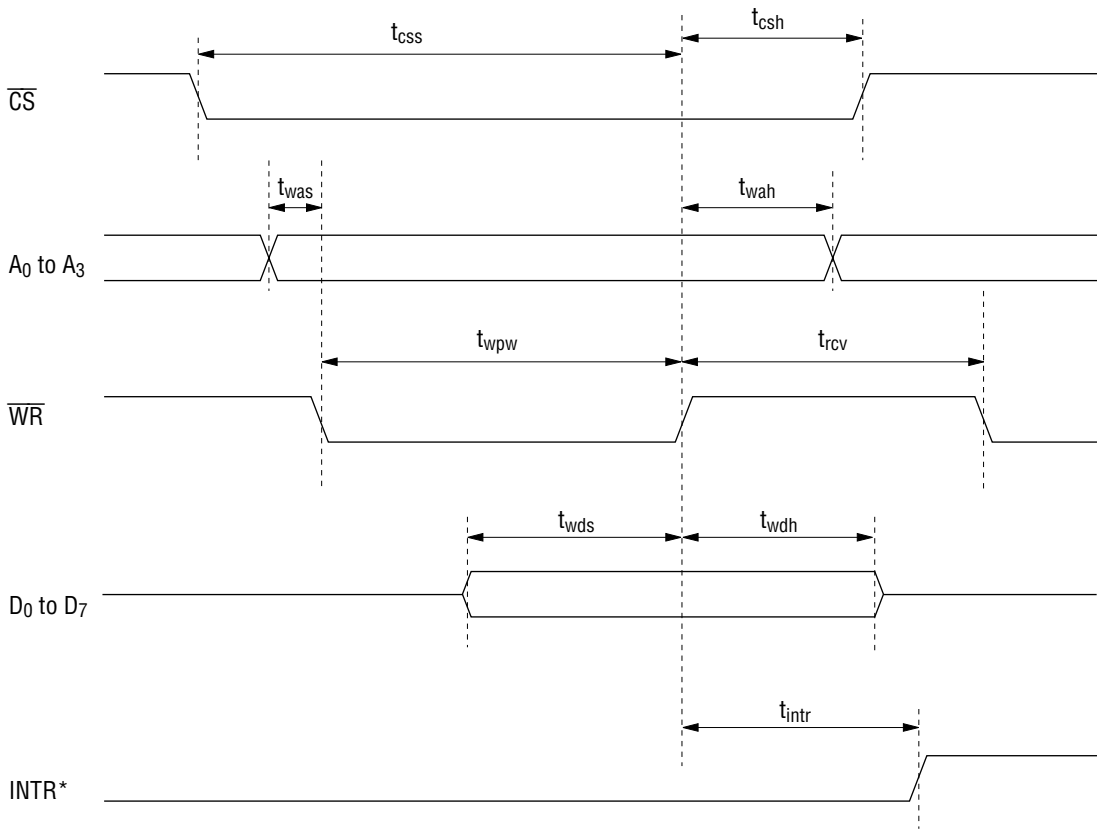
Appendix C Timing Diagram

Read Timing



* When the INTR pin is active low.

Write Timing

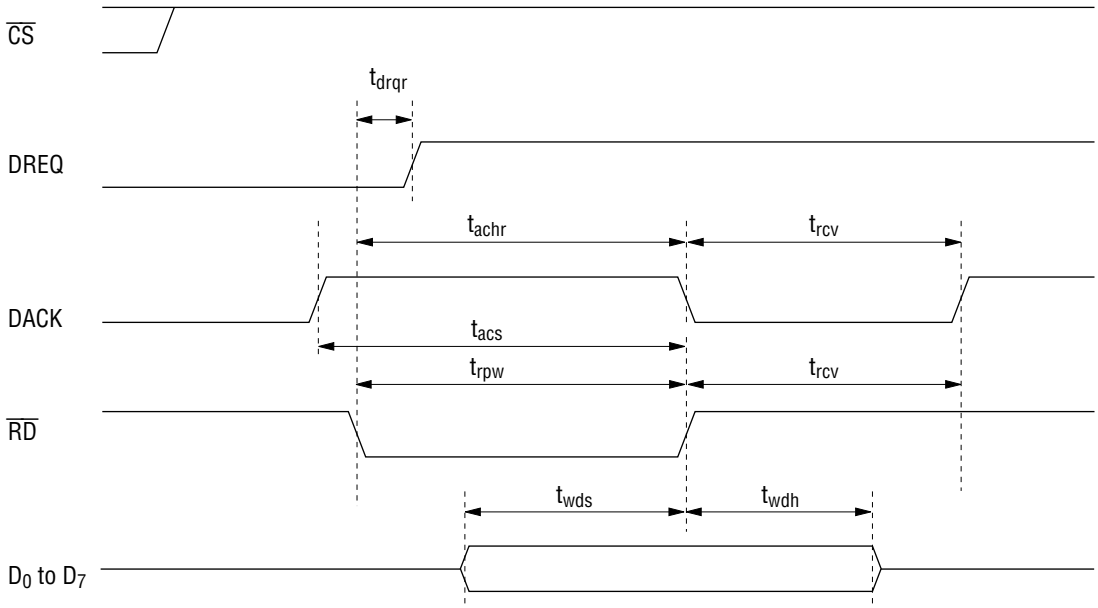


* When the INTR pin is active low.

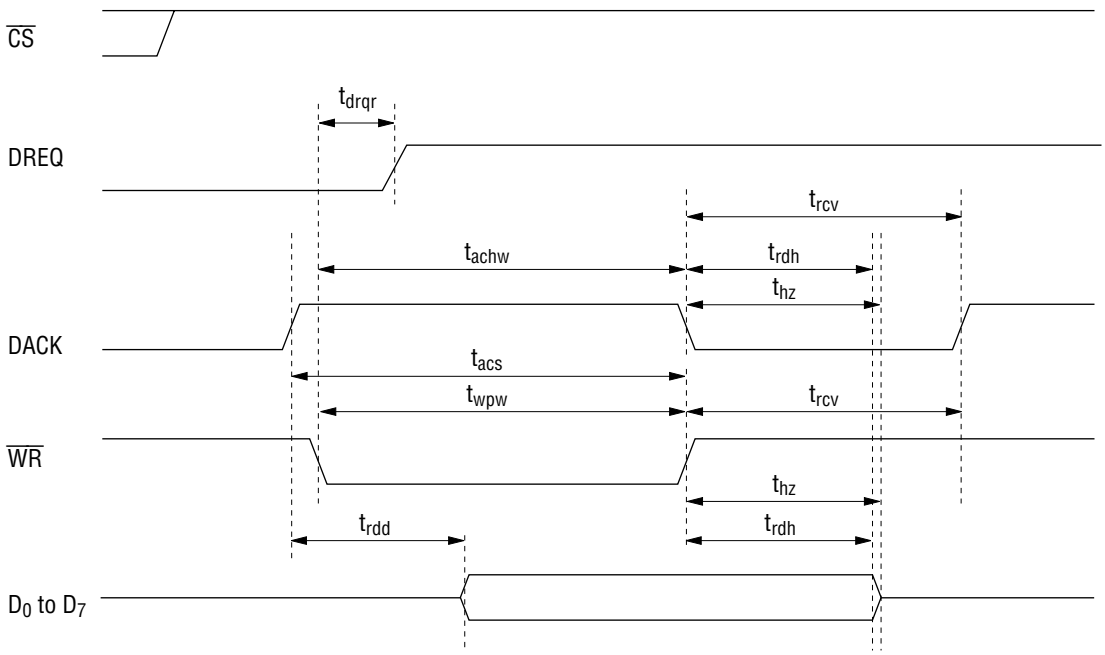
DMAC Access Timing 1

DMA_EN = "1", DMA_SL_1 = "0", DMA_SL_0 = "0", DREQ: active low, DACK: active high

Memory→M9405



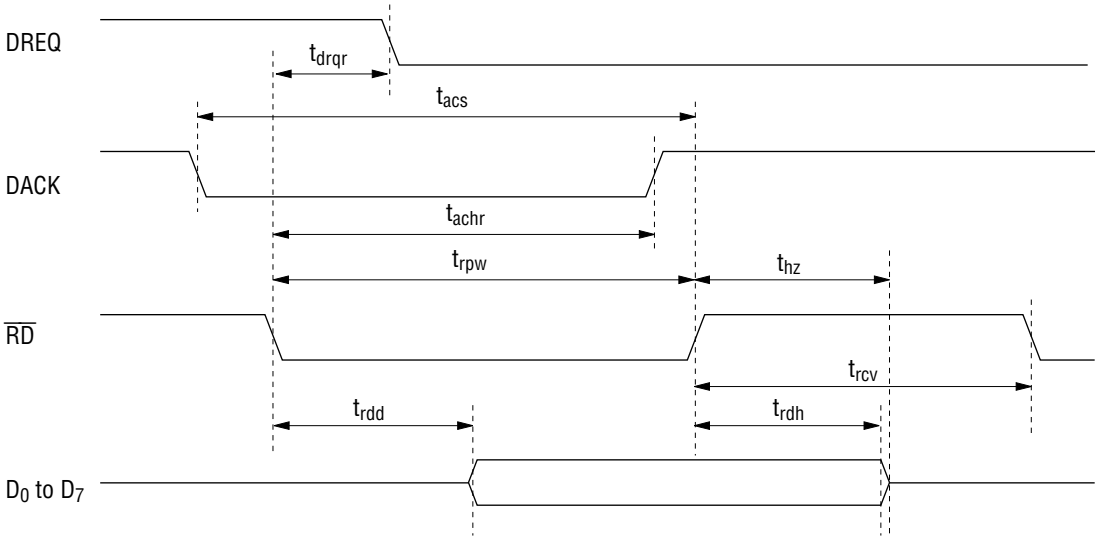
M9405→Memory



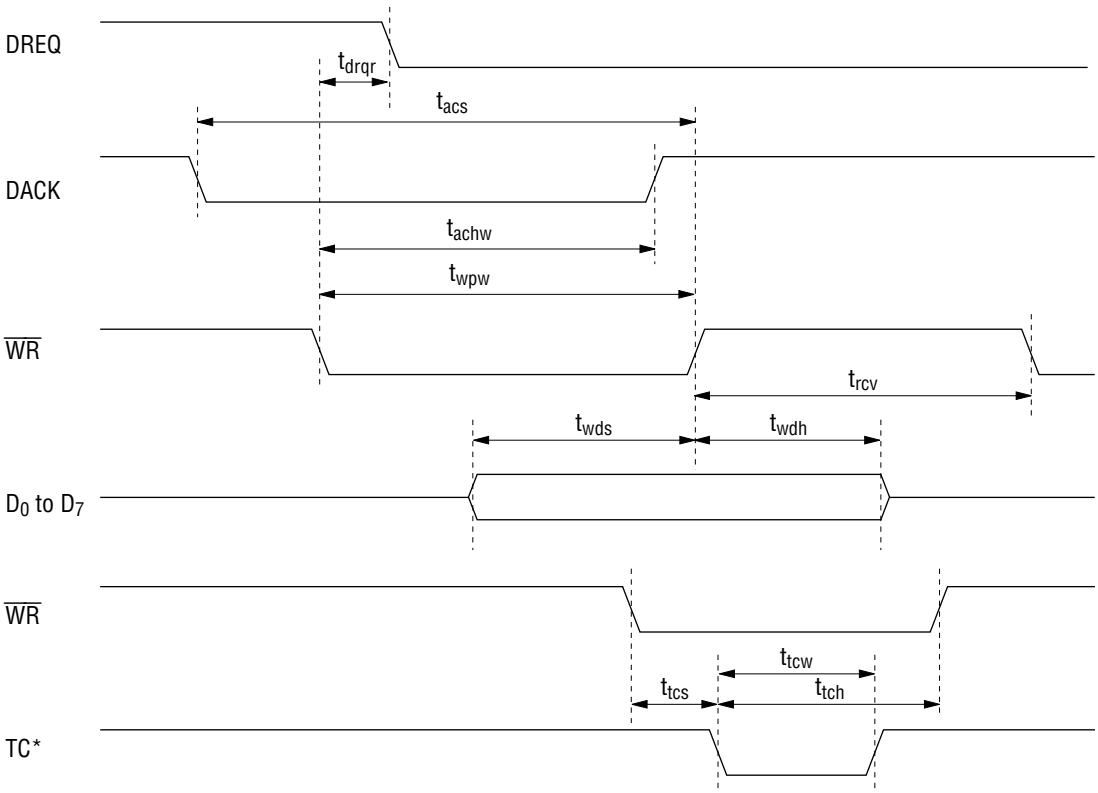
DMAC Access Timing 2

DMA_EN = "1", DMA_SL$_1$ = "0", DMA_SL$_0$ = "1", DREQ: active low, DACK: active high

M9405→Memory



Memory→M9405

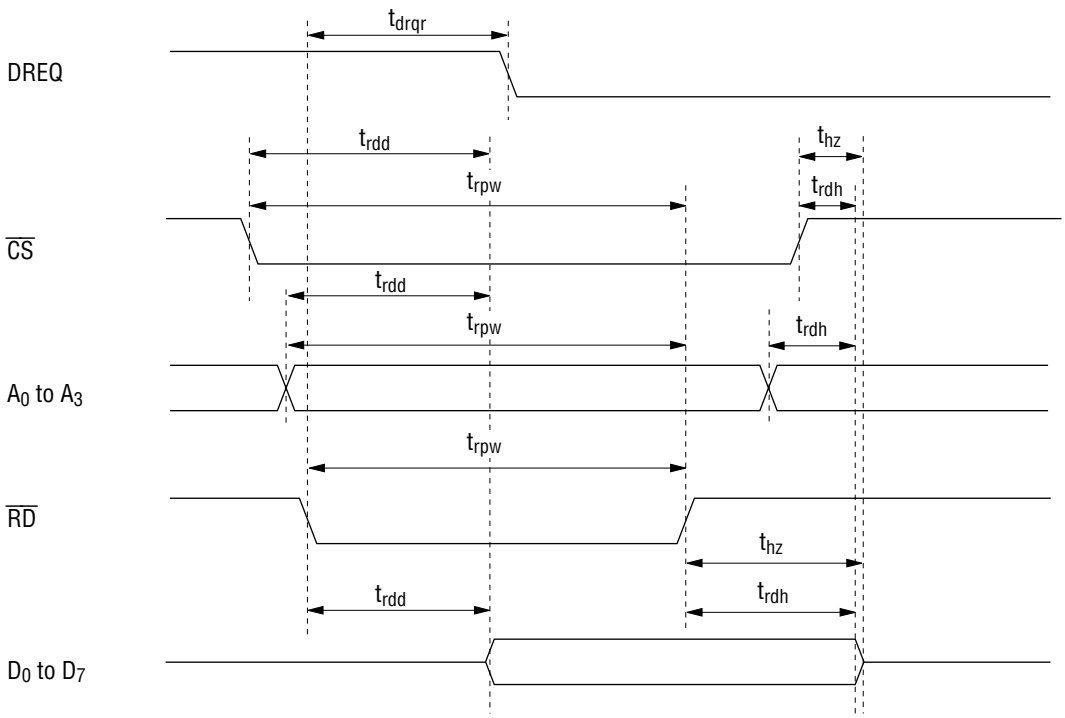


* When the TC pin is active low.

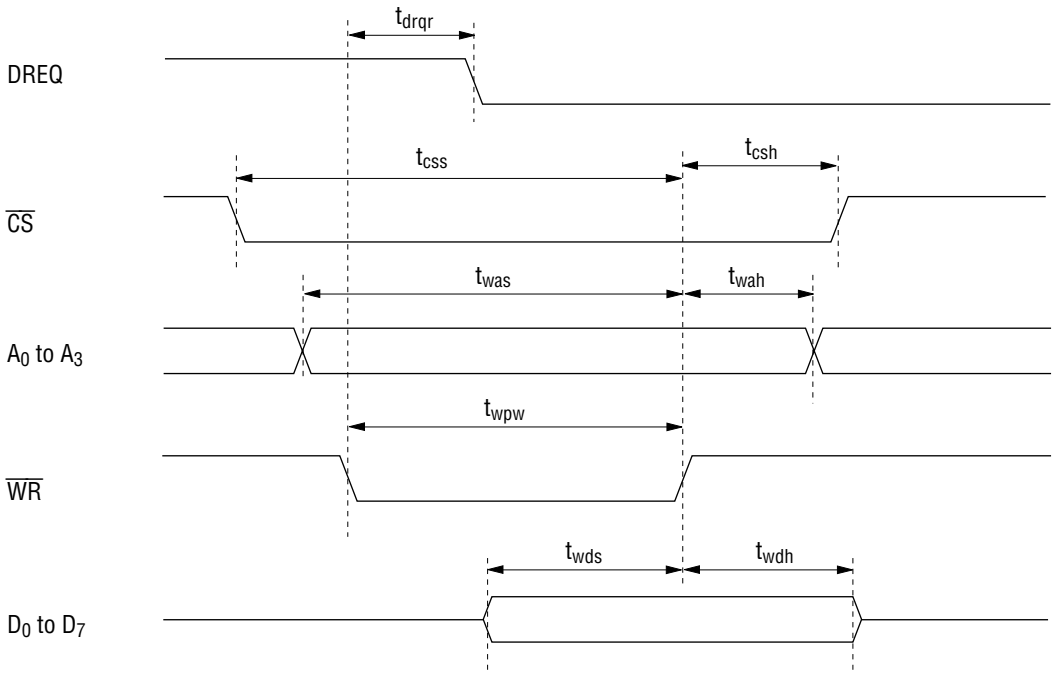
DMAC Access Timing 3

DMA_EN = "1", DMA_SL$_1$ = "1", DMA_SL$_0$ = "1" or "0", DREQ: active high

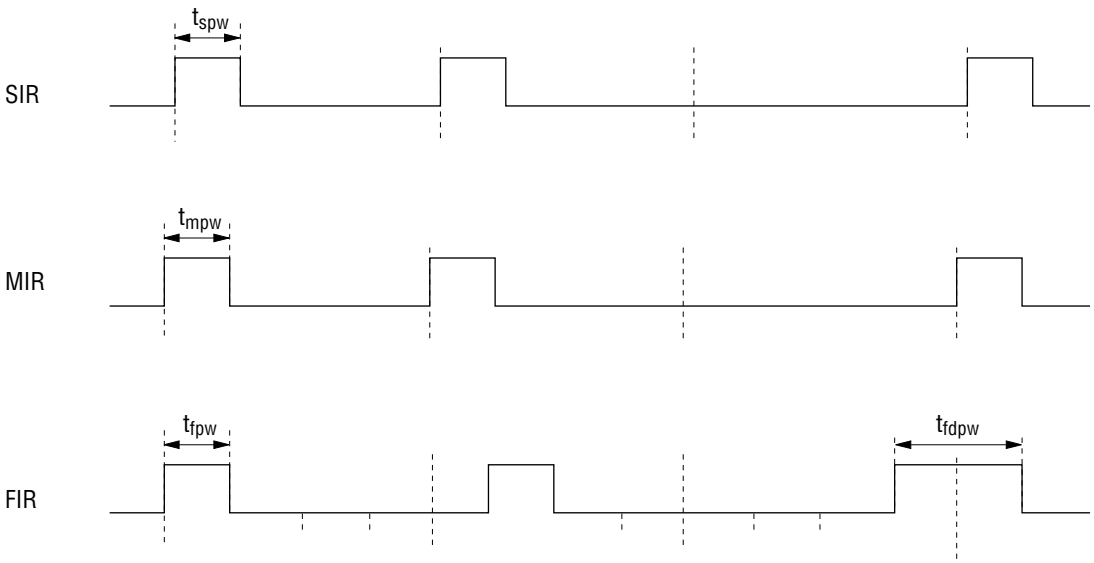
M9405→Memory



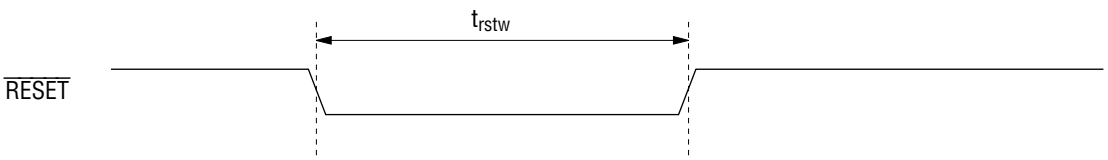
Memory→M9405



Infrared Interface Timing



Reset Timing



Appendix D

Register Table

Appendix D Register Table

Register Table

Add	Register name	Mode	R/W	Function of each bit							
				Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	TDR/RDR	all	R/W	TDR_7 /RDR_7	TDR_6 /RDR_6	TDR_5 /RDR_5	TDR_4 /RDR_4	TDR_3 /RDR_3	TDR_2 /RDR_2	TDR_1 /RDR_1	TDR_0 /RDR_0
1	ENR	SIR	R/W	TXE_IE	TXL_IE	RXH/T_IE	*	MLE_IE	*	OE_IE	FE_IE
		Ex-SIR					EOF_IE		CE_IE		*
		MIR									*
		FIR									
2	EIR	SIR	R	TXE_EV	TXL_EV	RXH/T_EV	*	MLE_EV	*	OE_EV	FE_EV
		Ex-SIR					EOF_EV		CE_EV		*
		MIR									*
		FIR									
3	LSR	all	R	FLV_5	FLV_4	FLV_3	FLV_2	FLV_1	FLV_0	IR_DET	TOUT
4	ICR1	SIR	R/W	MS_EN	TCC_EN	*	FCLR	*	*	RX_EN	TX_EN
		Ex-SIR				CRC_INV		IR_PLS	S_EOT		
		MIR									
		FIR									
5	ICR2	SIR	R/W	CTEST	SD_INV	IRIN_SL	RXINV	*	*	*	*
		Ex-SIR						SBF_3	SBF_2	SBF_1	SBF_0
		MIR						MBF_3	MBF_2	MBF_1	MBF_0
		FIR						*	*	*	*
6	MSR	all	R/W	DRS_2	DRS_1	DRS_0	XT_SL	*	*	$IRSL_1$	$IRSL_0$
7	DSR	all	R/W	DREQ_INV	DACK_INV	TC_INV	DMATH1	DMATH0	DMA_SL_1	DMA_SL_0	DMA_EN
8	FCR	all	R/W	$RXTH_3$	$RXTH_2$	$RXTH_1$	$RXTH_0$	$TXTH_3$	$TXTH_2$	$TXTH_1$	$TXTH_0$
9	TFL (L)	all	R/W	TFL_7	TFL_6	TFL_5	TFL_4	TFL_3	TFL_2	TFL_1	TFL_0
	TCC (L)	all	R	TCC_7	TCC_6	TCC_5	TCC_4	TCC_3	TCC_2	TCC_1	TCC_0
A	TFL (H)	all	R/W	*	*	*	*	TFL_{11}	TFL_{10}	TFL_9	TFL_8
	TCC (H)	all	R	*	*	*	*	TCC_{11}	TCC_{10}	TCC_9	TCC_8
B	MDS (L)	all	R/W	MDS_7	MDS_6	MDS_5	MDS_4	MDS_3	MDS_2	MDS_1	MDS_0
	RST (L)	all	R	RST_7	RST_6	RST_5	RST_4	RST_3	RST_2	RST_1	RST_0
C	MDS (H)	all	R/W	*	*	*	*	MDS_{11}	MDS_{10}	MDS_9	MDS_8
	RST (H)	all	R	*	*	*	*	RST_{11}	RST_{10}	RST_9	RST_8
D	ISR	all	R/W	*	*	*	*	*	*	*	INTR_INV
F	TEST	all	R/W	$TEST_7$	$TEST_6$	$TEST_5$	$TEST_4$	$TEST_3$	$TEST_2$	$TEST_1$	$TEST_0$

* Reserved

Registers

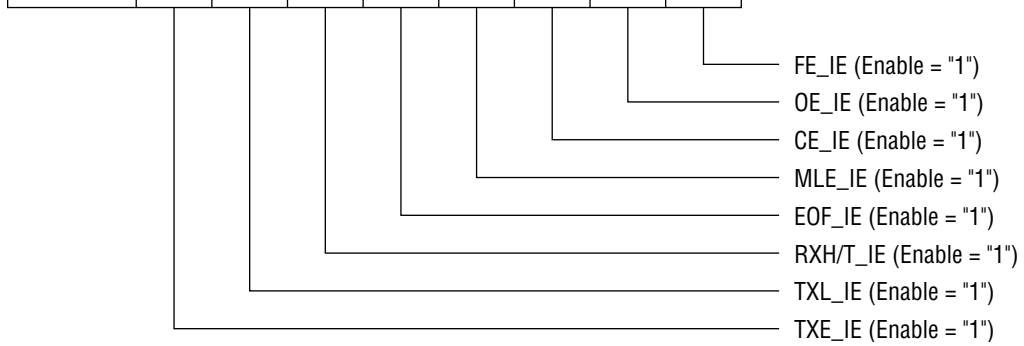
1. TDR: Transmitter Data Register (Write Only)
RDR: Receiver Data Register (Read Only) (Address = 0h)

The TDR (Transmitter Data Register) and RDR (Receiver Data Register) are used to read/write data directly upon receiving/transmitting the data. The TDR and RDR share the same address. When data is written in the transmit mode or during the idle mode, the TDR works as the top of the FIFO and 1-byte data can be written to the FIFO. When data is read in the receive mode, the RDR works as the bottom of the FIFO and 1-byte data in the FIFO can be read. Serial-to-parallel conversion is performed by the RSR. Parallel-to-serial conversion is performed by the TSR. Reading from the TDR or writing to the RDR is invalid. The contents of the FIFO and TDR/RDR are cleard by writing "1" to FCLR in the ICR1 register. The TSR and RSR cannot be cleared.

2. ENR: Enable Register (Address = 1h)

The ENR (Enable Register) is used to control enabling/disabling various interrupts on the MSM9405. Each of eight bits corresponds to each of eight interrupts provided on the MSM9405. Each of eight interrupts can be independently controlled by each bit. When the system is reset, all bits of ENR are reset to "0". By writing "1" to the bit corresponding to the desired interrupt, the specified interrupt is enabled.

	ENR 7	ENR 6	ENR 5	ENR 4	ENR 3	ENR 2	ENR 1	ENR 0
Initial value after reset	0	0	0	0	0	0	0	0

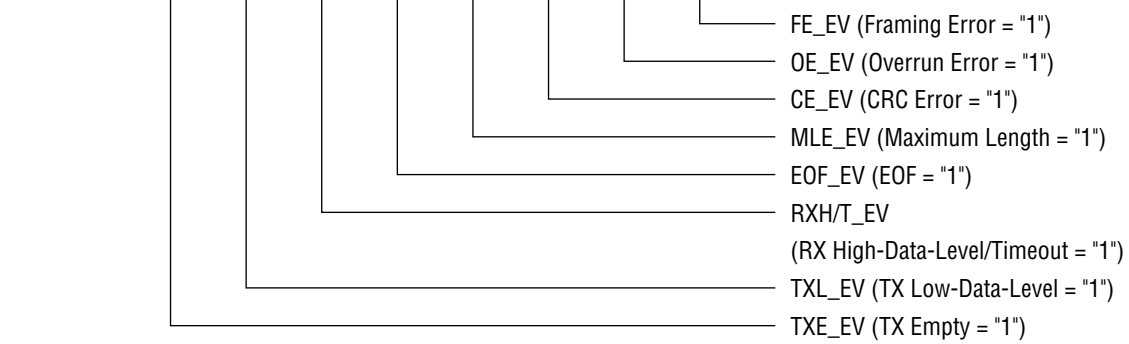


ENR bit	Table bit
ENR[0]	FE_IE (Framing Error Interrupt Enable): This bit enables or disables interrupt when an FE (Framing Error: Stop bit not detected) has occurred. This bit is valid in SIR mode and Ex-SIR mode. In MIR mode and FIR mode, this bit must be set to "0" (disable).
ENR[1]	OE_IE (Overrun Error Interrupt Enable) : This bit enables or disables interrupt when an OE (Overrun error : Error that occurs when the FIFO is full upon receiving and the next character is completely received by the RSR) has occurred.
ENR[2]	CE_IE (CRC Error Interrupt Enable) : This bit enables or disables interrupt when a CE (CRC Error) has occurred. This bit is valid in Extended-SIR mode, MIR mode, and FIR mode. In SIR mode, this bit must be set to "0" (disable).
ENR[3]	MLE_IE (Maximum Length Error Interrupt Enable) : This bit enables or disables interrupt when an MLE (Maximum Length Error: Error that occurs when a frame exceeding the maximum data size set by the MDS is received) has occurred. In Extended-SIR mode, MIR mode and FIR mode, this bit is valid. In SIR mode, this bit must be set to "0" (disable).
ENR[4]	EOF_IE (End Of Frame Interrupt Enable) : This bit enables or disables interrupt when the last byte in the frame's data field has been detected in Extended-SIR mode, MIR mode, and FIR mode. In Extended-SIR mode, MIR mode and FIR mode, this bit is valid. In SIR mode, this bit must be set to "0" (disable).
ENR[5]	RXH/T_IE (Receiver High-Data-Level/Timeout Interrupt Enable) : This bit enables or disables interrupt when the received data is at or above the receiving threshold level or time-out has occurred.
ENR[6]	TXL_IE (Transmitter Low-Data-Level Interrupt Enable) : This bit enables or disables interrupt when the sent data is below the sending threshold level.
ENR[7]	TXE_IE (Transmitter Empty Interrupt Enable) : This bit enables or disables interrupt when all of the data written in the FIFO has been transmitted and both the FIFO and the TSR have become empty.

3. EIR: Event Identification Register (Read Only) (Address = 2h)

The EIR (Event Identification Register) indicates factors of various interrupts on the MSM9405. Each of eight bits corresponds to each interrupt bit assignment set on the ENR. The EIR works as the status register even if the interrupt is disabled. When an event occurs, each corresponding bit is set to "1". When the system is reset, each bit of EIR is set to the initial value.

	EIR 7	EIR 6	EIR 5	EIR 4	EIR 3	EIR 2	EIR 1	EIR 0
Initial value after reset	0	1	0	0	0	0	0	0

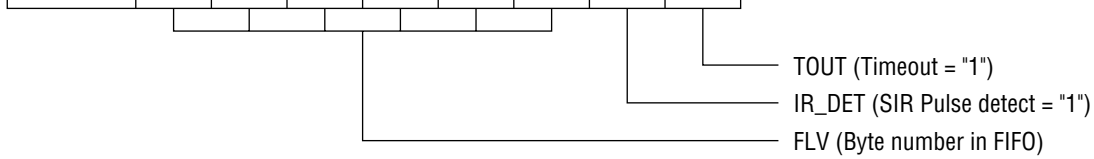


EIR bit	Description
EIR[0]	FE_EV (Framing Error Event): This bit is set to "1" when FE occurs. When the CPU reads the EIR, this bit is set to "0". In SIR mode and Ex-SIR mode, this bit is valid. This bit is not used in MIR mode and FIR mode.
EIR[1]	OE_EV (Overrun Error Event): When OE occurs, this bit is set to "1". When the CPU reads the EIR contents, OE_EV is set to "0". Data in RSR is not transfered to FIFO when OE_EV occurs and overwritten by the next receive data.
EIR[2]	CE_EV (CRC Error Event): When a CRC error occurs, this bit is set to "1". When the CPU reads the EIR, this bit is set to "0". In Extended-SIR mode, MIR mode and FIR mode, this bit is valid. This bit is not used in SIR mode.
EIR[3]	MLE_EV (Maximum Length Error Event): When MLE occurs, this bit is set to "1". When the CPU reads the EIR, this bit is set to "0". In Extended-SIR mode, MIR mode and FIR mode, this bit is valid. This bit is not used in SIR mode.
EIR[4]	EOF_EV (End Of Frame Event): This bit is valid in either Extended-SIR, MIR, or FIR mode. When the last byte in the frame's data field reaches the bottom of the FIFO in receiving mode, EOF_EV is set to "1". When the CPU reads the EIR, this bit is set to "0". In Extended-SIR mode, MIR mode and FIR mode, this bit is valid. In SIR mode, this bit is not used.
EIR[5]	RXH/T_EV (Receiver High-Data-Level/Timeout Event): When received data in the FIFO is at or above the receiving threshold level or time-out occurs, RXH/T_EV is set to "1". The condition for setting RXH/T_EV to "0" depends on the following two cases : If received data in the FIFO is at or above the receiving threshold level : Received data is read. When received data in the FIFO is below the threshold level, this bit is set to "0". If time-out occurs : After received data in the FIFO is read, this bit is set to "0".
EIR[6]	TXL_EV (Transmitter Low-Data-Level Event): When sent data in the FIFO is below the sending threshold level, this bit is set to "1". When sent data is written and sent data in the FIFO is at or above the threshold level, this bit is set to "0".
EIR[7]	TXE_EV (Transmitter Empty Event): When all of the data written in the FIFO has been transmit and both the FIFO and TSR are empty, this bit is set to "1". When the CPU reads the EIR, this bit is set to "0".

4. LSR: Line Status Register (Read Only) (Address = 3h)

The LSR (Line Status Register) indicates various statuses of the MSM9405 that is running. When the system is reset, all bits of the LSR are set to "0". This register is for read only and cannot be written.

	LSR 7	LSR 6	LSR 5	LSR 4	LSR 3	LSR 2	LSR 1	LSR 0
Initial value after reset	0	0	0	0	0	0	0	0

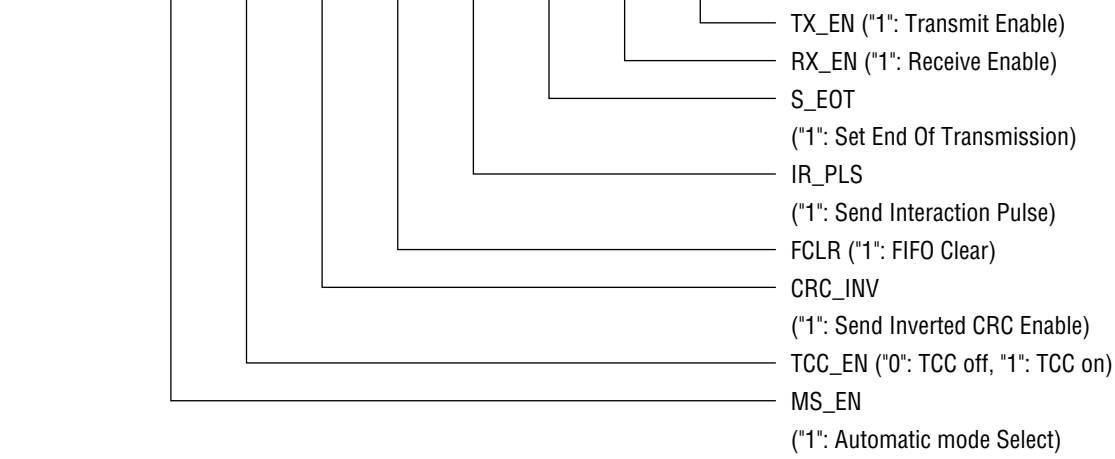


LSR bit	Description
LSR[0]	TOUT (FIFO Timeout): When time-out occurs, this bit is set to "1". When received data is read from the FIFO, TOUT is set to "0".
LSR[1]	IR_DET (SIR Pulse detect) : This bit is set to "1" when a pulse having a width of t_{spw} (SIR pulse width upon receiving) is detected. It is set to "0" when the CPU reads the LSR. This bit is valid in SIR mode and Ex-SIR mode, and is not used in MIR mode and FIR mode.
LSR[2-7]	FLV (FIFO Level): These bits indicate the number of data items in the FIFO with a value of 0 to 32. Bit 7 indicates the MSB and bit 2 indicates the LSB.

5. ICR1: Infrared Control Register 1 (Address = 4h)

The ICR1 (Infrared Control Register 1) is used to set various environments so that the MSM9405 can perform IrDA communication under proper conditions. When the system is reset, all bits of ICR1 are set to "0".

	ICR1 7	ICR1 6	ICR1 5	ICR1 4	ICR1 3	ICR1 2	ICR1 1	ICR1 0
Initial value after reset	0	0	0	0	0	0	0	0

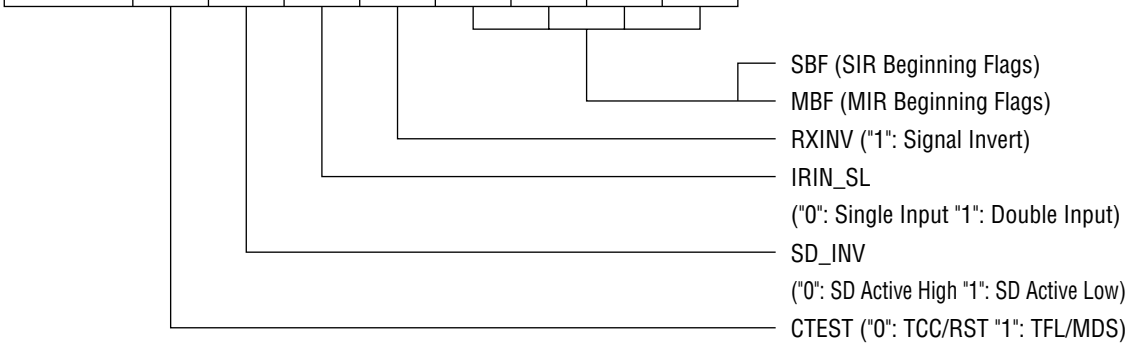


ICR1 bit	Description
ICR1[0]	TX_EN (Transmit Enable): When "1" is written to this bit, the device starts sending data that is in the FIFO. When "0" is written to this bit, sending terminates.
ICR1[1]	RX_EN (Receive Enable): When "1" is written to this bit, the device starts receiving data. When "0" is written to this bit, the device enters receive end mode.
ICR1[2]	S_EOT (Set End Of Transmission): When "1" is written to this bit, the data written to the FIFO next time is recognized as the end of frame, and immediately after it, the data added with CRC and EOF is sent as a frame. After a frame is sent, this bit is automatically set to "0". To use S_EOT, TFL must be set to the maximum value or TCC must be unused with TCC_EN = "0". This bit is not used in SIR mode. In Extended-SIR mode, MIR mode and FIR mode, this bit is valid. This bit is not used in SIR mode.
ICR1[3]	IR_PLS (Send Interaction Pulse): When "1" is written to this bit, an approximately 2-µs serial infrared interaction pulse is sent. The interaction pulse is sent immediately after the first STO sent after IR_PLS is set to "1". After a frame is sent, this bit is automatically set to "0". In MIR mode and FIR mode, this bit is valid. This bit is not used in SIR mode and Extended-SIR mode.
ICR1[4]	FCLR (FIFO Clear): When "1" is written to this bit, the FIFO (including the TDR and RDR) is made empty. The FIFO threshold level does not change. The TSR and RSR are not cleared. When the FIFO is made empty, this bit is automatically set to "0".
ICR1[5]	CRC_INV (Invert Transmitter CRC): When "1" is written to this bit, transmission is interrupted if TXE (Transmitter Empty) occurs during frame transmit. The inverted CRC and EOF are automatically added to the frame that caused TXE, then the frame is sent. Writing "0" to this bit disables this function. In MIR mode and FIR mode, this bit is valid. This bit is not used in SIR mode and Extended SIR mode.
ICR1[6]	TCC_EN (TCC Enable): When this bit is set to "1", the TCC is enabled. When TCC_EN is set to "0", the TCC is disabled. To use S_EOT, the TFL must be set to the maximum value or the TCC must be disabled with TCC_EN = "0". In Extended-SIR mode, MIR mode and FIR mode, this bit is valid. This bit is not used in SIR mode.
ICR1[7]	MS_EN (Mode Select Enable): When "1" is written to this bit, the MSM9405 performs the following operation depending on the mode. After the operation is completed, this bit is automatically set to "0". If the MSM9405 is in FIR mode: 1. The SD pin is set to "H"*, and the IROUT pin to "H". 2. Approximately 300 ns later, the SD pin is set to "L"*. 3. Approximately 300 ns later, the IROUT pin is set to "L". If the MSM9405 is in SIR, Extended-SIR, or MIR mode: 1. The SD pin is set to "H"*, and the IROUT pin to "L". 2. Approximately 300 ns later, the SD pin is set to "L"*. 3. The IROUT pin is held in the "L" level for approximately 300 ns. This bit is valid only when a 48 MHz crystal is used. Do not use this bit when an 18.432 MHz crystal is used. *: When the SD pin is active high. The level is reversed when the SD pin is active low.

6. ICR2: Infrared Control Register 2 (Address = 5h)

The ICR2 (Infrared Control Register 2) is used to set various environment so that the MSM9405 can perform IrDA communication under proper conditions. When the system is reset, all bits of ICR2 are set to "0".

	ICR2 7	ICR2 6	ICR2 5	ICR2 4	ICR2 3	ICR2 2	ICR2 1	ICR2 0
Initial value after reset	0	0	0	0	0	0	0	0

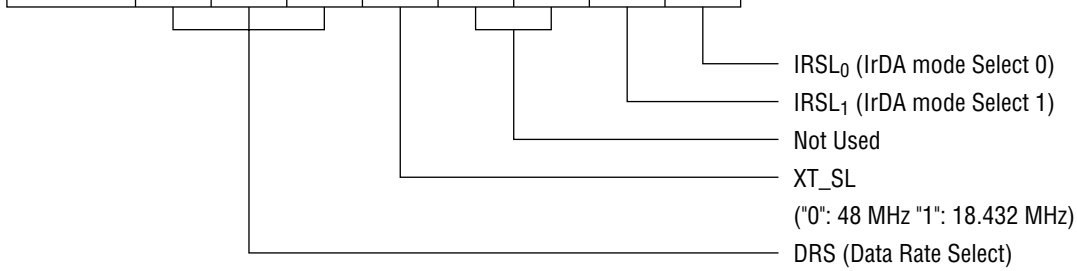


<table>
<tr><th>ICR2 bit</th><th>Description</th></tr>
<tr><td>ICR2[0-3]</td><td>These bits work as the SBF when Extended-SIR mode is selected, and as the MBF when the MIR mode is selected. This function is disabled in SIR mode and FIR mode.
SBF (SIR beginning Flags): These bits determine the number of BOFs to be added during sending in Extended-SIR mode as shown below.
MBF (MIR Beginning Flags): These bits determine the number of BOFs to be added during sending in MIR mode as shown below.
<table>
<tr><th>Encoding</th><th>SIR BOFs</th><th>MIR BOFs</th></tr>
<tr><td>0000</td><td>1</td><td>2</td></tr>
<tr><td>0001</td><td>2</td><td>3</td></tr>
<tr><td>0010</td><td>3</td><td>4</td></tr>
<tr><td>0011</td><td>4</td><td>5</td></tr>
<tr><td>0100</td><td>5</td><td>8</td></tr>
<tr><td>0101</td><td>7</td><td>12</td></tr>
<tr><td>0110</td><td>9</td><td>16</td></tr>
<tr><td>0111</td><td>13</td><td>24</td></tr>
<tr><td>1000</td><td>17</td><td>Reserved</td></tr>
<tr><td>1001</td><td>25</td><td>Reserved</td></tr>
<tr><td>1010</td><td>49</td><td>Reserved</td></tr>
<tr><td>1011</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>1100</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>1101</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>1110</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>1111</td><td>Reserved</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>ICR2[4]</td><td>RXINV (IRIN Signal Invert): This bit is used to select active low or active high of the receive signal.
RXINV = "0": Active low
RXINV = "1": Active high</td></tr>
<tr><td>ICR2[5]</td><td>IRIN_SL (IRIN Select): This bit determines how the receive signal input pin is used.
IRIN_SL = "0": Only the input from the IRIN-A pin (2.4 kbps to 4 Mbps) is accepted.
IRIN_SL = "1": An input from IRIN-A or IRIN-B is automatically selected depending on the transfer rate. (A: 2.4 to 115.2 kbps, B: 0.576 to 4 Mbps)</td></tr>
<tr><td>ICR2[6]</td><td>SD_INV (SD Signal Invert): This bit changes the polarity (active high/low) of the SD pin output on the MSM9405.
SD_INV = "0": Active high
SD_INV = "1": Active low</td></tr>
<tr><td>ICR2[7]</td><td>CTEST (Counter Test): Normally this bit is set to "0". When TFL/TCC and MDS/RST are read after "1" is written to this bit, the TFL and MDS values can be obtained. The values of TCC and RST can be obtained by reading TFL/TCC and MDS/RST when CTEST is "0".</td></tr>
</table>

7. MSR: Mode Select Register (Address = 6h)

The MSR is used to select various modes of the MSM9405. When the system is reset, each bit of MSR is set to the initial value.

	MSR 7	MSR 6	MSR 5	MSR 4	MSR 3	MSR 2	MSR 1	MSR 0
Initial value after reset	0	0	1	0	0	0	0	0

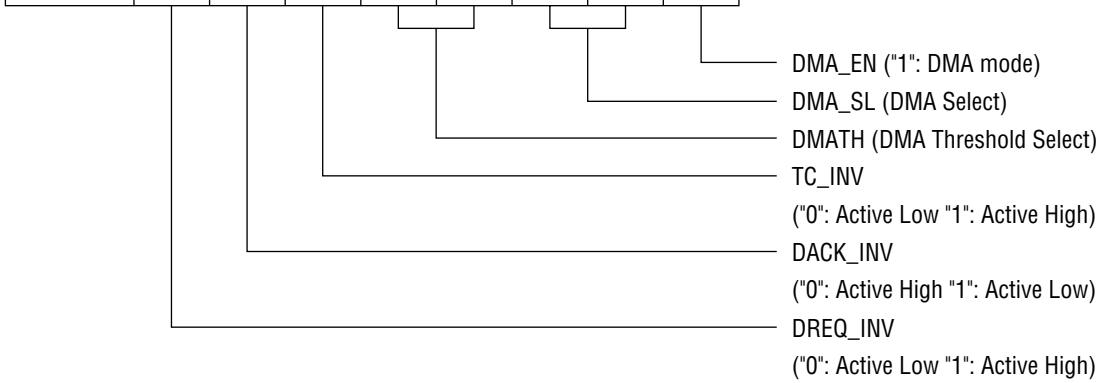


MSR Bit	Description
MSR[0-1]	IRSL (Infrared Mode Select): These bits are used to select the transfer mode as shown below. $IRSL_1$ / $IRSL_0$ / mode: 0 0 SIR; 0 1 Extended-SIR; 1 0 MIR; 1 1 FIR
MSR[2-3]	These bits are not used.
MSR[4]	XT_SL (Crystal Select): This bit determines the crystal to be used. XT_SL = "0": 48 MHz crystal is used XT_SL = "1": 18.432 MHz crystal is used
MSR[5-7]	DRS (Data Rate Select): These bits determine the transfer rate as shown below. Encoding / SIR Data Rate / MIR Data Rate / FIR Data Rate: 000 2400 bps 0.576 Mbps Reserved 001 9600 bps 1.152 Mbps 4 Mbps 010 19.2 kbps Reserved Reserved 011 38.4 kbps Reserved Reserved 100 57.6 kbps Reserved Reserved 101 115.2 kbps Reserved Reserved 110 Reserved Reserved Reserved 111 Reserved Reserved Reserved

8. DSR: DMA Mode Select Register (Address = 7h)

The DSR (DMA Mode Select Register) is used to select the DMA mode for the MSM9405. When the system is reset, all bits of DSR are set to "0".

	DSR 7	DSR 6	DSR 5	DSR 4	DSR 3	DSR 2	DSR 1	DSR 0
Initial value after reset	0	0	0	0	0	0	0	0

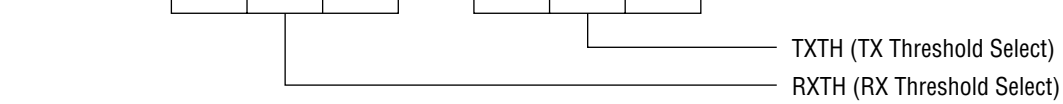


<table>
<tr><th>DSR Bit</th><th>Description</th></tr>
<tr><td>DSR[0]</td><td>DMA_EN (DMA Mode Enable): This bit determines whether the DMA is to be used.
When "1" is written to this bit, DSR[1-2] (DMA_SL0, DMA_SL1) setting is enabled and the MSM9405 enters the DMA transfer standby mode.
If DMA_EN = "0", DSR[1-2] (DMA_SL0, DMA_SL1) setting is disabled and DMA transfer is not performed.</td></tr>
<tr><td>DSR[1-2]</td><td>DMA_SL (DMA Select): These bits are used to select the method of interfacing with DMAC.
<table>
<tr><th>DMA_SL1</th><th>DMA_SL0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Supports the DMA transfer in Single Address mode. When the $\overline{RD}$ signal becomes active while DACK is active, the DMA read cycle (Memory→M9405) is selected. When the $\overline{WR}$ signal becomes active while DACK is active, the DMA write cycle (M9405→Memory) is selected. While DACK is being asserted, address "0" (TDR/RDR) is accessed regardless of the status of A_0 to A_3.</td></tr>
<tr><td>0</td><td>1</td><td>Supports the DMA transfer in Single Address mode. When the $\overline{WR}$ signal becomes active while DACK is active, the DMA read cycle (Memory→M9405) is selected. When the $\overline{RD}$ signal becomes active while DACK is active, the DMA write cycle (M9405→Memory) is selected. While DACK is being asserted, address "0" (TDR/RDR) is accessed regardless of the status of A_0 to A_3.</td></tr>
<tr><td>1</td><td>0</td><td>Supports the DMA transfer in Dual Address mode. Access TDR/RDR via $\overline{CS}$ and A_0 to A_3.</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>DSR[3-4]</td><td>DMATH (DMA Threshold Select): These bits determine the threshold level to release the DREQ. The DREQ signal is deasserted when the number of data bytes reaches the following values.
<table>
<tr><th>DMATH1</th><th>DMATH0</th><th>During transmission</th><th>During reception</th></tr>
<tr><td>0</td><td>0</td><td>32</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>30</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>28</td><td>4</td></tr>
<tr><td>1</td><td>1</td><td>24</td><td>8</td></tr>
</table></td></tr>
<tr><td>DSR[5]</td><td>TC_INV (TC Signal Invert): This bit selects the polarity of the TC signal.
TC_INV = "0": Active low
TC_INV = "1": Active high</td></tr>
<tr><td>DSR[6]</td><td>DACK_INV (DACK Signal Invert): This bit selects the polarity of the DACK signal.
DACK_INV = "0": Active high
DACK_INV = "1": Active low</td></tr>
<tr><td>DSR[7]</td><td>DREQ_INV (DREQ Signal Invert): This bit selects the polarity of the DREQ signal.
DREQ_INV = "0": Active low
DREQ_INV = "1": Active high</td></tr>
</table>

9. FCR: FIFO Control Register (Address = 8h)

The FCR (FIFO Control Register) is used to set the threshold level of the FIFO to be used by the MSM9405 upon sending/receiving. The FCR setting is applied to both interrupt and DMA. When the system is reset, each bit of the FCR is set to 0.

	FCR 7	FCR 6	FCR 5	FCR 4	FCR 3	FCR 2	FCR 1	FCR 0
Initial value after reset	0	1	1	1	0	1	1	1



<table>
<tr><th>FCR bit</th><th>Description</th></tr>
<tr><td>FCR[0-3]</td><td>TXTH (Transmit Threshold Select): These four bits set the following 16 sending threshold levels.
<table>
<tr><th>FCR (0-3)</th><th>TX Threshold Level (Byte)</th></tr>
<tr><td>0000</td><td>Reserved</td></tr>
<tr><td>0001</td><td>02</td></tr>
<tr><td>0010</td><td>04</td></tr>
<tr><td>0011</td><td>06</td></tr>
<tr><td>0100</td><td>08</td></tr>
<tr><td>0101</td><td>10</td></tr>
<tr><td>0110</td><td>12</td></tr>
<tr><td>0111</td><td>14</td></tr>
<tr><td>1000</td><td>16</td></tr>
<tr><td>1001</td><td>18</td></tr>
<tr><td>1010</td><td>20</td></tr>
<tr><td>1011</td><td>22</td></tr>
<tr><td>1100</td><td>24</td></tr>
<tr><td>1101</td><td>26</td></tr>
<tr><td>1110</td><td>28</td></tr>
<tr><td>1111</td><td>30</td></tr>
</table></td></tr>
<tr><td>FCR[4-7]</td><td>RXTH (Receive Threshold Select): These four bits set the following 16 receiving threshold levels.
<table>
<tr><th>FCR (4-7)</th><th>RX Threshold Level (Byte)</th></tr>
<tr><td>0000</td><td>Reserved</td></tr>
<tr><td>0001</td><td>02</td></tr>
<tr><td>0010</td><td>04</td></tr>
<tr><td>0011</td><td>06</td></tr>
<tr><td>0100</td><td>08</td></tr>
<tr><td>0101</td><td>10</td></tr>
<tr><td>0110</td><td>12</td></tr>
<tr><td>0111</td><td>14</td></tr>
<tr><td>1000</td><td>16</td></tr>
<tr><td>1001</td><td>18</td></tr>
<tr><td>1010</td><td>20</td></tr>
<tr><td>1011</td><td>22</td></tr>
<tr><td>1100</td><td>24</td></tr>
<tr><td>1101</td><td>26</td></tr>
<tr><td>1110</td><td>28</td></tr>
<tr><td>1111</td><td>30</td></tr>
</table></td></tr>
</table>

10. TFL: Transmitter Frame Length Register
TCC: Transmitter Current-Count Register (Address = 9, Ah)

The TFL (Transmitter Frame Length Register) and TCC (Transmitter Current-Count Register) are used to specify the length of the frame to be transferred for transmitting. The TFL and TCC shares the same address. Bits 0 to 7 of address 9h and bits 0 to 3 of address Ah (totally 12 bits) are used. Bit 0 of address 9h is the LSB.
When the TFL/TCC value is read, the CTEST setting is reflected. If CTEST = "0", the TCC contents can be read. If CTEST = "1", the TFL contents can be read. When the TFL/TCC is written, the TFL value is rewritten. The TCC cannot be written.
To use the TFL/TCC, write "1" to TCC_EN, and set the frame length in the TFL. The frame length to be set does not include the CE, FCS, BOF, and EOF. When "1" is written to TX_EN, the TFL value that has been set as the frame length is loaded to the TCC. When sending is started, the TCC value is decremented by 1 each time 1 byte is sent. When the TCC value becomes "0", the end of frame is assumed and the frame is automatically added with the CRC and EOF and sent. After one frame is sent, the TFL value is loaded again into the TCC when the BOF of the second frame is sent.
The TFL/TCC initial value is set to 800h.

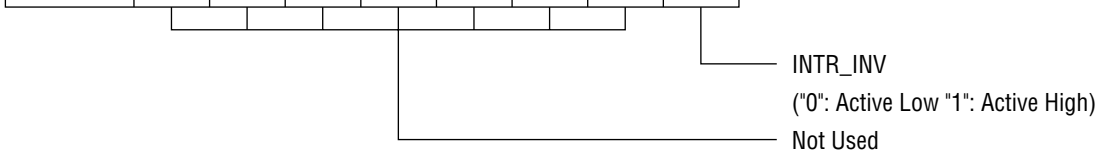
11. MDS: Maximum Data Size Register
RST: Receiver Frame Length Stack Register (Address = B, Ch)

The MDS (Maximum Data Size Register) is used to set the maximum data size. The RST (Receiver Frame Length Stack Register) is used to stack the received frame length. The MDS and RST share the same address. Bits 0 to 7 of address Bh and bits 0 to 3 of address Ch (totally 12 bits) are used. Bit 0 of address Bh is the LSB.
When the MDS/RST value is read, the CTEST setting is reflected. If CTEST = "0", the RST contents can be read. If CTEST = "1", the MDS contents can be read. When the MDS/RST is written, the MDS value is rewritten. The RST cannot be written.
To use the MDS, set the maximum data size in the MDS in advance. The frame length to be set does not include the CE, FCS, BOF, and EOF. When receiving is started, the RCC (Receiver Current-Counter) value is incremented by 1 each time one byte is received. If the RCC value exceeds the MDS value during receiving, MLE occurs. The MDS initial value is set to 800h.
When a frame is fully received and EOF_EV = "1", the received frame length counted by the internal counter is stacked in the RST. This value is stored until the next frame is fully received. The value stacked in the RST is maintained even if MSM9405 transmitting/receiving is switched. The RST initial value is set to 0h.

12. ISR: Interrupt Signal Control Register (Address = Dh)

The ISR (Interrupt Signal Control Register) is used to determine the polarity of the INTR signal. When the system is reset, each bit of ISR is set to 0.

	ISR 7	ISR 6	ISR 5	ISR 4	ISR 3	ISR 2	ISR 1	ISR 0
Initial value after reset	0	0	0	0	0	0	0	0



ISR bit	Description
ISR[0]	INTR_INV (DMA mode Enable): This bit selects the polarity of the INTR signal. INTR_INV = "0": Active Low INTR_INV = "1": Active High
ISR[1-7]	These bits are not used.

13. TEST: Test Register (Address = Fh)

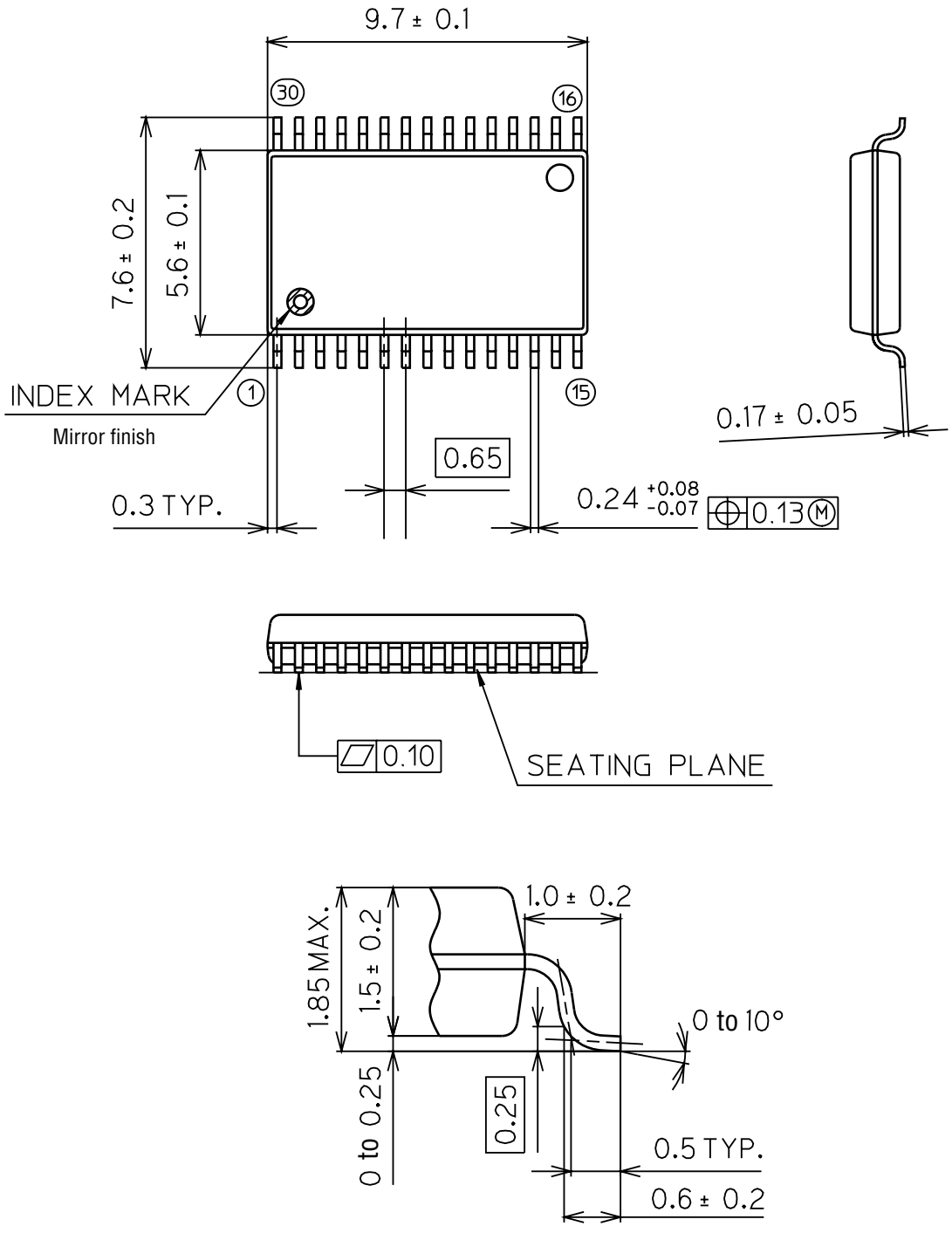
This register is used only for testing.

Appendix E

Package Outline and Dimensions

Appendix E Package Outline and Dimensions

(Unit : mm)



30-Pin Plastic SSOP

MSM9405

Application Manual

First Edition: January 1999
Second Edition: July 2000

FEAL9405-02