FEDL9810BDIGEST-02

OKI Semiconductor

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Previous version: Jun. 2000

MSM9810B

8-Channel Mixing OKI ADPCM Type Voice Synthesis LSI

This document contains minimum specifications. For full specifications, please contact your nearest Oki office or representative.

GENERAL DESCRIPTION

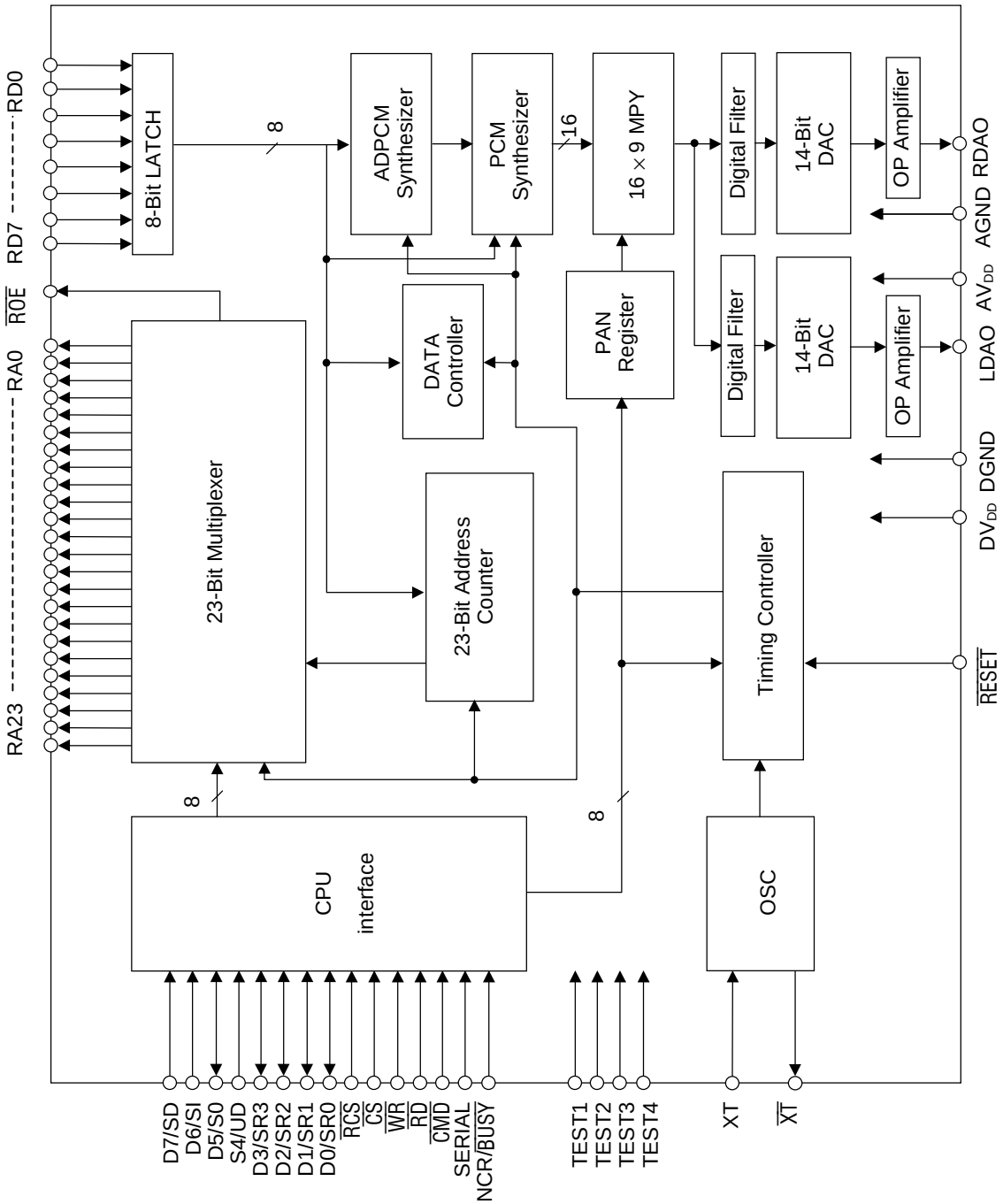
The MSM9810B is an 8-channel mixing voice synthesis LSI, to which up to 128 Mbits of ROM and/or EPROM storing voice data can directly be connected externally.
The device is straight 8-bit PCM playback, non-linear 8-bit PCM playback, 4-bit ADPCM playback, and 4-bit ADPCM2 playback selectable and provides 2-channel stereo output and volume control. The MSM9810B contains a 14-bit D/A converter and LPF.
The MSM9810B can easily configure a system by connecting voice data storage memory, power amplifier, and CPU externally.

FEATURES

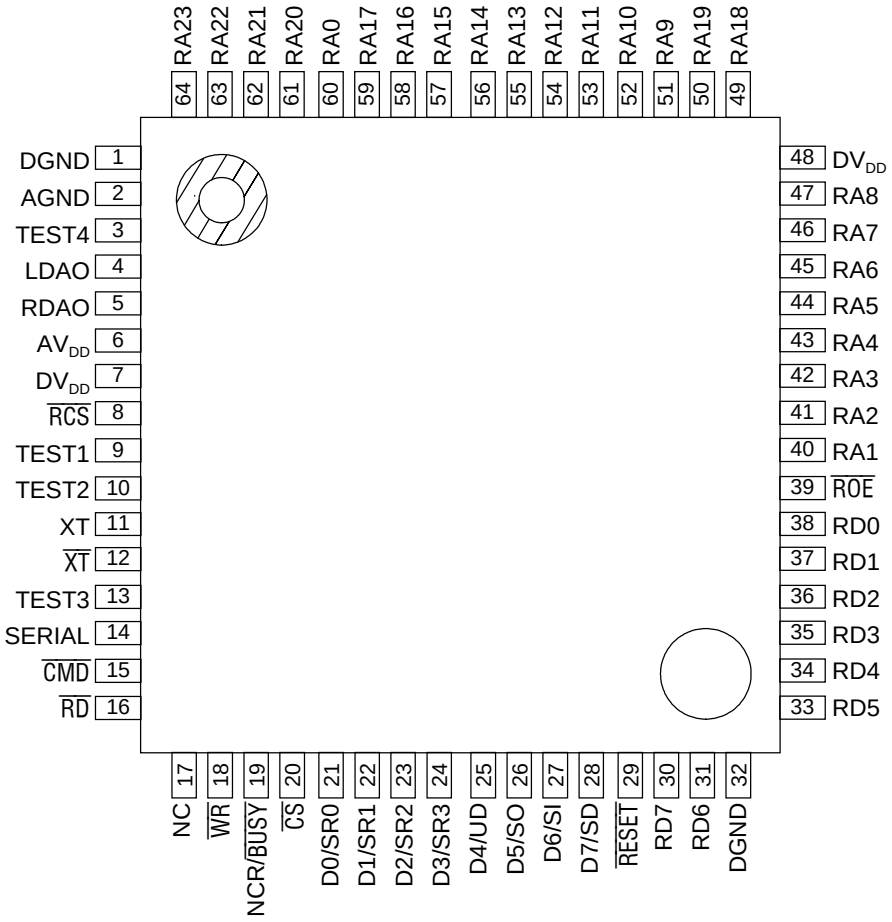
- Non-linear 8-bit PCM/straight 8-bit PCM/4-bit ADPCM/4-bit ADPCM2
- Serial input or parallel input selectable
- Phrase Control Table function
- 8-channel mixing function
- Master clock frequency : 4.096 MHz
- Sampling frequency : 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 21.2 kHz, 25.6 kHz, 32.0 kHz
- Maximum number of phrases : 256
- Output channel : L/R 2 channels
- Built-in volume control function (for each output channel)
- Built-in 14-bit D/A converter
- Built-in low-pass filter : Digital filter

64-pin plastic QFP (QFP64-P-1414-0.80-BK) (Product name: MSM9810BGS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No connection

64-pin Plastic QFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
40-47, 49-64	RA23-RA0	O	Address pins for external memory. These pins become high impedance when $\overline{RCS}$ pin is "H".
30, 31, 33-38	RD7-RD0	I	Data pin for external memory. Pull-down resistors are internally connected to these pins. These pull-down resistors become valid when the $\overline{RCS}$ pin is "H", and become invalid when the $\overline{RCS}$ pin is "L".
39	$\overline{ROE}$	O	Output enable pin for external memory.
8	$\overline{RCS}$	I	When this pin is "L", RA23 to RA0 and $\overline{ROE}$ pins output address data and output enable signal. When this pin is "H", RA23 to RA0 and $\overline{ROE}$ pins become high impedance.
15	$\overline{CMD}$	I	Select pin for Command data or Subcommand data for CPU interface. When this pin is "H", subcommand input is selected. When this pin is "L", command input is selected. A pull-up resistor is internally connected to this pin.
16	$\overline{RD}$	I	Read pin for CPU interface. A pull-up resistor is internally connected to this pin.
18	$\overline{WR}$	I	Write pin for CPU interface. A pull-up resistor is internally connected to this pin.
20	$\overline{CS}$	I	Chip select pin for CPU interface. When $\overline{CS}$ is "H", $\overline{WR}$/$\overline{RD}$ signal is not entered in this LSI. A pull-up resistor is internally connected to this pin.
14	SERIAL	I	CPU input interface select pin. When SERIAL is "H", serial input interface is selected. When it is "L", parallel input interface is selected.
28	D7/SD	I/O	Data bus pin for CPU interface when parallel input interface is selected. When $\overline{WR}$ is "L", this pin serves as data input pin. When $\overline{RD}$ is "L", this pin serves as channel status data output pin. When serial input interface is selected, this pin serves as serial data input pin.
27	D6/SI	I/O	Data bus pin for CPU interface when parallel input interface is selected. When $\overline{WR}$ is "L", this pin serves as data input pin. When $\overline{RD}$ is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as serial clock input pin.
26	D5/SO	I/O	Data bus pin for CPU interface when parallel input interface is selected. When $\overline{WR}$ is "L", this pin serves as data input pin. When $\overline{RD}$ is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as channel status serial output pin.

Pin	Symbol	Type	Description
25	D4/UD	I/O	Data bus pin for CPU interface when parallel input interface is selected. When $\overline{WR}$ is "L", this pin serves as data input pin. When $\overline{RD}$ is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as channel status select pin. When UD is "H", channels 8 thru 5 are output to SR3 thru SR0, respectively. When UD is "L", channels 4 thru 1 are output to SR3 thru SR0, respectively.
24	D3/SR3	I/O	Data bus pin for CPU interface when parallel input interface is selected. When $\overline{WR}$ is "L", this pin serves as data input pin. When $\overline{RD}$ is "L", this pin serves as channel status output pin. When serial input interface is selected, this pin serves as channel status output pin. When UD is "H", channels 8 thru 5 are output to SR3 thru SR0, respectively. When UD is "L", channels 4 thru 1 are output to SR3 thru SR0, respectively.
23	D2/SR2		
22	D1/SR1		
21	D0/SR0		
4	LDAO	O	LEFT side analog output pin.
5	RDAO	O	RIGHT side analog output pin.
11	XT	I	Crystal or ceramic oscillator connection pin. A feedback resistor of about 1MΩ is connected between XT and $\overline{XT}$. When external clocks are used, enter external clocks into this pin.
12	$\overline{XT}$	O	Crystal or ceramic oscillator connection pin. When external clocks are used, leave this pin open.
29	$\overline{RESET}$	I	When this pin is "L" level, the LSI is initialized. At that time, oscillation stops and D/A outputs go to GND level. A pull-up resistor is internally connected to this pin.
19	NCR/$\overline{BUSY}$	I	Channel status select pin. When this pin is "H", NCR signal is output. When it is "L", $\overline{BUSY}$ signal is output.
9	TEST1	I	Pins for LSI testing. Apply "L" level to these pins.
10	TEST2		
13	TEST3		
3	TEST4		
6	AV_{DD}	—	Analog power supply pin. A bypass capacitor of 01 μF or more should be connected between the AGND pin and the AV_{DD} pin.
7, 48	DV_{DD}	—	Digital power supply pin. A bypass capacitor of 0.1 μF or more should be connected between the DGND pin and the DV_{DD} pin.
2	AGND	—	Analog GND pin.
1, 32	DGND	—	Digital GND pin.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta= 25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}		–0.3 to V_{DD}+ 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power Supply Voltage	V_{DD}	—	4.5 to 5.5			V
Operating Temperature	T_{op}	—	–40 to +85			°C
Master Clock Frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

ELECTRICAL CHARACTERISTICS

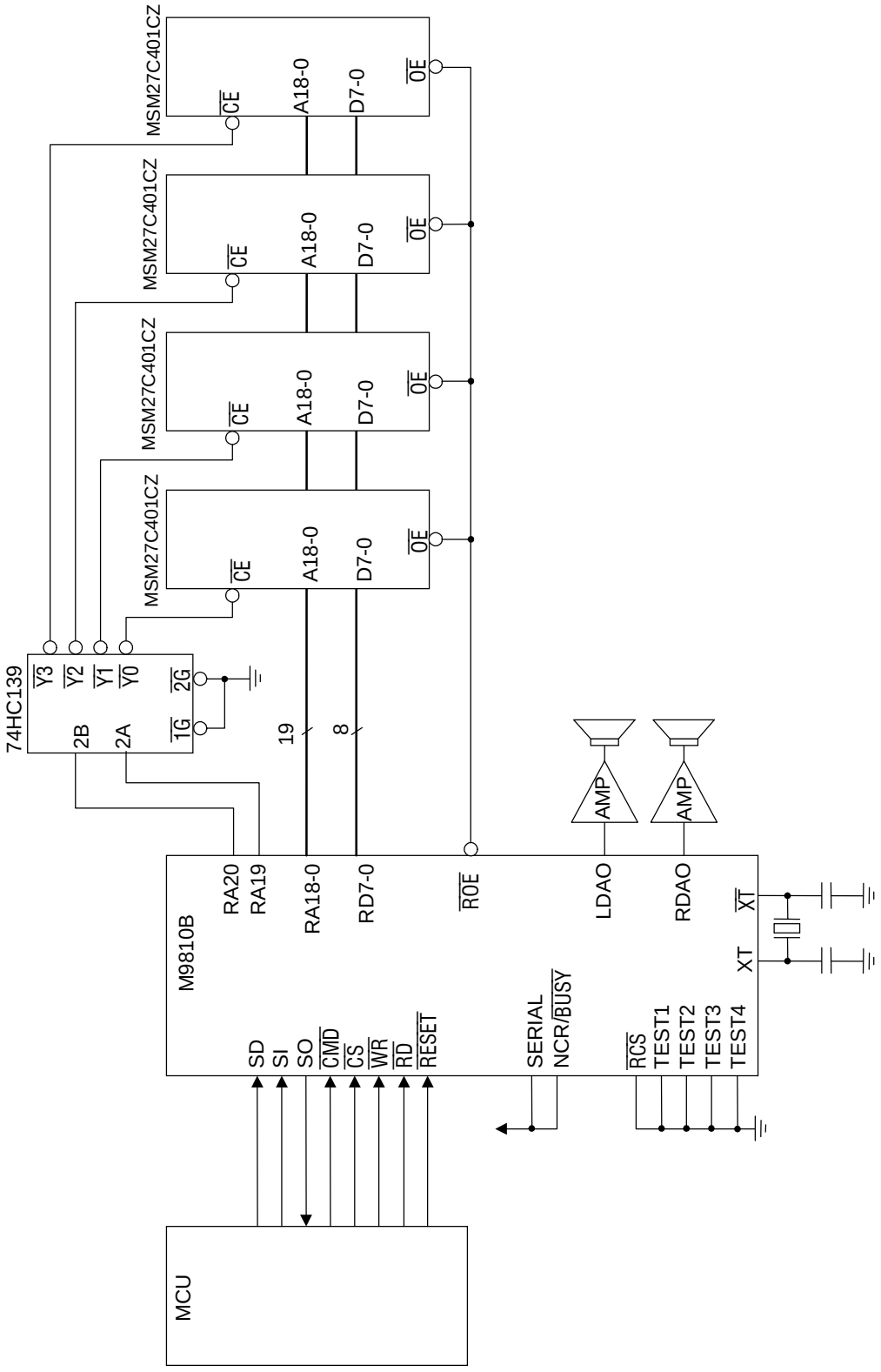
DC Characteristics

(DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level Input Voltage	V_{IH}	—	0.84 × V_{DD}	—	—	V
Low-level Input Voltage	V_{IL}	—	—	—	0.16 × V_{DD}	V
High-level Output Voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.4	—	—	V
Low-level Output Voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
High-level Input Current 1	I_{IH1}	V_{IH} = V_{DD}	—	—	10	µA
High-level Input Current 2 (Note 1)	I_{IH2}	Applied to pins with internal pull-down resistor	30	—	300	µA
Low-level Input Current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
Low-level Input Current 2 (Note 2)	I_{IL2}	Applied to pins with internal pull-up resistor	–300	—	–30	µA
Output Leakage Current	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}	–10	—	+10	µA
Operating Current	I_{DD}	f_{OSC} 4 MHz, no load	—	6	15	mA
Standby Current	I_{DS}	Ta = –40 to +70°C	—	—	15	µA
		Ta = +70 to +85°C	—	—	50	µA

Notes 1: Applicable to RD7 to RD0 pins (when $\overline{RCS}$ = "H").
2: Applicable to $\overline{CMD}$, $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ pins.

APPLICATION CIRCUITS

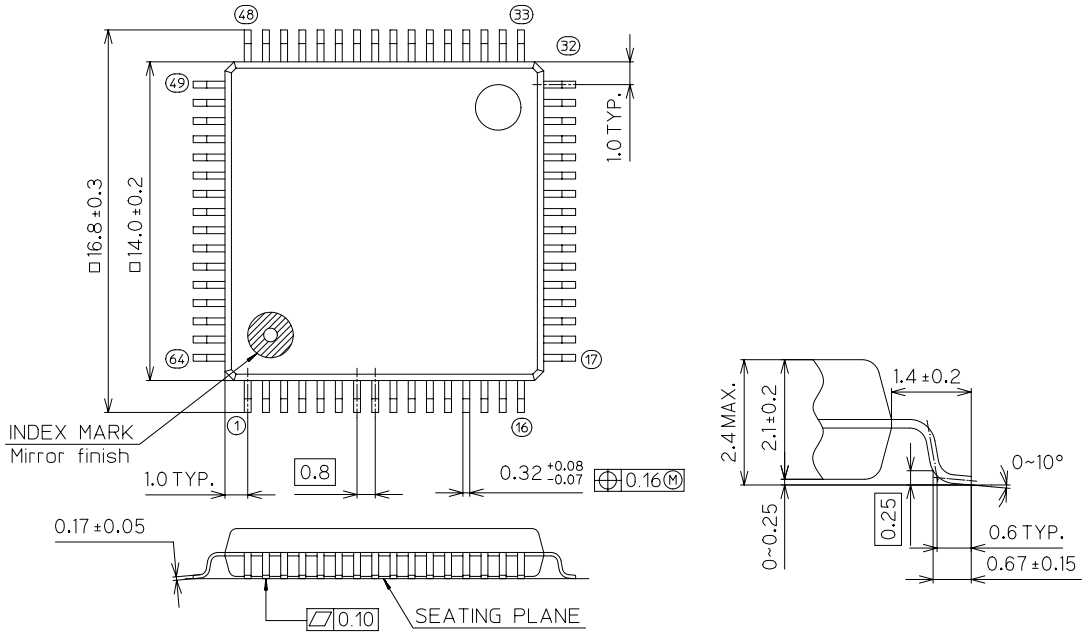


Application circuit example when four 4 Mbit OPT ROMs are connected (serial input interface)

PACKAGE DIMENSIONS

(Unit: mm)

QFP64-P1414-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.87 TYP.
Rev. No./Last Revised	5/Sept.21,1999

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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