FEDL9845DIGEST-01

OKI Semiconductor

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MSM9845

VOICE SYNTHESIS LSI with on-chip FIFO Memory

This document contains minimum specifications. For full specifications, please contact your nearest Oki office or representative.

GENERAL DESCRIPTION

MSM9845 is a Voice Synthesizer LSI with on-chip FIFO memory.
A newly developed synthesis algorithm, OKI ADPCM2, promises superb sound quality. The LSI is fully controllable from an external CPU via 16/8-bit bus interface.
MSM9845 is an ideal choice for application systems where such non-microchip data storage as CD ROM is used.

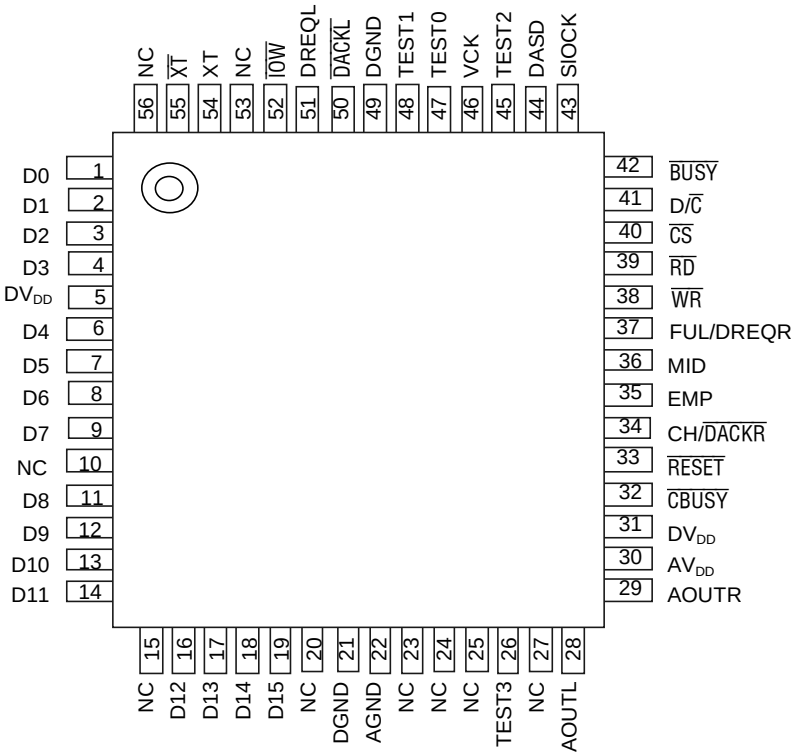
FEATURES

- 16/8-bit Bus Interface
- On-chip FIFO Memory Capacity : 1024 Bits 16 ms Buffering
  When Sampling Frequency at 16.0 kHz, 4-bit ADPCM2 and Monaural Playback selected
- Synthesis Algorithms for User's Selection
  4, 5, 6, 7, 8-bit Oki ADPCM2
  4-bit Oki ADPCM
  8/16-bit Straight PCM
  8-bit Oki Non-Linear PCM
- Oscillation Clock Frequency: 16.9344 MHz/24.576 MHz
- Sampling Frequency:
  11.025 kHz, 22.05 kHz, 44.1 kHz at f_{OSC} = 16.9344 MHz
  4.0 kHz, 6.4 kHz, 8.0 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz, 48.0 kHz at f_{OSC} = 24.576 MHz
- Sound Level Control (8 levels, 0 dB to –21 dB)
- Built-in 14-bit D/A Converter
- 3 types of Serial Interface for External DAC
- Sampling Rate Conversion Function
- Packaging: 56-pin Plastic QFP (QFP56-P-910-0.65-2K)
  Product Code: MSM9845GA

DIFFERENCE BETWEEN MSM9845 AND MSM9844

ITEM	MSM9845GA	MSM9844GA
SRC	On-Chip FIR Filter	Not On-Chip FIR Filter

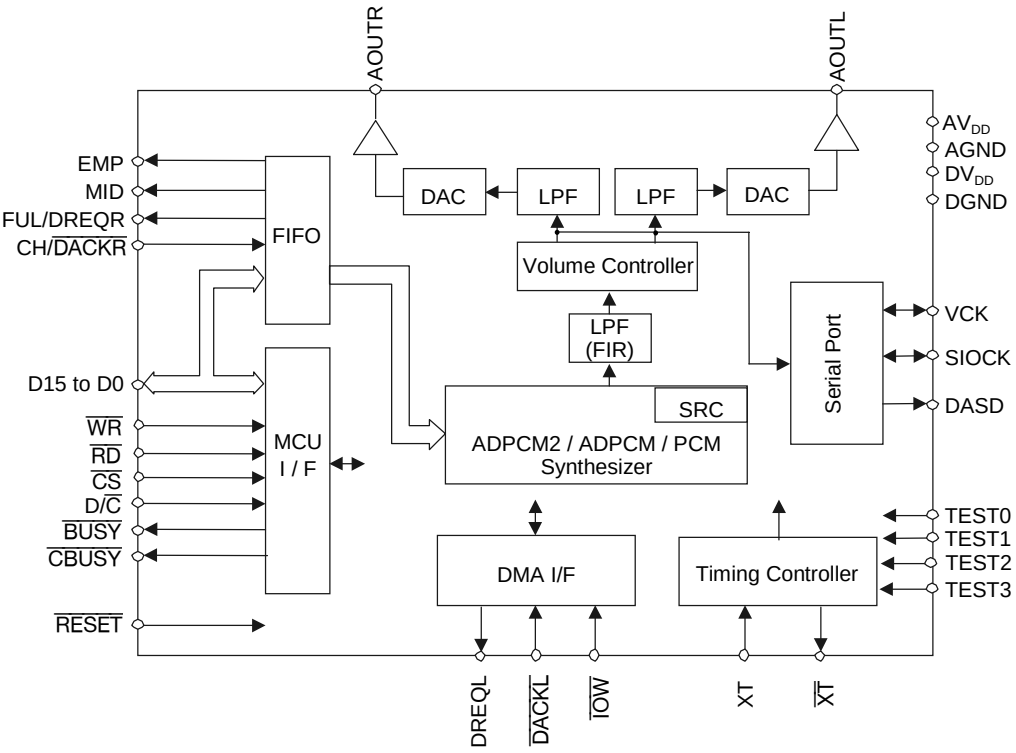
PIN CONFIGURATION (TOP VIEW)



NC : No Connection

56-Pin Plastic QFP

BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Symbol	Type	Description
11 - 14 16 - 19	D15 to D8	I/O	When 8-bit bus interface selected, you can define, by using a command, these pins as input/output to/from external memory. When no definition made, these pins are input mode. When 16-bit bus interface selected, they are one half of bi-directional data bus for data input/output from/to external micro-controller and memory.
1 - 4 6 - 9	D7 to D0	I/O	Another half of bi-directional data bus for data input/output from/to external micro-controller and memory and for status output.
38	$\overline{WR}$	I	WRITE pulse input pin. Input “L” pulse before you can enter command and data to D15 to D0 pins.
39	$\overline{RD}$	I	READ pulse input pin. Input “L” pulse before the LSI can output status and data to D15 to D0 pins.
40	$\overline{CS}$	I	With this pin at “L” level, the LSI accepts WRITE or READ pulse input. At “H” level the LSI would not accept WRITE or READ pulse.
41	D/$\overline{C}$	I	While this pin being held “H”, D15 to D0 pins are enabled to input/output sound data. While this pin being held “L”, D7 to D0 pins are enabled to input a command or output status data.
42	$\overline{BUSY}$	O	Output “L” level during playback/PAUSE operation.
32	$\overline{CBUSY}$	O	Output “L” level when the LSI is ready to accept a command.
35	EMP	O	“H” level output from this pin indicates FIFO memory is empty. You can change this pin to “L” active by a command input.
36	MID	O	“H” level output from this pin indicates FIFO memory is more than half. During playback, voice synthesis starts when MID changes to “H” level. You can change this pin to “L” active by a command input. This pin outputs a synchro signal for voice data input / output when non-use of FIFO is selected.
37	FUL/ DREQR	O	“H” level output from this pin indicates FIFO memory is full. During playback operation this pin is held “H” and FIFO memory is write -disabled. You can change this pin to “L” active by a command input. When DMA Transfer and stereo-playback selected by the command input, the output from this pin becomes DMA Transfer request signal. The pin outputs “H” when the right channel FIFO memory is empty. You can change this pin to “L” active by a command input.
34	CH/ $\overline{DACKR}$	I	When stereo-playback selected, write sound data to the right channel FIFO at “H” level, while data to the left channel FIFO at “L” level. When monaural playback selected, keep this pin “L”. You can change this pin to “L” active by a command input. When DMA Transfer and stereo-playback selected by the command input, this pin acknowledges the right channel DMA Transfer permission signal. With this pin at “L” level the LSI enabled the $\overline{IOW}$ pin to accept the signal. You can change this pin to “H” active by a command input.
51	DREQL	O	Output “H” level to represent DMA Transfer request signal when FIFO gets empty. If stereo-playback selected, the pin outputs “H” level to represent DMA Transfer request signal when the left channel FIFO gets empty.

Pin	Symbol	Type	Description
50	$\overline{\text{DACKL}}$	I	DMA Transfer Permission Acknowledgement signal. With this pin at "L" level the LSI enables the $\overline{\text{IOW}}$ pin to accept the signal. When stereo-playback selected, the pin acknowledges DMA Transfer permission signal for the left channel FIFO. You can change this pin to "H" active by a command input. When DMA Transfer is not in use, keep the pin "H".
52	$\overline{\text{IOW}}$	I	When DMA Transfer selected, the signal to start writing external memory data to the MSM9845 is entered to this pin. When DMA Transfer is not use, keep the pin "H".
44	DASD	O	16-bit serial data output pin when the external DAC is in use.
43	SIOCK	I/O	Synchronizing clock signal for 16-bit serial data input/output when the external DAC is in use.
54 55	XT $\overline{\text{XT}}$	I O	Pins wired to the oscillator. When the external clock is used, input the clock signal to the XT pin and keep the $\overline{\text{XT}}$ pin open.
46	VCK	I/O	Input/Output the sampling frequency in use. The signal is used as the synchronizing signal when the external DAC is in use.
33	$\overline{\text{RESET}}$	I	"L" level input to this pin turns the LSI to the initial status.
47, 48 45, 26	TEST0, 1 TEST2, 3	I	Pins for testing the LSI. Keep these pins "L".
28	AOUTL	O	The left channel output from the built-in LPF. Analog waveform output can be directly connected to an amplifier to drive a speaker.
29	AOUTR	O	The right channel output from the built-in LPF. Analog waveform output can be directly connected to an amplifier to drive a speaker.
5, 31	DV_{DD}	—	Digital power supply pin. Insert a 0.1µF or larger bypass capacitor between this pin and the DGND pin.
21, 49	DGND	—	Digital GND pin.
30	AV_{DD}	—	Analog power supply pin. Insert a 0.1µF or larger bypass capacitor between this pin and the AGND pin.
22	AGND	—	Analog GND pin.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Conditions	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}		–0.3 to V_{DD} +0.3	V
Power Dissipation	P_D		571.4	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Conditions	Rating	Unit
Power Supply Voltage	V_{DD}	DGND = AGND = 0 V	+4.5 to +5.5	V
Operating Temperature	T_{OP}	—	–40 to +85	°C
Master Clock Frequency	f_{OSC}	—	24.576	MHz

ELECTRICAL CHARACTERISTICS

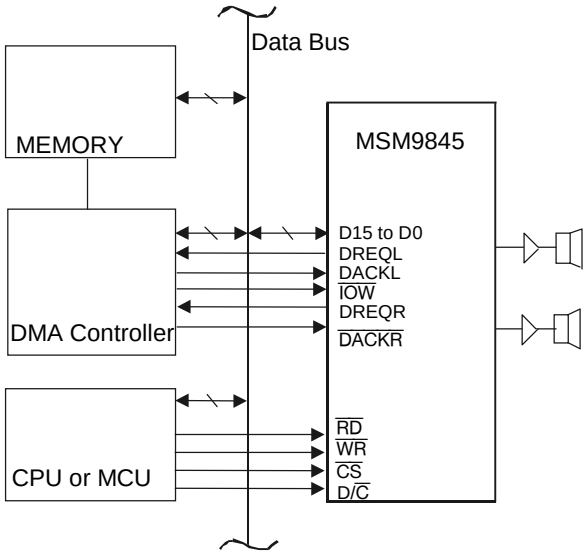
DC Characteristics

$DV_{DD} = AV_{DD}$ = +4.5 V to +5.5 V
DGND = AGND = 0 V, Ta = –40 to + 85°C

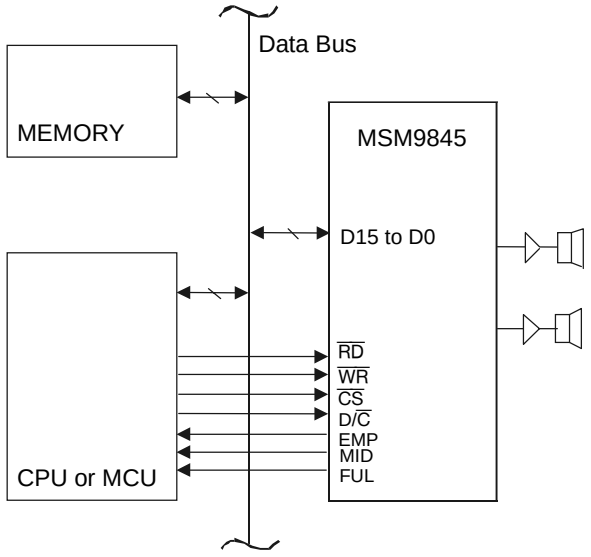
Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage		V_{IH}	—	$V_{DD} \times 0.85$	—	—	V
"L" Input Voltage		V_{IL}	—	—	—	$V_{DD} \times 0.15$	V
"H" Output Voltage	note 1	V_{OH1}	I_{OH} = –40 µA	V_{DD} –0.3	—	—	V
"L" Output Voltage	note 1	V_{OL1}	I_{OL} = 2 mA	—	—	0.45	V
"H" Output Voltage	note 2	V_{OH2}	I_{OH} = –40 µA	V_{DD} –0.3	—	—	V
"L" Output Voltage	note 2	V_{OL2}	I_{OL} = 2 mA	—	—	0.8	V
"H" Input Current	note 3	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
"H" Input Current	note 4	I_{IH2}	$V_{IH} = V_{DD}$	—	—	20	µA
"L" Input Current	note 3	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" Input Current	note 4	I_{IL2}	V_{IL} = GND	–20	—	—	µA
Operating Current Consumption		I_{DD}	f_{OSC} = 24.576 MHz without load	—	—	40	mA
Standby Current Consumption		I_{DDS}	At reset, power down without load Ta = –40 to +70°C	—	—	10	µA
			At reset, power down without load Ta = +70 to +85°C	—	—	50	µA

note 1) Applies to output pins excluding $\overline{XT}$ pin.
note 2) Applies to $\overline{XT}$ pin.
note 3) Applies to input pins excluding XT pin.
note 4) Applies to XT pins .

APPLICATION CIRCUIT SAMPLE



Sample 1 for 16 bit bus interface with DMA Controller

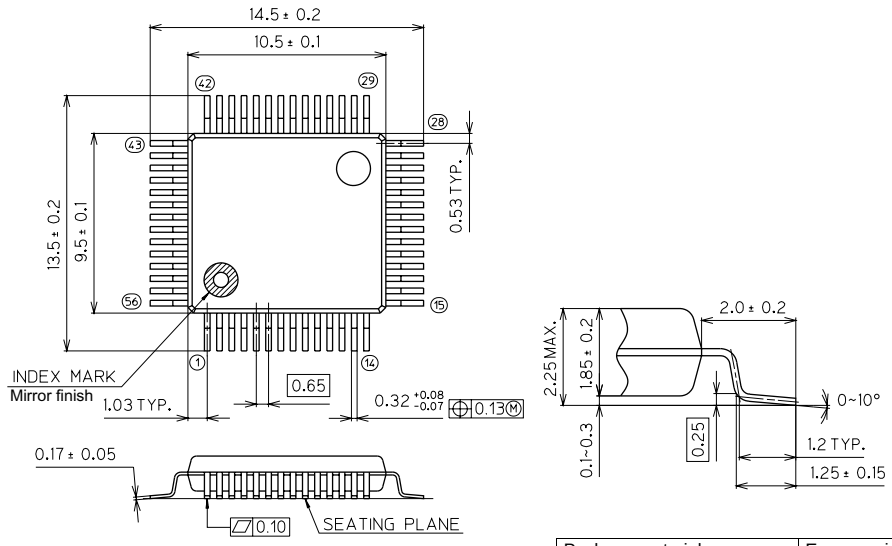


Sample 2 for 16 bit bus interface with External Memory

PACKAGE DIMENSIONS

(Unit: mm)

QFP56-P-910-0.65-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.43 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

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Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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