Technical Brief

OKI ASIC PRODUCTS

W812
IEEE 1394 Controller
0.35 µm Technology
Mega Macrofunction

November 1997

Oki Semiconductor

Contents

Oki Semiconductor

W812 IEEE 1394 Link Layer Controller

0.35 μm Technology Mega Macrofunction

DESCRIPTION

The W812, Oki Semiconductor's 1394 Link Layer Controller, is IEEE 1394-1995 compliant and features an embedded high-performance application bus interface. This device performs data packaging according to the IEEE 1394-1995 Standard, and bidirectional asynchronous / isochronous data transfers to / from an IEEE 1394 serial bus physical layer (PHY) device.

The W812 is optimized for use as a peripheral link layer controller. The application bus interface, which transfers data between a FIFO and the host controller, is designed for highly efficient transport. Oki also provides an optional FIFO controller, the W812-F to readily interface with the W812.

Oki's W812 accommodates different application needs by using a flexible architecture which to support both asynchronous and isochronous data transfers or only asynchronous data transfers. This technology give system designers the maximum flexibility in their design.

FEATURES

- Compliant with IEEE 1394-1995 Standard Link Layer Controller
- Compatible with Texas Instruments' Physical Layer Controllers
- Offers programmable FIFO channel for asynchronous and isochronous transmission and general reception
- Supports transfer rates of 100, 200, and 400 Mbps
- Uses flexible architecture to support both asynchronous and isochronous data transfers or only asynchronous data transfers
- Offers high performance application bus interface
- Has 32-bit cyclic redundancy check (CRC) for transmission and reception of 1394 packets

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	2.7	3.3	3.6	V
Operating temperature	T_j	-40	+25	+85	°C

Mega Macrofunction Characteristics

Mega Macrofunction	Description	Logic Gate Count	Logic Pin Count
W812	IEEE 1394 Link Layer Controller	12K	95

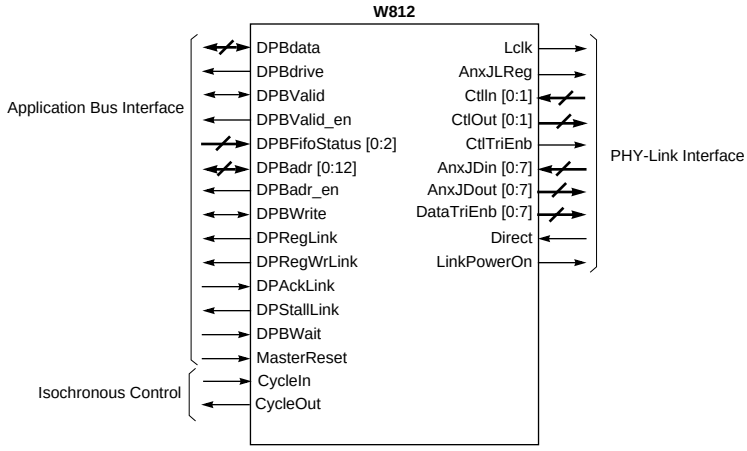

Figure 1. W812 Logic Symbol

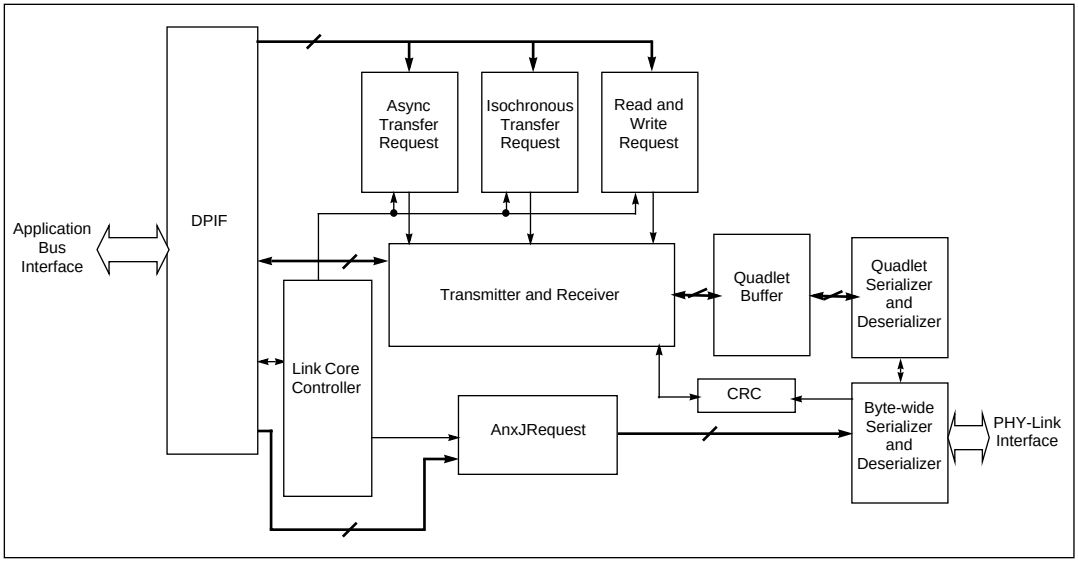

Figure 2. W812 Block Diagram

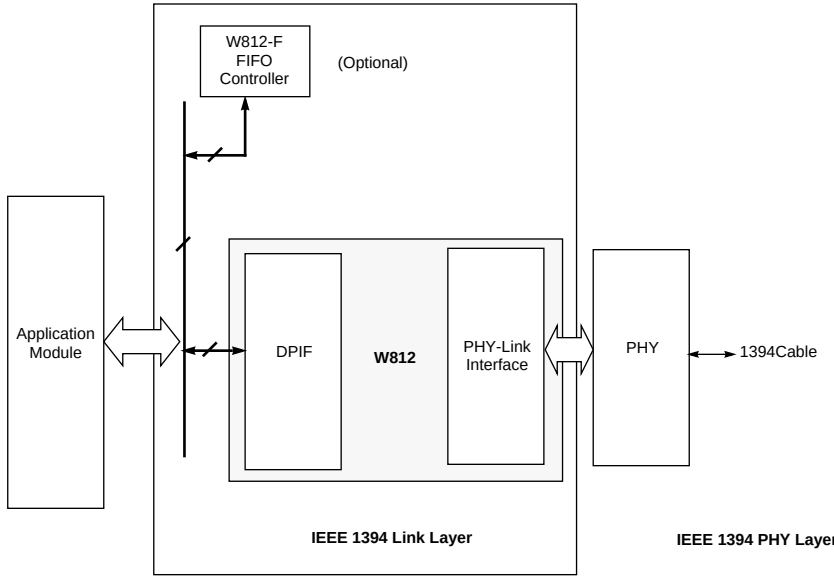

Figure 3. Example W812 Application

SIGNAL DESCRIPTIONS

PHY-Link Interface

Signal	Type	Assertion	Description
Lclk	In	—	50-MHz SCLK from PHY.
AnxJLReg	Out	—	LINK request port to PHY. Used to make bus requests or accesses to PHY.
CtlIn	In	—	Input from Bi-di control port for bi-directional pins.
CtlOut	Out	—	Output to Bi-di control port for bi-directional pins.
CtlTriEnb	Out	HIGH	Tri-state enable to Bi-di control port.
AnxJDin	In	—	Input from Bi-di data port. Used to exchange data with PHY.
AnxJDout	Out	—	Output to Bi-di data port. Used to exchange data with PHY.
DataTriEnb	Out	HIGH	Tri-state enable to Bi-di data port.
Direct	In	HIGH	Indicates LINK and PHY are directly connected, rather than through an isolation barrier.
LinkPowerOn	Out	HIGH	Indicates LINK is powered on.

Application Bus Interface

Signal	Type	Assertion	Description
DPBdata	Bi-di	—	**Data Path Data Bus.** Used to exchange data with other application modules.
DPBdrive	Out	HIGH	Indicates W812 is driving DPBdata.
DPBValid	Bi-di	HIGH	Indicates the quality description of DPBdata.
DPBValid_en	Out	HIGH	Enable to DPBValid signal
DPBFifoStatus	In	—	Indicates the FIFO status for fetches and stores by FIFO controller, such as Oki's W812-F.
DPBadr	Bi-di	—	**Data Path Bus Address**. Specifies the DPBus transfer.
DPBadr_en	Out	HIGH	Enables to DPBadr signals.
DPBWrite	Bi-di	HIGH	Specifies whether the DPBus transfer is a read or write.
DPReqLink	Out	HIGH	DPBus request line for LINK.
DPReqWrLink	Out	HIGH	DPBus request operation type line for LINK.
DPAckLink	In	HIGH	DPBus request grant line to LINK.
DPStallLink	Out	HIGH	LINK indication of need to extend current DPBus cycle.
DPBWait	In	HIGH	Indicates the DPBus operation is to be extended a cycle.
MasterReset	In	HIGH	Initializes the whole module. It is a synchronous reset, clocked by Lclk.

Isochronous Control Interface

Signal	Type	Assertion	Description
CycleIn	In	—	8-kHz clock to optionally indicate isochronous cycle.
CycleOut	Out	—	20-ns pulse to indicate the start of an isochronous cycle.

FUNCTIONAL DESCRIPTION

The W812 controller has three basic interfaces:

- Application Bus
- PHY-Link
- Isochronous Control

The Application Bus and Isochronous Control interfaces are application interfaces; whereas, the Link-PHY interface conforms to the IEEE 1394-1995 Standard (as described in Annex J section) and provides an industry standard interface to the PHY. The Application Bus interface provides a highly efficient interface to other application modules including the FIFO controller. Oki also provides an optional W812-F FIFO controller which is ready to interface with the W812.

Functional Modules

Data Path Interface (DPIF)

This block interfaces with Oki's high performance application bus which is a multi-drop multiple master bus that uses a streamlined, 3-phase protocol. W812 uses this interface to communicate with the application modules and necessary FIFO controller. Oki's bus interface is simple and relatively inexpensive in terms of pin and interface count. Yet the W812 has good bandwidth of ~200 MBps and a low and predictable latency. Oki's optional W812-F FIFO controller also uses this busing scheme to provide an overall high performance 1394 Link Layer solution.

Asynchronous Transfer Request

This block queues requests for asynchronous transmission by fetching all the necessary parameters to the transmitter and receiver.

Isochronous Transfer Request

This block queues requests for isochronous transmission by fetching all the necessary parameters to the transmitter and receiver.

Read-Write Request

This block queues read and write requests to the PHY register through the Annex J request block and formats and fetches request packets to the Annex J Request Block.

Annex J Request

This block generates the Annex J Request to the PHY. When more than one request is queued at the same time, this block prioritizes the queued requests.

Transmitter and Receiver

This block generates the flow control signals for the W812 and determines when, what, where, and how a packet is fetched during transmission and stored during reception. This block performs the following functions:

- Format appropriate packets
- Cycle monitor
- Cycle master

- Packet header check and decoding
- Coordinate function with optional FIFO controller
- Packet flow control for transmission and receiving

Byte-wide Serializer and Deserializer

During transmission, this block serializes an 8-bit byte into appropriate size of data according to the associated transmission speed. During receiving, this block accumulates receiving data, deserialzies it, and passes data one byte at a time to the Quadlet Serializer and Deserializer. This block also generates signal pertaining to the Annex J states like start and end of a receive, states during transmit or receive. It controls when to read and or write a byte from or to the Quadlet Serializer and Desirializer and when to compute new CRC.

Quadlet Serializer and Deserializer

During transmission, this block serializes 32-bit data into four 1-byte data. During receiving, this block deserialzies four 1-byte data at a time into a 32-bit quadlet.

Quadlet Buffer

This block is a FIFO-type storage area.

Link Core Controller State Machine

This machine performs link layer packet transmit and receive operations as described in Figure 6-19, of *IEEE Standard 1394-1995*.

CRC Generator and Checker

This block generates and checks the CRC. The 32-bit polynomial function is as follows:

$$G(x) = x(32) + x(26) + x(23) + x(22) + x(16) + x(12) + x(11) + x(10) + x(8) + x(7) + x(5) + x(4) + x(2) + x + 1$$

To run the W812 at 400 Mbps, this block uses a specialized scheme to achieve desired performance.

Notes:

Notes:

References

See the *IEEE 1394-1995 Standard* for more information on Link Layer Controller functionality.

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