

HCMOS/TTL COMPATIBLE TRI-STATE VCXO IN CERAMIC LCC PACKAGE - VC75 Series

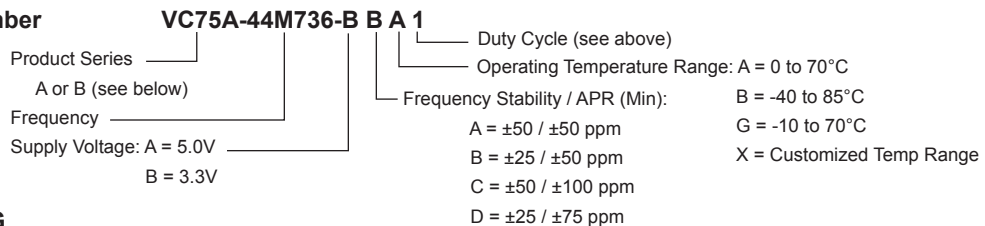
FEATURES

- RoHS Compliant (Pb-Free), Wide Frequency Pulling Range
- Very Low Phase Jitter with Fundamental Crystal Design, 5 VDC or 3.3 VDC Option
- Leadless Chip Carrier (LCC) Ultra Small Package with Industry de facto Standard Footprint
- Optional Enable/Disable Control at Either Pin #2 (VC75A) or Pin #5 (VC75B)

SPECIFICATIONS

Frequency Range	1 MHz to 77.760 MHz (5V), to 125 MHz (3.3V)
Input Voltage (Vcc)	A = +5 VDC ± 5%; B = +3.3 VDC ± 5%
Input Current	30 mA Maximum, depending on frequency and output load
Control Voltage (Vc)	+2.5V ± 2.0V for 5.0V part; +1.65V ± 1.5V for 3.3V part
Storage Temperature	-55°C to 125°C
Frequency Stability / APR (Min)	A = ±50 / ±50 ppm; B = ±25 / ±50 ppm; C = ±50 / ±100 ppm; D = ±25 / ±75 ppm
Temperature Range	A = 0°C to 70°C; B = -40°C to 85°C; G = -10°C to 70°C
Standard Stability / Pullability	BA = ±25 ppm / 0°C to 70°C, Absolute pull range (APR): ±50 ppm Minimum
Duty Cycle	1 = Tristate 60/40% symmetry; 3 = Tristate 55/45% symmetry
Output Load	HCMOS: drive up to 15 pF load; TTL: drive up to 10 TTL gates
Logic "1" / Logic "0" Level	0.9Vcc Minimum / 0.1Vcc Maximum
Rise/Fall Time (Tr/Tf)	5 ns Maximum at 20% to 80% Vp-p
Start-up time	10 ms Maximum
Phase Jitter (RMS, 1 Sigma)	1 ps Maximum for fj > 1kHz; 0.3 ps Typical for fj = 12KHz to 20MHz
Modulation Bandwidth	12 kHz Minimum at -3 dB
Linearity / Slope	±10% Maximum of best straight line fit / Positive
Input Impedance	10 kOhms Minimum
Setability at Fnom, 25°C	+2.5V ±0.5V for 5.0V part; +1.65V ±0.4V for 3.3V part
Tristate Function	Input (Pin 2 or 5) High (> 2.2V) or open: Output (Pin 4) active Input (Pin 2 or 5) Low (< 0.5V): Output disabled in high impedance
Enable/Disable Time	100 ns Maximum

Creating a Part Number



OUTLINE DRAWING

