

OKI Semiconductor

MSC23CV23218D-xxBS4

2,097,152-word x 32-bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

DESCRIPTION

The MSC23CV23218D-xxBS4 is a fully decoded, 2,097,152-word x 32-bit CMOS dynamic random access memory module composed of four 16Mb DRAMs (1Mx16) in TSOP packages mounted with eight decoupling capacitors on a 72-pin glass epoxy small outline package. This module supports any application where high density and large capacity of storage memory are required.

FEATURES

- 2,097,152-word x 32-bit organization
- 72-pin Small Outline Dual In-line Memory module
MSC23CV23218D-xxBS4 : Gold tab
- Single +3.3V supply $\pm 0.3V$ tolerance
- Input : LVTTTL compatible
- Output : LVTTTL compatible, 3-state
- Refresh : 1024cycles/16ms
- /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
- Fast page mode capability

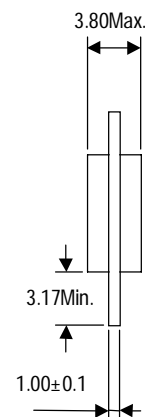
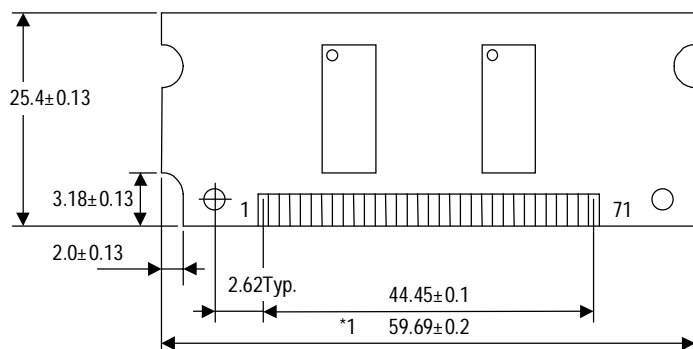
PRODUCT FAMILY

| Family | Access Time (Max.) | | | Cycle Time (Min.) | Power Dissipation | |
|---------------------|--------------------|-----------------|------------------|-------------------|-------------------|----------------|
| | t _{RAC} | t _{AA} | t _{CAC} | | Operating (Max.) | Standby (Max.) |
| MSC23CV23218D-60BS4 | 60ns | 30ns | 15ns | 110ns | 864mW | 7.2mW |
| MSC23CV23218D-70BS4 | 70ns | 35ns | 20ns | 130ns | 792mW | |

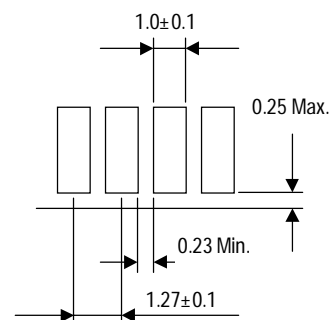
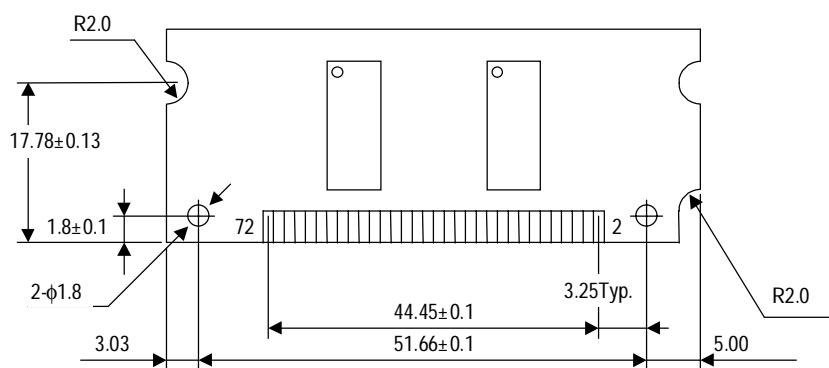
MODULE OUTLINE

MSC23CV23218D-xxBS4

(Unit : mm)



*1 The common size difference of the board width 19.78mm of its height is specified as ± 0.2 .
The value above 19.78mm is specified as ± 0.5 .



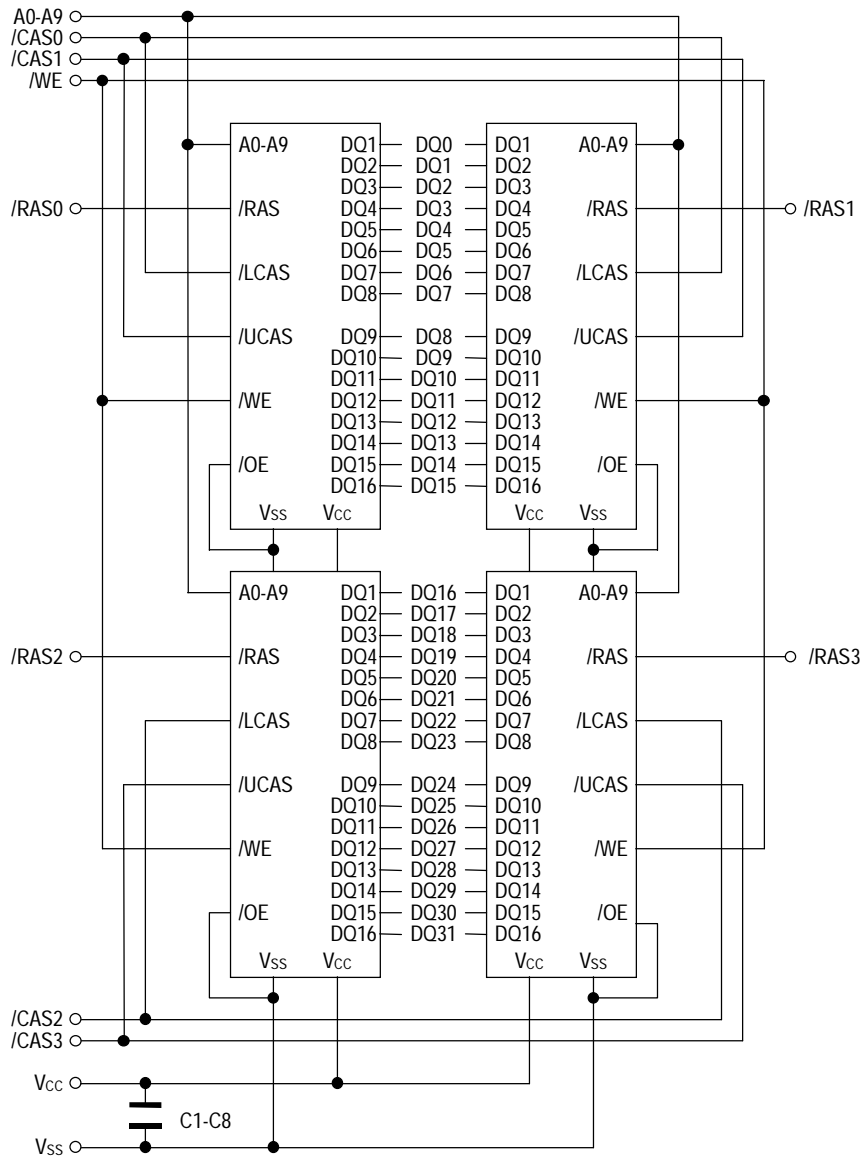
PIN CONFIGURATION

| Front Side | | | | Back Side | | | |
|------------|-----------------|---------|-----------------|-----------|-----------------|---------|-----------------|
| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
| 1 | V _{SS} | 37 | DQ16 | 2 | DQ0 | 38 | DQ17 |
| 3 | DQ1 | 39 | V _{SS} | 4 | DQ2 | 40 | /CAS0 |
| 5 | DQ3 | 41 | /CAS2 | 6 | DQ4 | 42 | /CAS3 |
| 7 | DQ5 | 43 | /CAS1 | 8 | DQ6 | 44 | /RAS0 |
| 9 | DQ7 | 45 | /RAS1 | 10 | V _{CC} | 46 | NC |
| 11 | PD1 | 47 | /WE | 12 | A0 | 48 | NC |
| 13 | A1 | 49 | DQ18 | 14 | A2 | 50 | DQ19 |
| 15 | A3 | 51 | DQ20 | 16 | A4 | 52 | DQ21 |
| 17 | A5 | 53 | DQ22 | 18 | A6 | 54 | DQ23 |
| 19 | A10 | 55 | NC | 20 | NC | 56 | DQ24 |
| 21 | DQ8 | 57 | DQ25 | 22 | DQ9 | 58 | DQ26 |
| 23 | DQ10 | 59 | DQ27 | 24 | DQ11 | 60 | DQ28 |
| 25 | DQ12 | 61 | V _{CC} | 26 | DQ13 | 62 | DQ29 |
| 27 | DQ14 | 63 | DQ30 | 28 | A7 | 64 | DQ31 |
| 29 | NC | 65 | NC | 30 | V _{CC} | 66 | PD2 |
| 31 | A8 | 67 | PD3 | 32 | A9 | 68 | PD4 |
| 33 | /RAS3 | 69 | PD5 | 34 | /RAS2 | 70 | PD6 |
| 35 | DQ15 | 71 | PD7 | 36 | NC | 72 | V _{SS} |

Presence Detect Pins

| Pin No. | Pin Name | -60 | -70 |
|---------|----------|-----------------|-----------------|
| 11 | PD1 | NC | NC |
| 66 | PD2 | V _{SS} | V _{SS} |
| 67 | PD3 | V _{SS} | V _{SS} |
| 68 | PD4 | NC | NC |
| 69 | PD5 | NC | V _{SS} |
| 70 | PD6 | NC | NC |

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|-------------------|--------------|------|
| Voltage on Any Pin Relative to V_{SS} | V_{IN}, V_{OUT} | -0.5 to +4.6 | V |
| Voltage on V_{CC} Supply Relative to V_{SS} | V_{CC} | -0.5 to +4.6 | V |
| Short Circuit Output Current | I_{OS} | 50 | mA |
| Power Dissipation | P_D * | 4 | W |
| Operating Temperature | T_{OPR} | 0 to +70 | °C |
| Storage Temperature | T_{STG} | -40 to +125 | °C |

* $T_a = 25^\circ\text{C}$

Recommended Operating Conditions

($T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------|----------|------|------|--------------|------|
| Power Supply Voltage | V_{CC} | 3.0 | 3.3 | 3.6 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V_{IH} | 2.0 | - | $V_{CC}+0.3$ | V |
| Input Low Voltage | V_{IL} | -0.3 | - | 0.8 | V |

Capacitance

($V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

| Parameter | Symbol | Typ. | Max. | Unit |
|----------------------------------|-----------|------|------|------|
| Input Capacitance (A0 - A9) | C_{IN1} | - | 31 | pF |
| Input Capacitance (/WE) | C_{IN2} | - | 35 | pF |
| Input Capacitance (/RAS0- /RAS3) | C_{IN3} | - | 13 | pF |
| Input Capacitance (/CAS0- /CAS3) | C_{IN4} | - | 20 | pF |
| I/O Capacitance (DQ0 - DQ31) | C_{DQ} | - | 20 | pF |

DC Characteristics

(V_{CC} = 3.3V ± 0.3V, Ta = 0°C to +70°C)

| Parameter | Symbol | Condition | -60 | | -70 | | Unit | Note |
|---|------------------|--|------|-----------------|------|-----------------|------|------|
| | | | Min. | Max. | Min. | Max. | | |
| Input Leakage Current | I _{LI} | 0V ≤ V _{IN} ≤ V _{CC} +0.3V; All other pins not under test = 0V | -40 | 40 | -40 | 40 | μA | |
| Output Leakage Current | I _{LO} | DQ disable 0V ≤ V _{OUT} ≤ V _{CC} | -20 | 20 | -20 | 20 | μA | |
| Output High Voltage | V _{OH} | I _{OH} = -2.0mA | 2.4 | V _{CC} | 2.4 | V _{CC} | V | |
| Output Low Voltage | V _{OL} | I _{OL} = 2.0mA | 0 | 0.4 | 0 | 0.4 | V | |
| Average Power Supply Current (Operating) | I _{CC1} | /RAS, /CAS cycling, t _{RC} = Min. | - | 240 | - | 220 | mA | 1, 2 |
| Power supply current (Standby) | I _{CC2} | /RAS, /CAS = V _{IH} | - | 8 | - | 8 | mA | 1 |
| | | /RAS, /CAS ≥ V _{CC} -0.2V | - | 2 | - | 2 | mA | 1 |
| Average Power Supply Current (/RAS only refresh) | I _{CC3} | /RAS cycling, /CAS = V _{IH} , t _{RC} = Min. | - | 240 | - | 220 | mA | 1, 2 |
| Average Power Supply Current (/CAS before /RAS refresh) | I _{CC6} | /RAS cycling, /CAS before /RAS | - | 240 | - | 220 | mA | 1, 2 |
| Average Power Supply Current (Fast Page Mode) | I _{CC7} | /RAS = V _{IL} , /CAS cycling, t _{PC} = Min. | - | 170 | - | 160 | mA | 1, 3 |

- Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. The address can be changed once or less while /RAS = V_{IL}.
 3. The address can be changed once or less while /CAS = V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 3.3V ± 0.3V, T_a = 0°C to +70°C) Note: 1, 2, 3

| Parameter | Symbol | -60 | | -70 | | Unit | Note |
|--|-------------------|------|------|------|------|------|---------|
| | | Min. | Max. | Min. | Max. | | |
| Random Read or Write Cycle Time | t _{RC} | 110 | - | 130 | - | ns | |
| Fast Page Mode Cycle Time | t _{PC} | 40 | - | 45 | - | ns | |
| Access Time from /RAS | t _{RAC} | - | 60 | - | 70 | ns | 4, 5, 6 |
| Access Time from /CAS | t _{CAC} | - | 15 | - | 20 | ns | 4, 5 |
| Access Time from Column Address | t _{AA} | - | 30 | - | 35 | ns | 4, 6 |
| Access Time from /CAS Precharge | t _{CPA} | - | 35 | - | 40 | ns | 4 |
| Output Low Impedance Time from /CAS | t _{CLZ} | 0 | - | 0 | - | ns | 4 |
| /CAS to Data Output Buffer Turn-off Delay Time | t _{OFF} | 0 | 15 | 0 | 20 | ns | 7 |
| Transition Time | t _T | 3 | 50 | 3 | 50 | ns | 3 |
| Refresh Period | t _{REF} | - | 16 | - | 16 | ms | |
| /RAS Precharge Time | t _{RP} | 40 | - | 50 | - | ns | |
| /RAS Pulse Width | t _{RAS} | 60 | 10K | 70 | 10K | ns | |
| /RAS Pulse Width (Fast Page Mode) | t _{RASP} | 60 | 100K | 70 | 100K | ns | |
| /RAS Hold Time | t _{RSH} | 15 | - | 20 | - | ns | |
| /CAS Precharge Time (Fast Page Mode) | t _{CP} | 10 | - | 10 | - | ns | |
| /CAS Pulse Width | t _{CAS} | 15 | 10K | 20 | 10K | ns | |
| /CAS Hold Time | t _{CSH} | 60 | - | 70 | - | ns | |
| /CAS to /RAS Precharge Time | t _{CRP} | 5 | - | 5 | - | ns | |
| /RAS Hold Time from /CAS Precharge | t _{RHCP} | 35 | - | 40 | - | ns | |
| /RAS to /CAS Delay Time | t _{RCD} | 20 | 45 | 20 | 50 | ns | 5 |
| /RAS to Column Address Delay Time | t _{RAD} | 15 | 30 | 15 | 35 | ns | 6 |
| Row Address Set-up Time | t _{ASR} | 0 | - | 0 | - | ns | |
| Row Address Hold Time | t _{RAH} | 10 | - | 10 | - | ns | |
| Column Address Set-up Time | t _{ASC} | 0 | - | 0 | - | ns | |
| Column Address Hold Time | t _{CAH} | 10 | - | 15 | - | ns | |
| Column Address to /RAS Lead Time | t _{RAL} | 30 | - | 35 | - | ns | |
| Read Command Set-up Time | t _{RCS} | 0 | - | 0 | - | ns | |
| Read Command Hold Time | t _{RCH} | 0 | - | 0 | - | ns | 8 |
| Read Command Hold Time referenced to /RAS | t _{RRH} | 0 | - | 0 | - | ns | 8 |

AC Characteristics (2/2)

(V_{CC} = 3.3V ± 0.3V, T_a = 0°C to +70°C) Note: 1, 2, 3

| Parameter | Symbol | -60 | | -70 | | Unit | Note |
|--|------------------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | | |
| Write Command Set-up Time | t _{WCS} | 0 | - | 0 | - | ns | |
| Write Command Hold Time | t _{WCH} | 10 | - | 15 | - | ns | |
| Write Command Pulse Width | t _{WP} | 10 | - | 10 | - | ns | |
| Write Command to /RAS Lead Time | t _{RWL} | 15 | - | 20 | - | ns | |
| Write Command to /CAS Lead Time | t _{CWL} | 15 | - | 20 | - | ns | |
| Data-in Set-up Time | t _{DS} | 0 | - | 0 | - | ns | |
| Data-in Hold Time | t _{DH} | 10 | - | 15 | - | ns | |
| /CAS Active Delay Time from /RAS Precharge | t _{RPC} | 5 | - | 5 | - | ns | |
| /RAS to /CAS Set-up Time (/CAS before /RAS) | t _{CSR} | 10 | - | 10 | - | ns | |
| /RAS to /CAS Hold Time (/CAS before /RAS) | t _{CHR} | 10 | - | 10 | - | ns | |

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.
 2. The AC characteristics assumes $t_T = 5$ ns.
 3. $V_{IH}(\text{Min.})$ and $V_{IL}(\text{Max.})$ are reference levels for measuring input timing signals. Transition time (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 1TTL loads and 100pF. The output timing reference levels are $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
 5. Operation within the $t_{RCD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met. $t_{RCD}(\text{Max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{Max.})$ limit, then the access time is controlled by t_{CAC} .
 6. Operation within the $t_{RAD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met. $t_{RAD}(\text{Max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{Max.})$ limit, then the access time is controlled by t_{AA} .
 7. $t_{OFF}(\text{Max.})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.