



**XEMICS**

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**AN8000.09**  
**Application note**

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**D.F.L.L.**  
**Digital Frequency Locked Loop**

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# AN8000.09

# Application note

## Introduction

This application note describes the implementation of a D.F.L.L. (Digital Frequency Locked Loop) algorithm for the XE8000 series.

The XE8000 series standard products include 2 oscillators, an imprecise RC oscillator ( $\pm 35\%$ ), and a precise quartz oscillator ( $\pm 200\text{ppm}$ ).

The D.F.L.L. locks the frequency of the RC oscillator on the quartz frequency, thereby making it a precision of ( $\pm 2\%$ ). The precision of the D.F.L.L. is based on the precision of the quartz oscillator.

For the XE8000 series, this algorithm is needed in an area, for example like UART communications where bauds rates of between 4800 and 38400 are used.

**Please note that the implementation in C language of the D.F.L.L. algorithm can be found on XEMICS' web site.**

## D.F.L.L. Principle

Within the XE8000 series the following two types of clocks are found:

- One quartz oscillator (32768 Hz)
- One RC oscillator. This oscillator has two ranges : 100 kHz - 1 MHz and 1 MHz - 10 MHz

Once reaching 32768 clock cycles, the quartz oscillator guarantees a frequency with a stable duty cycle. The CPU and its peripherals can also employ this. This stability remains sufficient even when there are temperature variations.

The RC oscillator will rapidly stabilize (in 8 clock cycles), but its frequency is highly dependent on temperature

For some applications, the frequency of a microcontroller can change in function of time and temperature. Therefore, in order to guaranty a fixed frequency on the RC oscillator, the user must periodically call on the D.F.L.L. routine.

## Counters and oscillators description

The XE8000 series standard product has four 8 bits up/down counters with 4 clock inputs. These up/down counters can be chained to make two 16 bits counters.

The D.F.L.L. routine uses an 8 bits down counter with a clock input from the quartz oscillator and an 8 bits up counter with a clock input from the RC oscillator.

The RC oscillator frequency is set by a trimming word of 11 bits.

- **1 bit** selects the range of the RC oscillator: 100 kHz - 1MHz or 1MHz - 10 MHz. When this bit is reset we have the lowest frequency range.
- **4 bits** for a coarse adjustment of frequency. With these four bits we can adjust 16 different frequencies according to the range bit.
- **6 bits** for a fine adjustment of the frequency chosen approximately by the 4 bits of coarse and the range bit.

## D.F.L.L. Description

When the D.F.L.L. routine is executed, the RC oscillator frequency converges to the frequency programmed in four phases:

1. An approximate adjustment of the frequency is made with the 4 bits of coarse and the range bit.
2. Calculation at 2% of max and min value of up counter to be reached.
3. Frequency measurement.
4. A test to determine that the measured frequency lies within a 2% range of the preferred frequency.

The 3<sup>rd</sup> and 4<sup>th</sup> phases can be executed as many times as necessary to reach the preferred frequency.

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## Detailed description

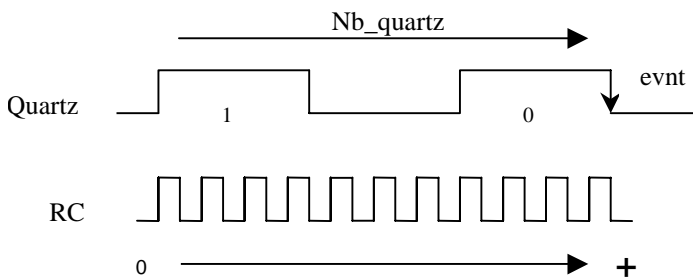
For this application, the up counter clock input is the RC oscillator and the down counter clock input is the XTAL oscillator. The down counter is loaded with an initial value that represents the number of clock cycles during the period for which the down counter is active. By having a greater initial value leads to both having a higher D.F.L.L precision and a higher time of measurement. The counter will decrement at a frequency of 32768 Hz. The up counter will increment at the frequency of the RC oscillator given by the trimming word (initial value of up counter is 0x00).

**Phase 1:** The RC oscillator is set approximately to the preferred frequency by setting the range and its coarse bits according to the input frequency. The fine adjustment is set at the middle of its range.

**Phase 2:** The calculation of the value to be set in the up counter is based on the following equation:  

$$\text{CntValue} = ((\text{Nb\_quartz} + 1) * \text{Frequency}) / 32768.$$
 Once the CntValue is obtained, the CntValue margins between +2% and -2% are then calculated.

**Figure 1:** above demonstrates that the counter



down clocked by the quartz oscillator generates an event on the falling edge of the zero value. At this time, the RC oscillator counter value is memorised, and is then followed by a comparison of the value to be reached.

Nb\_quartz value is defined in function of the frequency to be found. In the implementation of D.F.L.L., the values chosen are 20 for frequencies smaller than 650 kHz and 1 for frequencies greater than 650 kHz.

With a Nb quartz value of 20 for low frequencies, the precision of frequency measurement is increased due to the higher value in the up counter at the end of measurement.

**Phase 3:** Starts the down counter, then the CPU is put in HALT mode. The HALT mode disables the CPU clock. On the other hand, all counters, oscillators, watchdog, voltage regulators and interrupt/events handler are enabled.

Once the down counter reaches the value 0x00 it generates an event that wakes up the CPU. (Figure 1). The CPU will then reactivate the up counter and go back into HALT mode.

When the down counter generates the next event, the two counters cease. The up counter value relates to the RC oscillator frequency. This value is used on the 4<sup>th</sup> phase of the D.F.L.L. routine.

**Phase 4:** This phase compares the up counter value with the range of maximum and minimum values to be reached. When the value of the up counter is greater than the maximum value to be reached we decrement the bits of fine-tuning. When the value of the up counter is less than the minimum value to be reached we increment the bits of fine-tuning.

## D.F.L.L. Utilization

In the first instance where the D.F.L.L. routines are used, the first routine to be called must be InitializeDFLL, this must have as a parameter the frequency to be reached. The 2<sup>nd</sup> instance must use the DFLLRun routine applying again the same given parameter as the one used for InitializeDFLL.

The InitializeDFLL routine must be called only at the beginning of your application or when your application frequency changes.

The DFLLRun routine should only be called when you need to have a precise frequency or when you want to change the RC oscillator frequency.

## Improvements to D.F.L.L. routines

At present, the RunDFLL routine does not test possible errors.

A typical error occurs when the DFLL is not able to lock in the preferred frequency, this will cause it to run infinitely and therefore prevents it from returning to the main program.

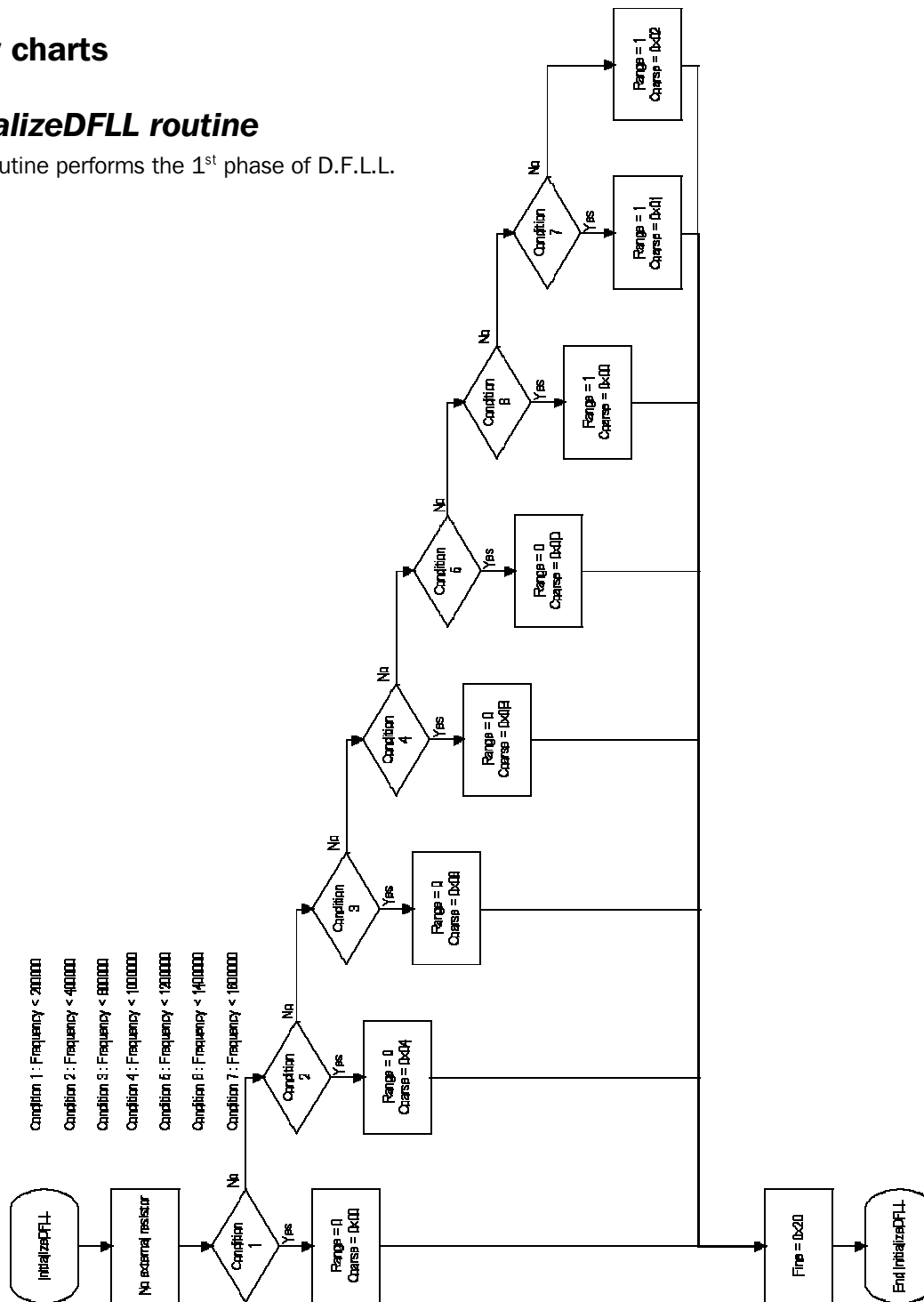
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## Flow charts

### InitializeDFLL routine

This routine performs the 1<sup>st</sup> phase of D.F.L.L.



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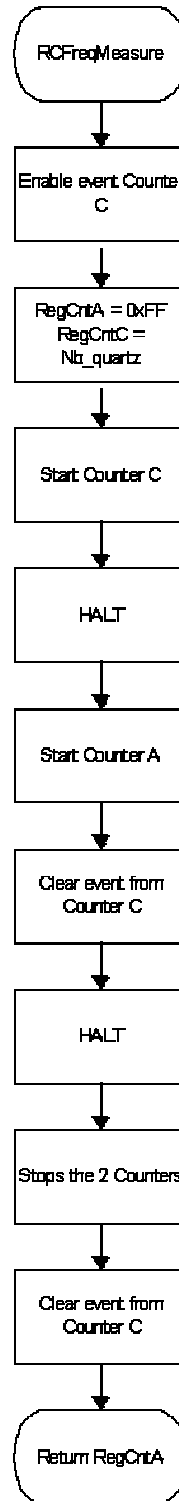
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## ***RCFreqMeasure routine***

This routine is performed in the 3<sup>rd</sup> phase of D.F.L.L



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