XEMICS

AN8000.02

Application note

XE8000 MTP programming

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1 Introduction

This application note concerns all the XE8000M products.

The MTP programming process uses the test interface of the CoolRISC. This includes the main clock of the processor, another clock (ptck) and its test-in, test-out and test-check ports. These signals are multiplexed on the oscillator pins, as well as on ports A and B. In order to connect the internal signals to inputs the XE8000 must be in test mode (TEST/VPP above VDD).

Two types of high voltage pulses are used: normal (5 us) and long (10 s) voltage pulses. Long voltage pulses are required to erase the MTP. The exact duration of these voltage pulses will be updated with the final product. Prototypes are programmed with 40 us normal pulses.

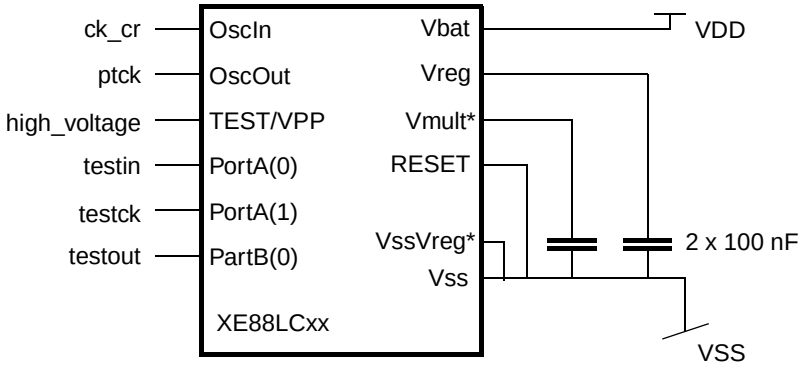


Figure 1.1: XE88LCxxM connection for programming. Vmult, VssVreg pins are not available on all packages. Unused pins shall be left floating

MTP signal	pad in test mode
testin	PortA(0)
testout	PortB(0)
testck	PortA(1)
ck_cr	OscIn
ptck	OscOut
high_voltage	TEST/VPP

Table 1.1: MTP signal connection to pads

parameter	min	max	unit
vdd	2.40	5.50	V
vddt	vdd + 1.50	vdd + 2.00	V
vddhigh	10.4	10.6	V

Table 1.2: Power supply parameters during MTP programming (values for devices marked XE8851, XX88LC01-03-05 and dice delivered before June 2000)

2 Programming the whole MTP array using default settings

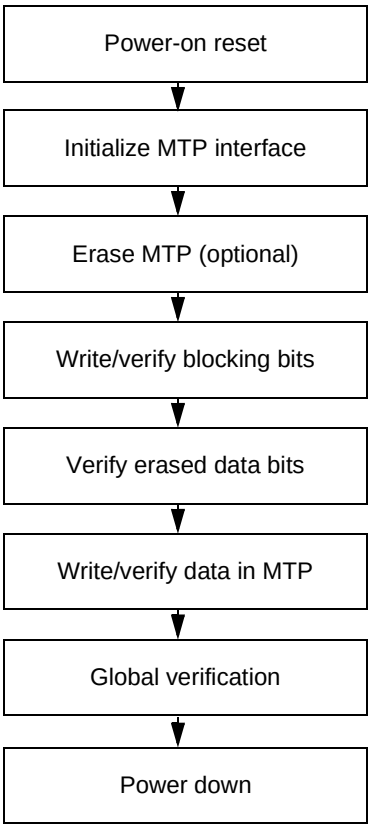


Figure 2.1: Default MTP programming algorithm.

The programming process of the complete flash array using default settings runs as follows:

1. After power-on reset, the flash interface is in a stable state. The clock of the interface does not influence its state.
2. The programmer must lock the chip in test mode and write two times 0x80 to **RegEEP1**,in order to give control of the flash array to the interface (that is the MTP interface initialisation sequence in Figure 2.1).
3. The programmer has to write 0x08 to **RegEEP**, then apply a wait sequence (read from **RegSysTest3**), one ptck pulse, one long high voltage pulse, two ptck pulses, and one long high voltage pulse (this is the erase sequence). This can be by-passed if the chip is already erased (new chips are delivered erased).
4. The programmer has to write 0x30 to **RegSysVIreg**, wait for 100 us. Then a sequence composed of two ptck pulses, one short high voltage pulse and three ptck pulses must be applied 16384 times (this is the blocking bits writing/verifying sequence).
5. The programmer must apply 1 ptck pulse, write 0x20 to **RegSysVIreg**, wait for 200 us (13 ms for the prototype on Starter-kit and ProStart), and apply 16384 pulses on ptck (this is the erased data verifying sequence).
6. He must write 0x30 to **RegSysVIreg** and wait for 200 us. For each address in the flash, the programmer has then to perform three CPU write operations to **RegEEP3**, apply a wait sequence (read from **RegSysTest3**), one ptck pulse, one short high voltage pulse and four ptck pulses. The three CPU write operations are necessary to write the data into the interface registers. The 8 least significant bits are written first, then the 8 next bits, and last the 6 most significant bits (this is the data writing sequence).
7. He must write 0x00 to **RegSysVIreg** and wait for 100 us (13 ms for the prototype on Starter-kit and ProStart), and then perform a CPU read operation at **RegEEP**. Bit 0 of the read byte indicates if an error occurred during the programming process (this is the global verification sequence).
8. After the MTP programming, the programmer should power down the chip.

3 Modifying the settings

Writing to **RegEEP1**, the programmer can modify the programming process.
- Bits 2 to 0 set an internal voltage. These bits should be set to 0b000.
- Bits 4 and 3 set an internal delay of the MTP memory. These bits should be set to 0b00.
- Bit 6 and 5 set the number of trials for witing in the memory. Default value is 0b00 (1 trial).
- Bit 7 determines who drives the control lines of the interface: the state machine of the interface or the CPU program bus.

4 Special operations

At any time during the whole programming process, the programmer can read or force the state, address, and data registers in the state machine of the interface. The state is accessible at **RegEEP**, the address register at **RegEEP2**, and the data register at **RegEEP3**. Since the address and data registers are multi-byte registers, they can not be accessed in one CPU peripheral read/write operation. Two successive CPU operations are necessary to access the address register. Three operations are necessary for the data register.

5 Examples of programming sequences

5.1 Introduction

In the following sequences, we use macro definitions and repeat loops to shorten the pattern length.

Basic ‘set’ pattern lines represents the values put on the ck_cr, testck, testin, ptck and high_voltage lines during one period. ‘check_testout(x)’ is a comparison of testout pin with the parameter ‘x’. The result is only correct if the testout pin is high for ‘x’ is ‘1’, and low for ‘x’ is ‘0’.

The macros used are the following:

```
macro cycle_cr_ck(nbcycles)  ;Toggle CoolRISC clock nbcycles times
  repeat nbcycles
    set(0 1 0 0 vdd)
    set(1 1 0 0 vdd)
  end repeat
end macro
```

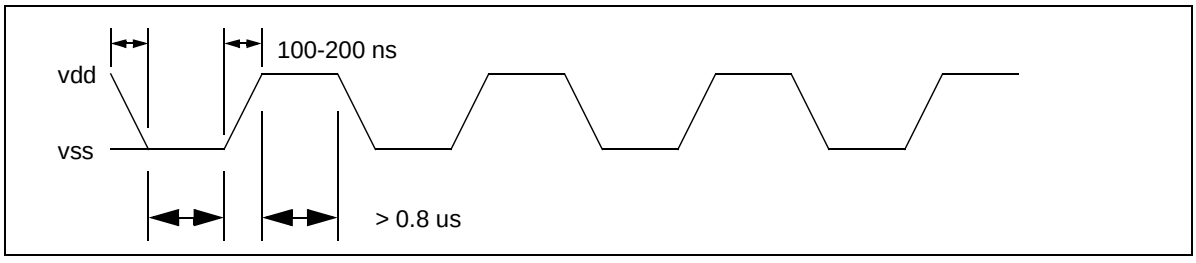


Figure 5.1: Timing diagram for cr_ck and ptck clock

```
macro cycle_ptck(nbcycles)  ;Toggle periperal test clock nbcycles times
  repeat nbcycles
    set(0 1 0 0 vdd)
    set(0 1 0 1 vdd)
```

```
  end repeat
end macro

macro shift_instruction(inst(21:0))  ; Repeat shift bit to input full
  for index=0 to 21                  ;   22 bits intruction
    set(1 0 inst(index) 0 vdd)
    set(1 1 inst(index) 0 vdd)
  end for
end macro shift_instruction
```

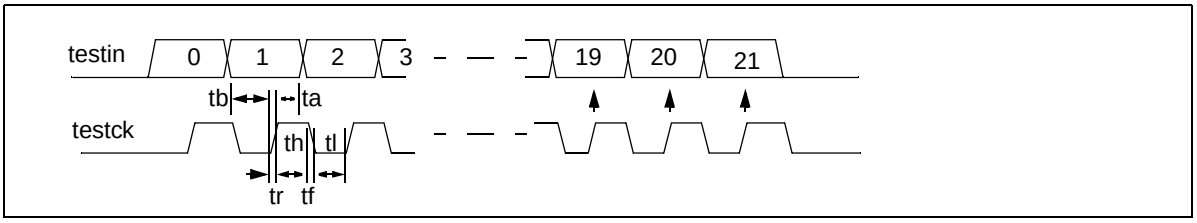


Figure 5.2: Timing diagram shift_instruction

parameter	description	min	max	unit
tb	testin stable before rise of testck	50		ns
ta	testin stable after rise of testck	50		ns
tr	testck rise time		100	ns
tf	testck fall time		100	ns
th	testck high	50		ns
tl	testck low	50		ns

Table 5.1: Testin and testck timing constraints

```
macro write_cr (address(7:0), data(7:0))
  cycle_cr_ck(1)
  shift_instruction(000000 not(data) not(address))
  cycle_ptck(1)
end macro
```

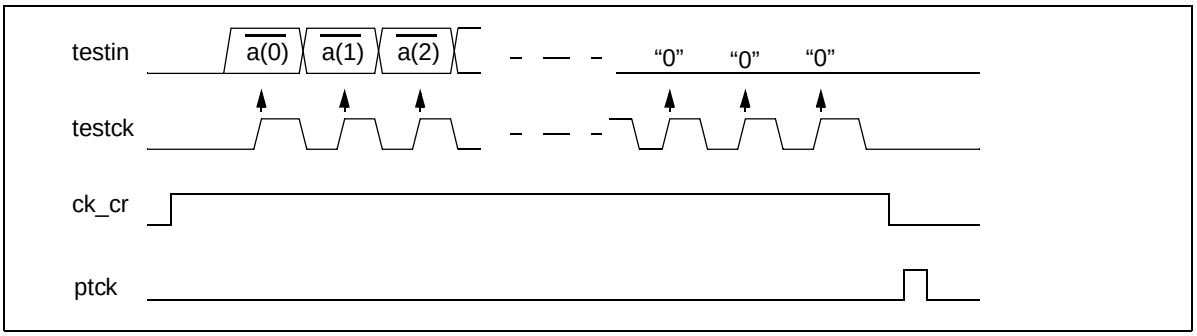


Figure 5.3: Timing diagram write_cr

```
macro write_cr_normal (address(7:0), data(7:0))
  cycle_cr_ck(1)
  shift_instruction(000000 not(data) not(address))
  cycle_cr_ck(1)
```

```
end macro

macro read_cr (address(7:0))
  cycle_cr_ck(1)
  shift_instruction(00010010101110 not(address))
  cycle_cr_ck(2)
  check_testout(0)
  shift_instruction(001110100011100000000l)
  cycle_cr_ck(2)
  shift_instruction(00110010101110111011l0)
  cycle_cr_ck(2)
  check_testout(1)
end macro

macro lock_test                          ;Got to test mode, then lock it, then
define inst: instruction (22 bits wide)
  set(0 1 0 0 vdd)                      ;  release high voltage line,
  set(0 1 0 0 vddt)                     ;  test mode is released at power down
  repeat 5
    set(0 1 0 0 vddt)
    set(1 1 0 0 vddt)
  end repeat
  inst=(000000 not(0x80) not(0x19))
  for index=0 to 21                      ;   22 bits intruction
    set(1 0 inst(index) 0 vddt)
    set(1 1 inst(index) 0 vddt)
  end for
  set(0 1 0 0 vddt)
  set(1 1 0 0 vddt)
  set(0 1 0 0 vdd)                      ;  set Vpp to Vdd
end macro

macro pulse_high_voltage (duration)     ;Put high voltage on VPP for MTP-
  set(0 1 0 0 vdd)                      ;  writing/erasing.
  set(0 1 0 0 vddhigh)
  wait(duration)
  set(0 1 0 0 vdd)
end macro
```

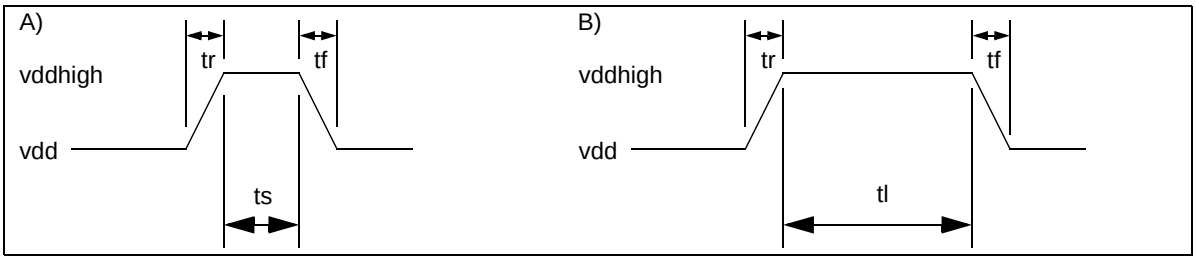


Figure 5.4: Timing diagram for pulse_high_voltage, for (A) short and (B) long pulses

parameter	description	min	max	unit
tr	rise time	2	3	us
tf	fall time	2	3	us

Table 5.2: High voltage pulse timing constraints

parameter	description	min	max	unit
ts	short pulse duration	8	10	us (micro-second)
tl	long pulse duration	9	10	s (second)

Table 5.2: High voltage pulse timing constraints

```
macro wait_cr
  cycle_ptck (1)
  shift_instruction(00010010101111111100110)
  cycle_ptck (1)
end macro

macro trim_vreg (bias, sign)
  write_cr_normal (0x1D, 00 bias sign 0000)
end macro
```

Constants N0, N1 and N2 in the pulse_high_voltage macro ensure that the time constrains for the programming of the flash are respected.

5.2 Programming the whole array (version 1)

This programming algorithm should be used for devices marked XE8851, f XX88LC01-03-05 and for dice delivered devices marked before July 2000.

```
sequence full_programming
  lock_test                          ; initialize programming mode
  write_cr(RegEEP3, 00000000)
  write_cr(RegEEP3, 00000000)
  write_cr(RegEEP3, 00000000)
  write_cr(RegEEP2, 00000000)
  write_cr(RegEEP2, 00000000)
  write_cr(RegEEP1, 11100100)
  write_cr(RegEEP, 00001000)
  wait_cr
  cycle_ptck(1)                      ; erase memory
  pulse_high_voltage (long)
  cycle_ptck(2)
  pulse_high_voltage (long)
  trim_vreg (1,1)
  wait (100 us)
  cycle_ptck(1)
  for address = 0 to 8191            ; write blocking bits
    write_cr(RegEEP2, address_LSB)
    write_cr(RegEEP2, address_MSB)
    cr_wait
    for counter = 0 to 7
      cycle_ptck (1)
      pulse_high_voltage (short)
      cycle_ptck (5)
      pulse_high_voltage (short)
      cycle_ptck (4)
    end for
  end for
```

```
  trim_vreg (1,0)
  wait (200 us)
  for address = 0 to 8191              ; check blocking bits
    write_cr(RegEEP2, address_LSB)
    write_cr(RegEEP2, address_MSB)
    cr_wait
    cycle_ptck (2)
  end for
  trim_vreg (1,1)
  wait (200 us)  ; 13 ms for the prototype on the Starter-kit and ProStart
  for address = 0 to 8191              ; write data in memory
    write_cr(RegEEP2, address_LSB)
    write_cr(RegEEP2, address_MSB)
    write_cr(RegEEP3, data_8_least_significant_bits)
    write_cr(RegEEP3, data_8_next_bits)
    write_cr(RegEEP3, 00 data_6_most_significant_bits)
    wait_cr
    cycle_ptck (1)
    pulse_high_voltage (short)
    cycle_ptck (4)
  end for
  trim_vreg (0,0)
  wait (100 us)  ; 13 ms for the prototype on the Starter-kit and ProStart
  read_cr(RegEEP)                      ; check error bit
end sequence
```

5.3 MTP Registers

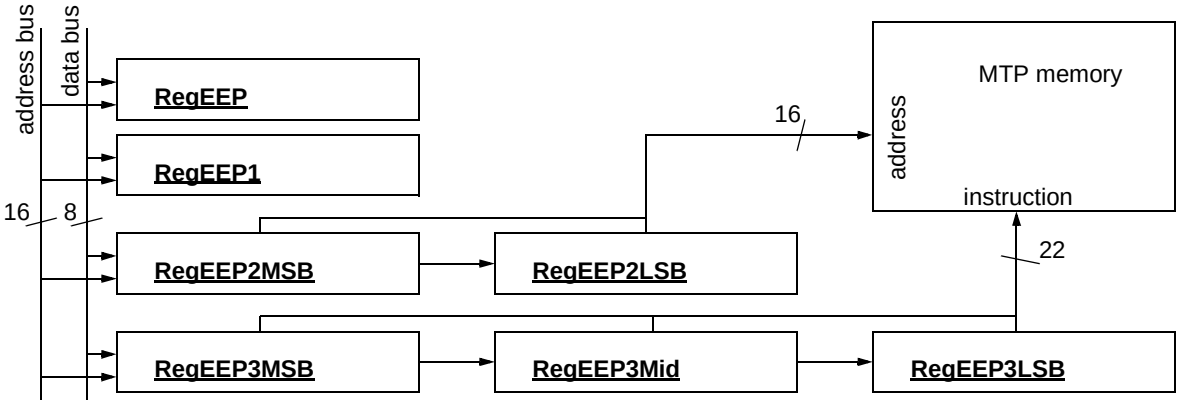
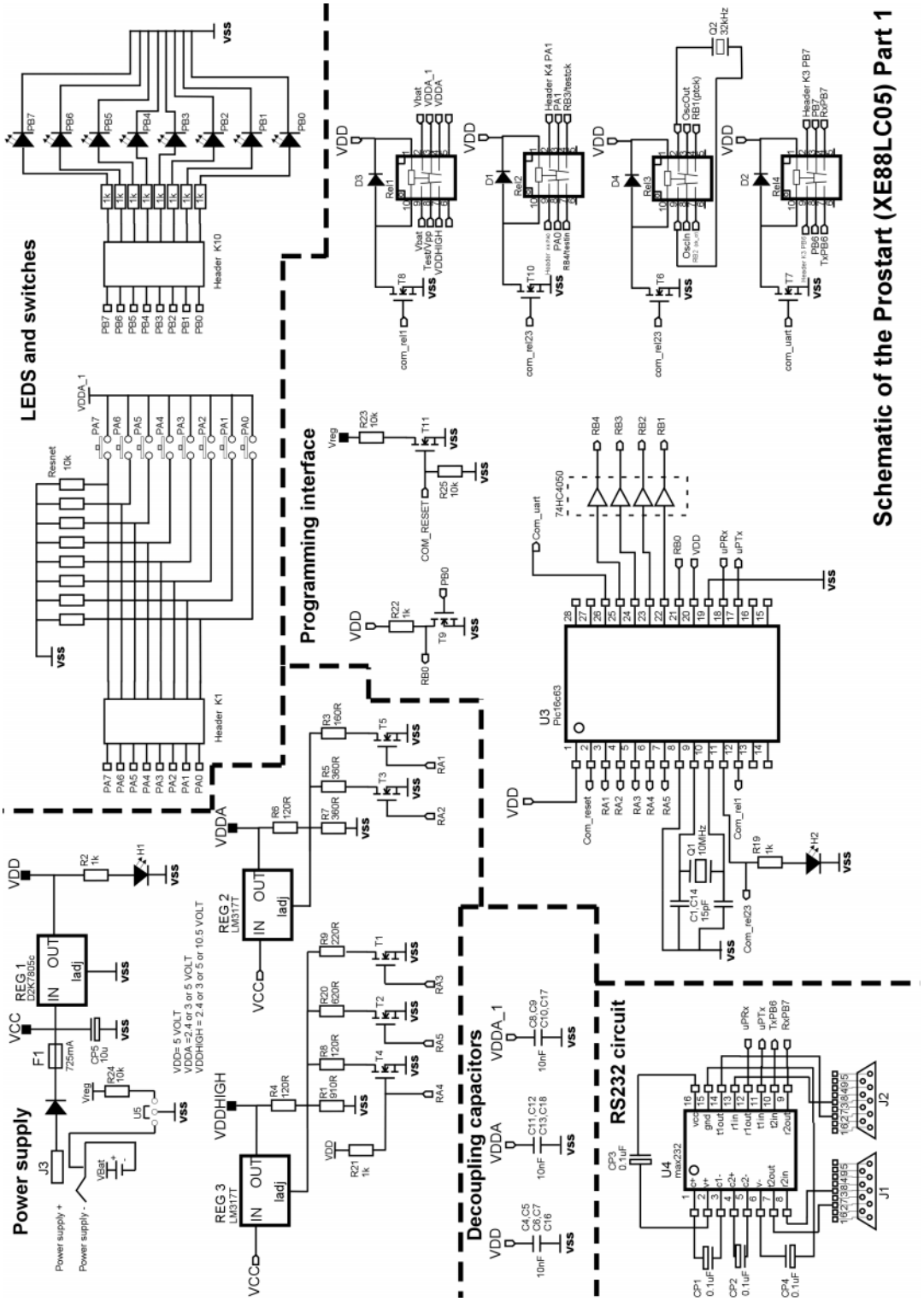
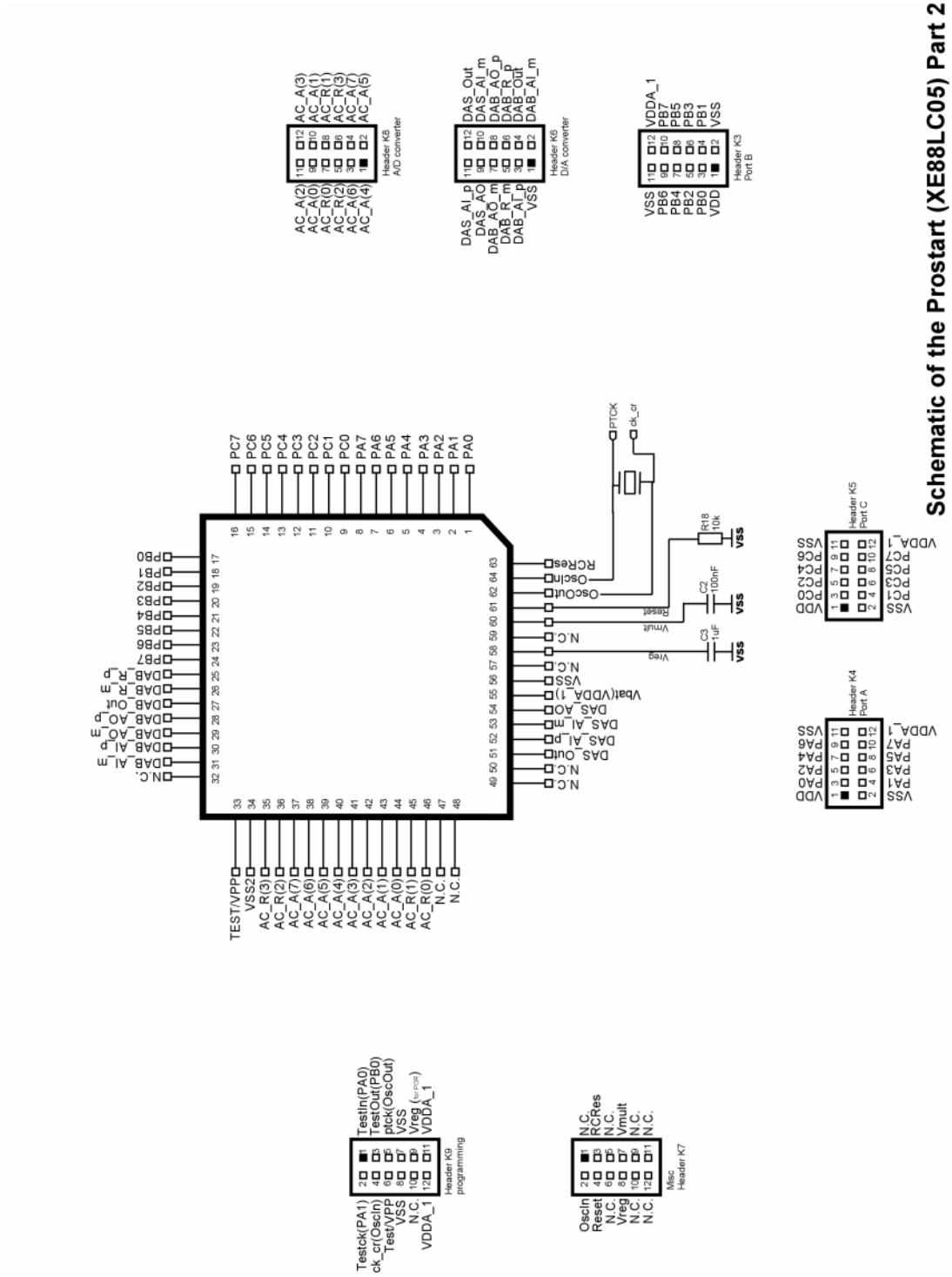


Figure 5.5: MTP registers organization

register name	address
RegEEP	h0038
RegEEP1	h0039
RegEEP2	h003A
RegEEP3	h003B

Table 5.3: MTP Registers

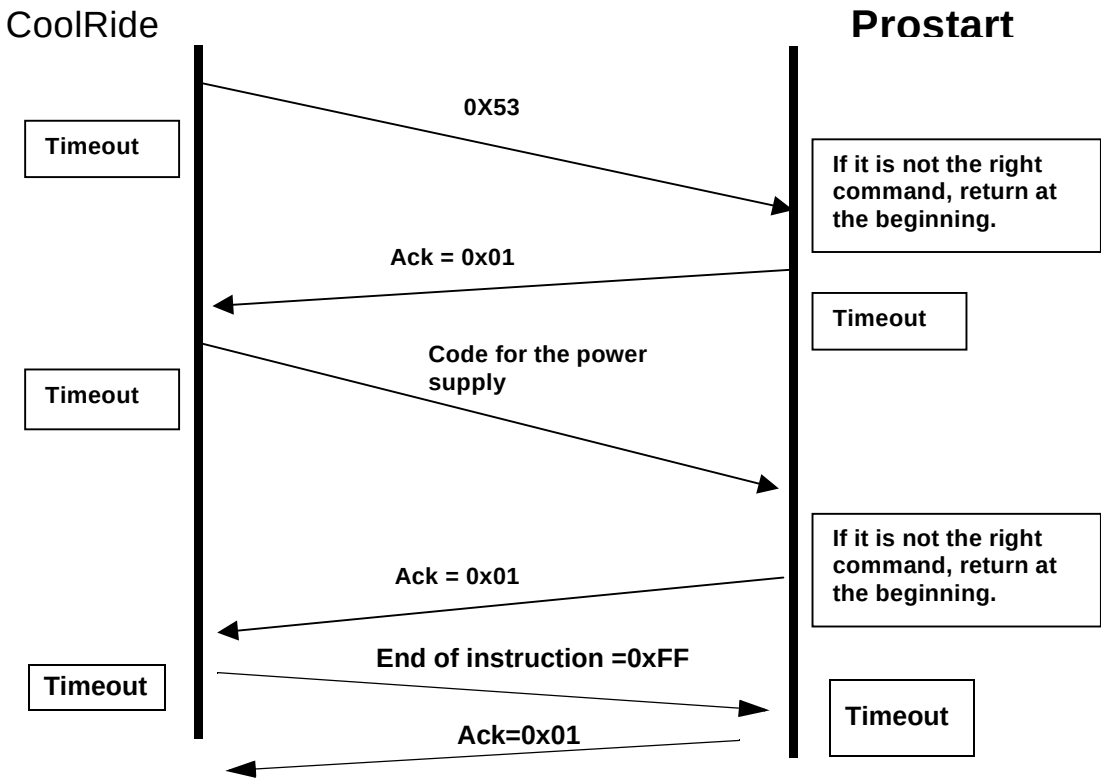




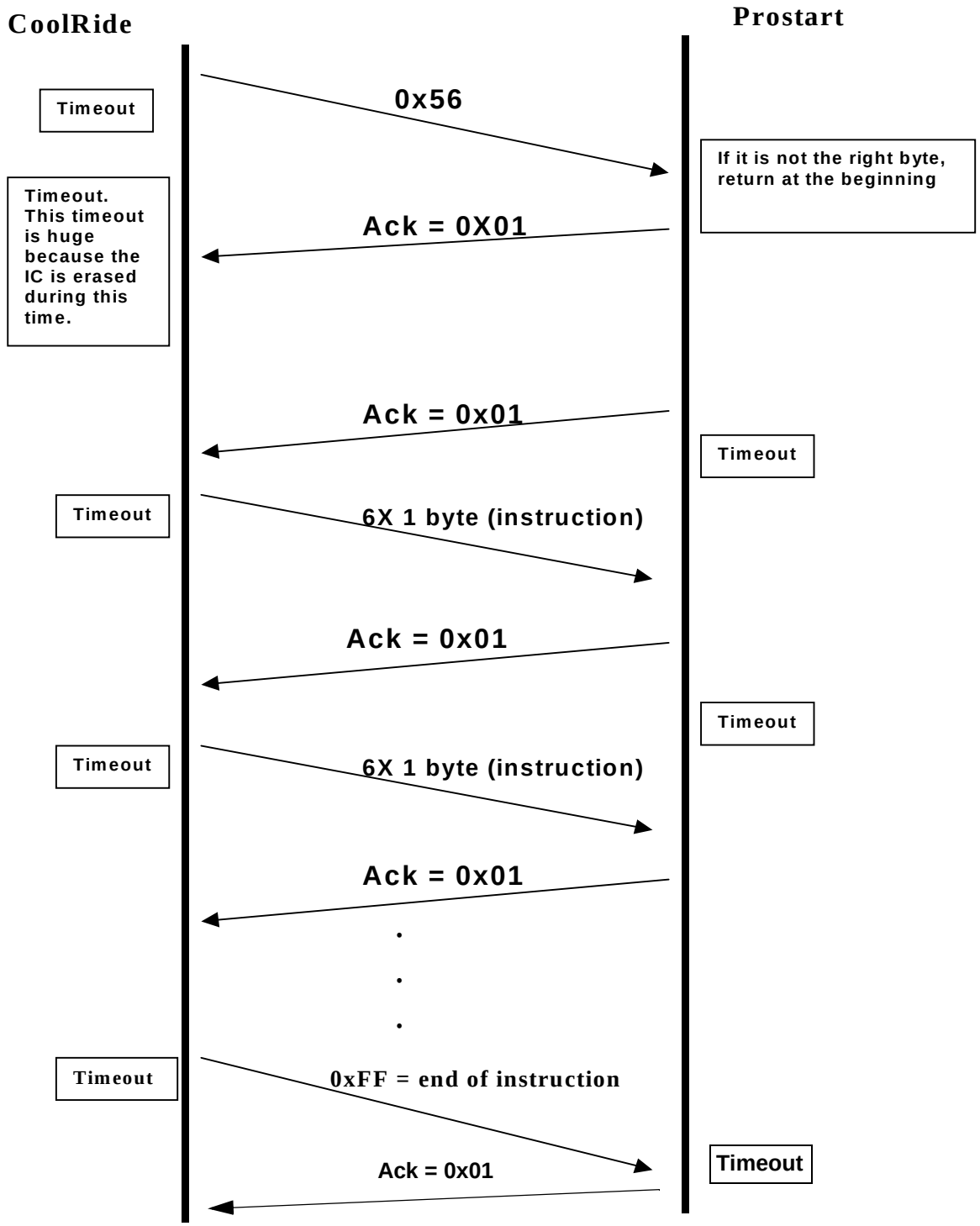
Communication Protocol between CoolRide and the Prostart

The protocol between CoolRide and the Prostart is a simple one. The protocol only uses messages “acknowledges”, which control the rate of the data, as well as the “even parity control” on the bytes.

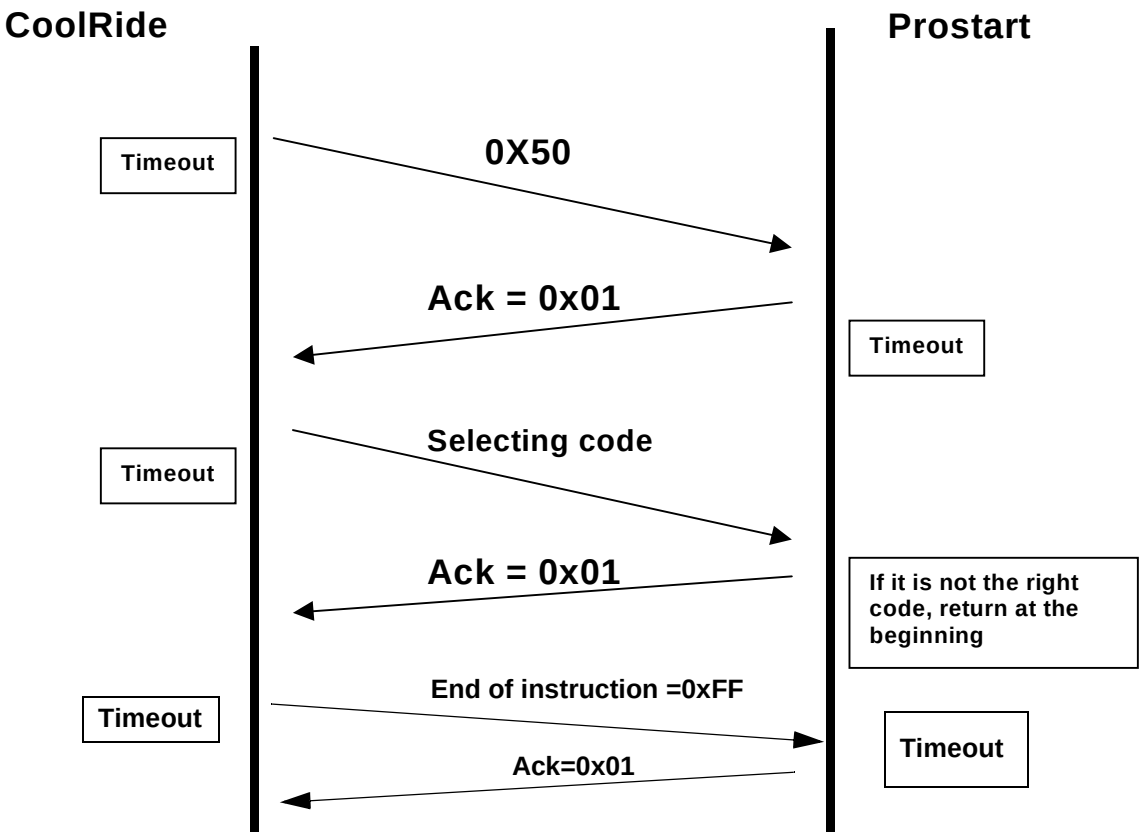
There are only three bytes to begin a communication. The first is 0x53H. This byte allows for a change in the power supply on the Prostart. Then there is three different possibilities:0x30 = 5V, 0x31 = 3V, 0x32 = 2.4V.



The second is 0x56. This byte allows it to program the IC on the Prostart. The data are sent in ASCII. (For example, 0X34A579H => 3 = 0x33 4 = 0x34 A = 0X41 5 =0x35 7 =0x37 9 = 0x39) Six bytes represent a CoolRISC instruction.



The third command is 0x50. This byte allows to select pins 6,7 of the microcontroller on a RS232 connector. These provide two options. First 0x30 = port B normal, second 0x31 = port B on RS232 connector.



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