XEMICS

AN8000.03

Application note

XE8851 DACs usage

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1 Introduction

This application note concerns the XE8851R and XE8851M products.

2 Analog outputs

The PWM DACs available in all XE8000 products are described in the XE8000 series data book, TIMERS chapter.

The XE8851 has two additional digital to analog converters (DAC)s: a signal DAC able to pass a 4 KHz signal with 10 bits precision, and a bias DAC, able to output 10 mA to bias a resistive bridge sensor. Both are DACs formed from a generic DAC and an amplifier. This makes current and voltage drive possible and gives the user freedom to choose the preferred filtering scheme.

2.1 DAC Signal

2.1.1 Application

The DAC signal block described in this document converts a digital signal into an analog output signal (voltage output or 4-20mA loop).

2.1.2 Typical external components

External components are needed for the filtering of the generic DAC output. These external components depend on the characteristics the customer wants to obtain. Some application examples are shown in this document.

External resistors are required to fix the gain of the output amplifier. This gives the user freedom to set the output range of the block within certain limits.

In case the output signal is given through a 4-20mA loop, an external transistor is needed to generate the output current and some resistors to sense the current.

2.1.3 Block diagram

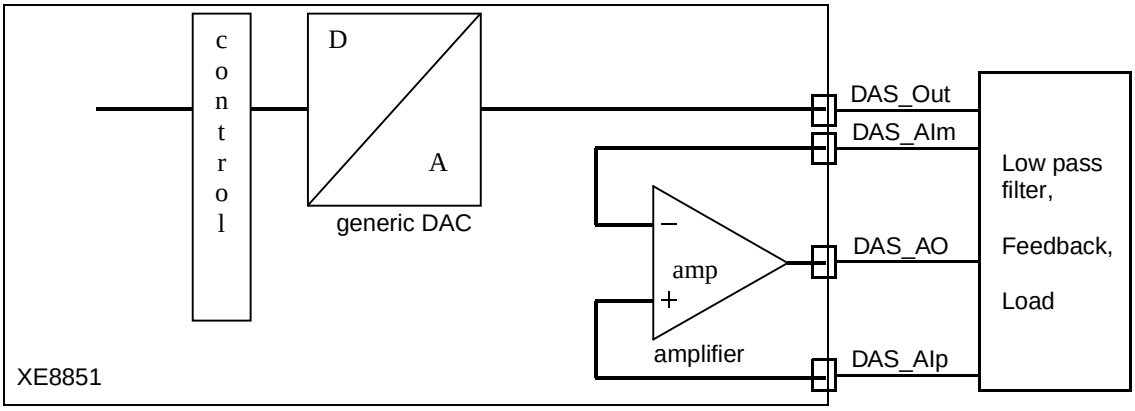

Figure 2.1: General block diagram

Figure 2.1 shows the general block diagram of the peripheral. It consists of a control block that manages all communication with the CPU, sets the configuration of the peripheral and implements the different test modes. The DAC converts the digital data in a PWM output signal. A completely independent amplifier is added. This allows the user to build a low impedance voltage output after the (external, probably passive) filter. It also allows building of a 4-20mA loop. (See amplifier section below for examples)

2.1.4 The generic DAC

The generic DAC block consists of two major parts: the noise shaper and the PWM modulator as shown in Figure 2.2.

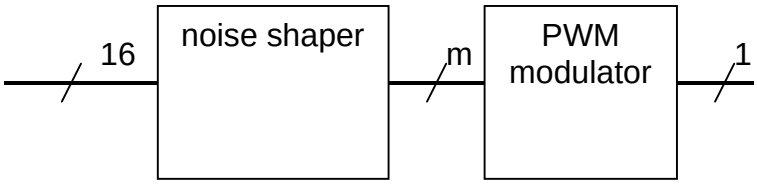

Figure 2.2: The DAC signal structure

The DAC word width on input is 16 bit. If the word is narrower, 0's have to be added after the LSB to fill the 16 bits. To maintain maximum flexibility, the order of the noise shaper and the resolution of the PWM modulation are programmable by writing the codes **code_lmax** and **ns_order** to the configuration register. The possible noise shaper order is 0, 1 or 2. With noise shaper order 0, the generic DAC is a conventional PWM DAC. The possible PWM modulation resolution can be set between 4 and 11.

The purpose of the noise shaper is to increase the DAC resolution by changing the PWM input code such that the mean code is equal to the DAC input code. As an example, the PWM can directly generate codes h8000 and h8020, but not h8010, so if one wants to generate code h8010, the modulator will force PWM to issue alternatively code h8020 and code h8000. As the high frequencies have to be filtered out of the PWM signal, the increase in resolution is made at no extra cost. A first order noise shaper should be used with a first order filter, and a second order noise shaper needs a second order filter.

When using noise shaper, PWM period can be made smaller with same accuracy as without the noise shaper. This increases the system bandwidth accordingly, at the cost of some losses in linearity for full scale signals.

With a first order noise shaper, optimal filtering of the modulation is made with a first order filter, and so resolution is proportional to the number of samples. With a second order noise shaper, optimal filtering is made with a second order filter and so resolution is increasing much faster.

Filter corner frequency must be placed such that it rejects the fundamental frequency below the LSB (worst case is for the code having a duty cycle of 0.5, that is h8000) and that it averages a sufficient number of PWM codes.

One can define the following variables:

1. FC is the DAC main clock frequency
2. PWMresolution is the resolution reached by the PWM without the noise shaper
3. DACresolution is the resolution reached by the DAC
4. FPWM is the frequency associated with the period of the PWM
5. FF1 is the 1st order filter corner frequency required for suppressing the fundamental frequency of the PWM below the DAC resolution
6. FF2 is the 2nd order filter corner frequency required for suppressing the fundamental frequency of the PWM below the DAC resolution

On have the following relations:

1. $FPWM = FC / 2^{PWMresolution}$
2. $FF1 = FPWM / (DACresolution/2 - 1)$
3. $FF2 = FPWM / ((DACresolution/2)^{0.5} - 1)$

Example for reaching 12 bits resolution with a 1 MHz clock and 4 bits on the PWM:
FPWM = 1 MHz / 2^4 = 62.5 kHz
FF1 = 62.5 kHz / (2^12 / 2 - 1) = 30 Hz
FF2 = 62.5 kHz / ((2^12 / 2)^0.5 - 1) = 1.4 kHz

DACs and filter settings are resumed in Table 2.1

noise shaper order	PWM resolution in bits	DAC maximum resolution in bits	PWM sample output rate (1)	low passfilter type	filter corner frequency for maximum resolution (1)	filter corner frequency for 12 bits resolution (1)	filter corner frequency for 8 bits resolution (1)
0	4	4	62.5 kHz	1st order			
0	4	4	62.5 kHz	2nd order			
0	5	5	31 kHz	1st order			
0	11	11	500 Hz	1st order			3.8 Hz
0	11	11	500 Hz	2nd order			47 Hz
1	4	16	62.5 kHz	1st order		30 Hz	490 Hz
1	5	16	31 kHz	1st order		15 Hz	246 Hz
1	11	16	500 Hz	1st order		0.23 Hz	3.8 Hz
2	4	16	62.5 kHz	2nd order		1.4 kHz	6 kHz
2	5	16	31 kHz	2nd order		700 Hz	3 kHz
2	10	16	1 kHz	2nd order		22 Hz	95 Hz
2	11	16	500 Hz	2nd order		11 Hz	47 Hz

Table 2.1: DAC settings examples

Note: 1) For 1MHz main clock

2.1.5 The amplifier

The amplifier can be used in several configurations. Because of this, it is not connected internally. The first possibility is to use a normal voltage output. In this case, the amplifier is set as a normal inverting gain amplifier. It is not recommended to use the amplifier in unity gain configuration. The advantage of inverting the amplifier is that its common mode is fixed at a given voltage. This reduces the non-linearity. The matching between the external resistors setting the gain does not have to be very precise, since errors can be corrected by predistortion of the digital input code written to the A/D by the CPU. Figure 2.3 gives an application example for a voltage output configuration and a first order low pass filter at the PWM output.

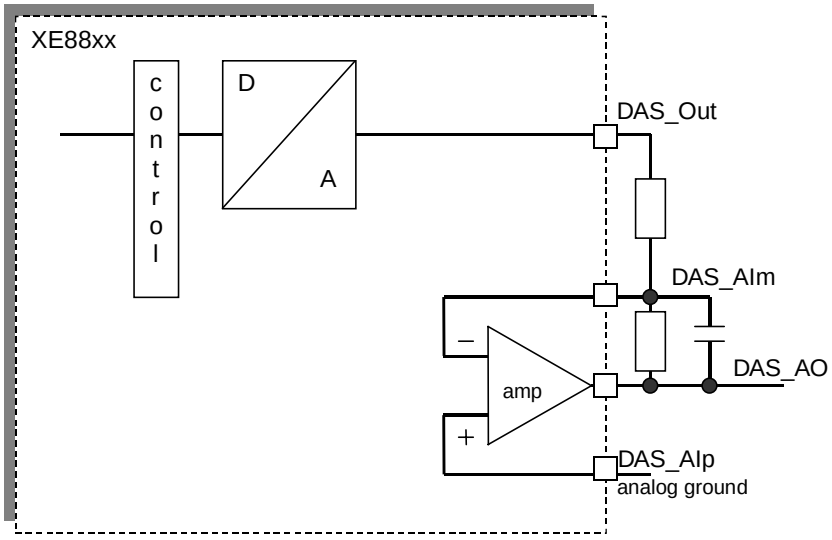

Figure 2.3: Output configuration for a first order low pass filter and voltage output. DAS-AIp must be connected to a voltage source (like a resistive voltage divider between VDD and VSS).

A second possibility is a 4-20mA loop, not including the circuit consumption. In this case an external transistor is needed in order to deliver the required current. Figure 2.4 shows an example of such a configuration with again a first order low pass filter.

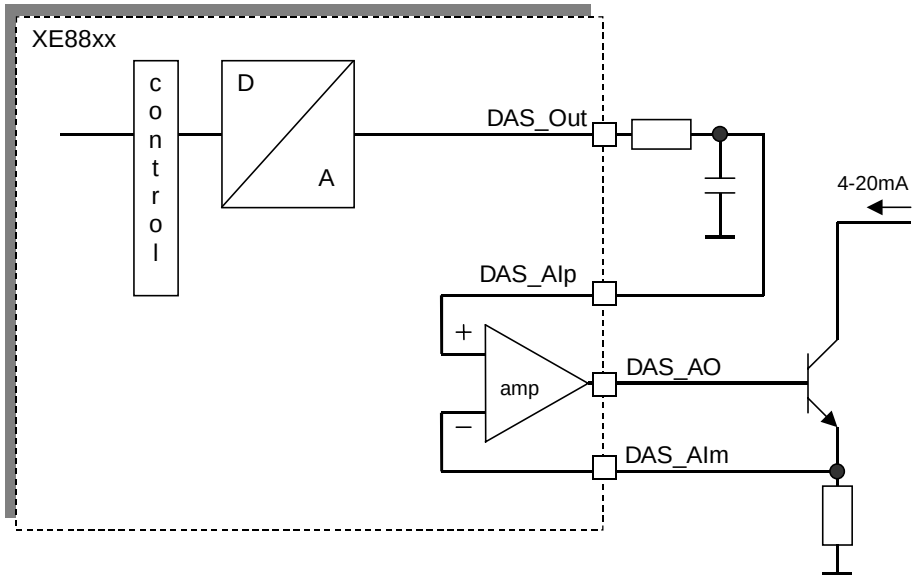

Figure 2.4: 4-20mA loop configuration without the circuit consumption (first order low pass)

Finally, a 4-20mA loop can be build including the consumption of the circuit. In this case the current consumption of the circuit itself has to be included in the sense resistor, while the sense voltage of the amplifier should stay within the supply voltages of the circuit. An example of such a circuit is given in Figure 2.5.

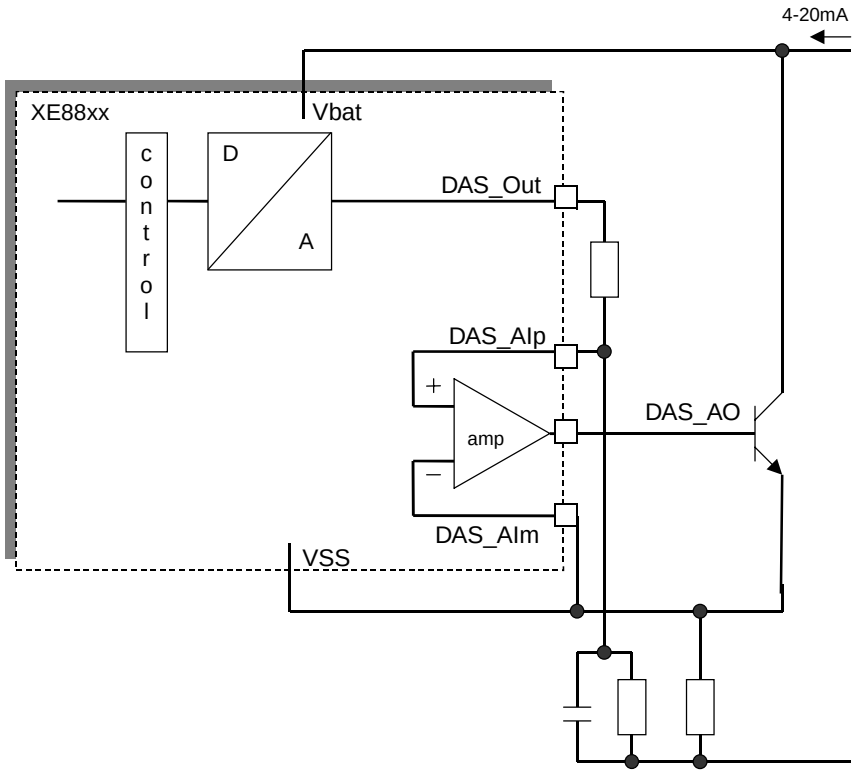

Figure 2.5: 4-20mA loop including the circuit (and bridge) current consumption (first order low pass)

In the case of a 2 wire current loop, the capacitive load of the output amplifier is much smaller than in the case of the voltage output configuration. However, the required bandwidth of the amplifier is higher since it has to be capable to react at all current consumption modifications of the circuit. Therefore, the amplifier bandwidth is made programmable.

sym	description	min	typ	max	unit	Comments
gain	gain at DC	80			dB	1
GBW0	gain bandwidth product	25			kHz	7
cl0	capacitive load			5	nF	7
GBW1	gain bandwidth product	250			kHz	8
cl1	capacitive load			200	pF	8
fm	phase margin	55			°	9
rl	resistive load	5			kohm	6
SR	slew rate	10			kV/s	5
CMR	common mode input range	vss-0.2		vdd-1.2	V	2
OR	output range	vss+0.2		vdd-0.2	V	
voff	offset			±5	mV	
CMRR	common mode rejection	60			dB	3
noise	integrated input noise			100	mVrms	
PSRR	power supply rejection ratio	20			dB	4
ibias	quiescent bias current		200	500	uA	
ioff	off current			1	uA	

Table 2.2: DAC signal amplifier performances

Notes: 1. For the minimal resistive load and the maximal capacitive load

Notes: 2. The amplifier common mode is vss in the 4-20mA loop (Figure 6).
3. At DC
4. At DC. Only a low rejection ratio is needed since the DAC output refers directly to the power supplies.
5.For maximal load cl0, BW=0 and maximal resistive load rl
6. Short circuit protection at ~5mA.
7. GBW when the maximal load is cl0 and with the bit BW=0
8. GBW when the maximal load is cl1 and with the bit BW=1
9. In both cases BW=0 and BW=1 for the maximal capacitive load and the minimal resistive load.

2.1.6 DAC signal registers

register name	address (hex)	comments
RegDasInLsb	H0068	input code (LSB)
RegDasInMsb	H0069	input code (MSB)
RegDasCfg0	H006A	DAC settings
RegDasCfg1	H006B	

Table 2.3: DAC signal registers

bit	name	reset	rw	description
7-6	NsOrder	0 resetsystem	r w	modulator order
5-3	CodeImax	0 resetsystem	r w	PWM resolution
2-1	Enable	0 resetsystem	r w	DAC and buffer enable
0	Fin	0 resetsystem	r w	input frequency selection

Table 2.4: RegDasCfg0

bit	name	reset	rw	description
7-2	reserved	0 resetsystem	r w	
1	BW	0 resetsystem	r w	output bandwidth selection
0	Inv	0 resetsystem	r w	output polarity selection

Table 2.5: RegDasCfg1

The input data will have to be resynchronized with respect to the peripheral clock. To guarantee data integrity, the data will not be copied to the DAC while the interface signal cs is high and readnwrite is low. In order to guarantee the synchronization of the MSB and LSB part of the input data, a validity flag will be reset when the CPU is writing into the LSB register and set again when the CPU is writing to the MSB register. The contents of the registers will not be copied to the DAC while the validity flag is reset. This means that the CPU always has to write the LSB register before writing the MSB register.

The different set-up words (set-up register definition in Table 2.4) are coded as indicated in the tables below.

ns_order(1:0)	Noise shaping order
00	0
01	1
1x	2

Table 2.6: Noise shaping setting

code_Imax	m (PWM resolution in bits)
000	4
001	5
010	6
011	7
100	8
101	9
110	10

Table 2.7: PWM setting

code_lmax	m (PWM resolution in bits)
111	11

Table 2.7: PWM setting

enable(1:0)	Peripheral status
00	DAC: switched off; Amplifier switched off
01	DAC: normal operation; Amplifier: switched off
10	DAC: switched off; Amplifier: normal operation
11	normal operation

Table 2.8: DAC status

The **Fin** bit allows the choice between two clock inputs that can be connected in two different places of the prescaler of the XE8000.

fin	used clock input	input clock frequency for RC at 1MHz
0	ckRC	1 MHz
1	ck500k	500 kHz

Table 2.9: Clock setting

Finally, the **inv** bit indicates if the PWM output pulse is active low or active high. This makes possible the use of the output amplifier in an inverting (e.g. in Figure 2.3) or not inverting configuration (e.g. in Figure 2.4).

inv	PWM pulse
0	active high
1	active low

Table 2.10: PWM polarity

2.2 DAC bias

2.2.1 Application

The DAC_bias block described in this document converts a digital signal into an analog output signal in DC. It can be used to bias resistive sensors. In some cases it could also be used to do a rough offset calibration of a resistive bridge.

2.2.2 Typical external components

No other external devices are needed in case of voltage controlled bridge bias. An additional resistor is needed for current controlled bridge bias.

2.2.3 Block diagram

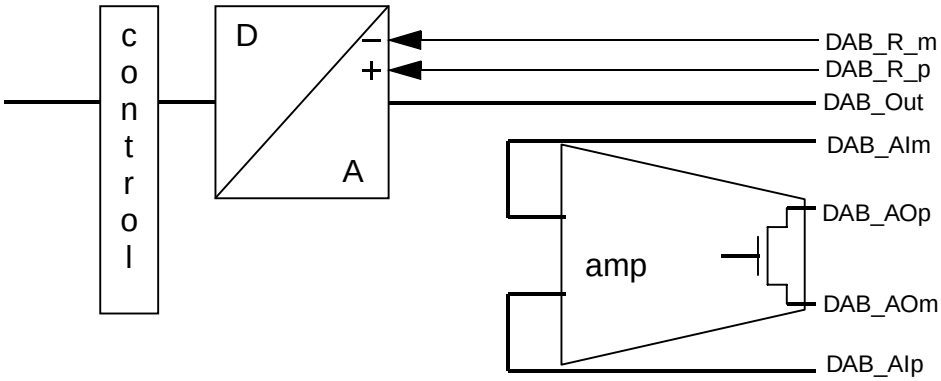

Figure 2.6: General block diagram

Figure 2.6 shows the general block diagram of the peripheral. It consists of a control block that manages all communication with the CPU, sets the configuration of the peripheral and implements the different test modes. The DAC converts the digital data in an analog output signal. An amplifier is added in order to be able to deliver large currents.

2.2.4 The DAC

The DAC convertor is a resistive divider connected between pads DAB_R_m and DAB_R_p.

sym	description	min	typ	max	unit	Comments
wda	number of input bits		8		bits	
tstep	step response			100	ms	1
range	DAC output range	DAB_R_m		DAB_R_p		2

Table 2.11: DAC performances

Notes: 1) Time to reach the final value within 5%.
2) In most cases DAB_R_m will be connected to vss and DAB_R_p to vdd.

2.2.5 The amplifier

The amplifier can be used in several configurations for biasing a bridge in voltage or current. Application examples are given in the following figures. Figure 2.7 shows a configuration for the voltage biased bridge. Figure 2.8 shows a configuration for a current biased bridge.

sym	description	min	typ	max	unit	Comments
gain	gain at DC	60			dB	1
GBW	gain bandwidth product	100			Hz	1
fm	phase margin	60			°	1
rl	resistive load	300		100000	ohm	5,6
cl	capacitive load			1	nF	
CMR	common mode input range	vss		vdd	V	
OR	output range	vss+0.2		vdd-0.2	V	3,4
outp vr	outp pin voltage range	vss+2.3		vdd	V	
voff	offset			±10	mV	
noise	integrated input noise			100	uVrms	
isourc	max source current			10	mA	
PSRR	power supply rejection ratio	40			dB	2
ibias	quiescent bias current		2	5	uA	6
ioff	off current			1	uA	

Table 2.12: Amplifier performances

Note: 1) For all possible combinations of resistive load and capacitive load.
Note: 2) At DC.
Note: 3) For voltage controlled bias control. For current controlled operation the voltage drop on the pMOS output transistor has to be less than 200mV at maximum current.
Note: 4) Special analog output pads without series resistor will be needed in order to get the specification. Care has to be taken with the layout so that ESD and latchup specifications can be met.
Note: 5) Short circuit protection at ~80mA.
Note: 6) This amplifier must be loaded for correct operation. Ibias is without load current.

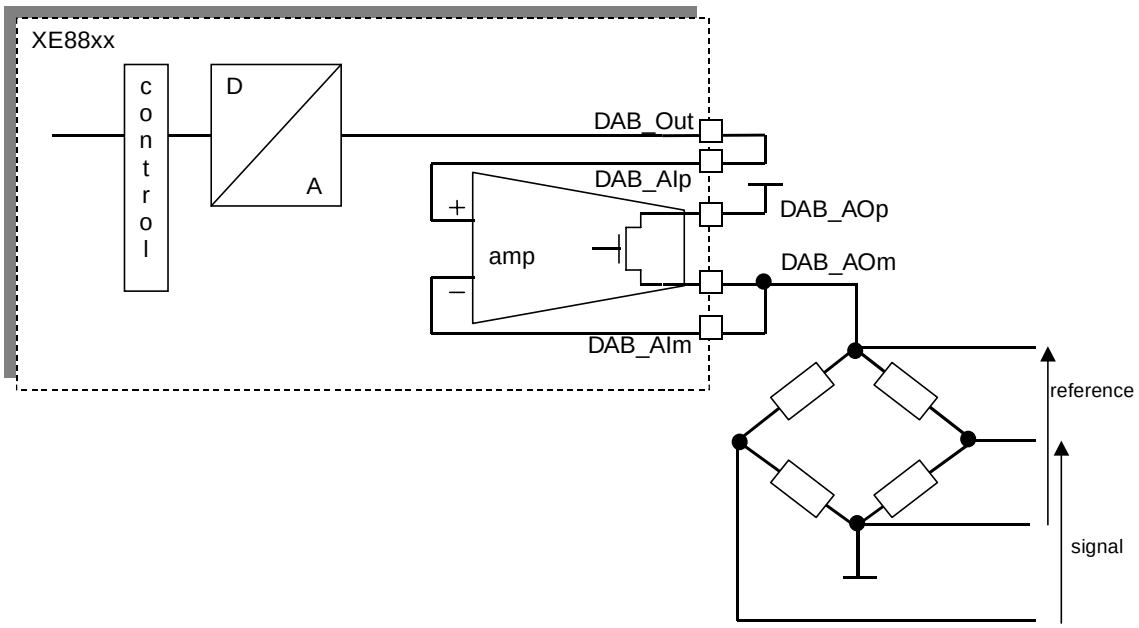

Figure 2.7: Voltage controlled bridge bias

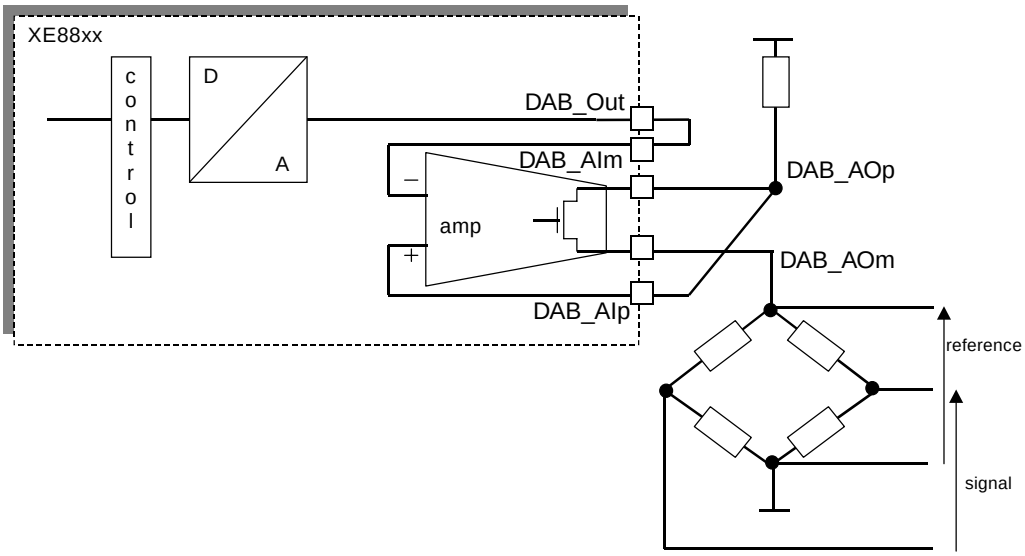

Figure 2.8: Current controlled bridge bias

2.2.6 DAC bias registers

register name	address (hex)	comments
RegDab1In	H006C	input code
RegDab1Cfg	H006D	DAC settings

Table 2.13: DAC bias registers

enable(1:0)	Peripheral status
00	DAC disabled, amplifier disabled
01	DAC: normal operation; Amplifier: switched off
10	DAC: switched off; Amplifier: normal operation
11	DAC: enabled; Amplifier: enabled

Table 2.14: RegDab1Cfg

A904-043 - AN8000.03 Application Note: XE8851 DACs usage

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