

CooLIB 4.1™

Standard ultra low power cell library, SRAMs & ROMs for digital low power designs

General Description

CooLIB 4.1 is the latest version to the CooLIB low power standard cell library. The CooLIB 4.1 enables substantial power savings in its IC designs by creating up to 3x power reduction when used at nominal voltages, and/or 9x power reduction when using low voltages. CooLIB 4.1 is ported on the world's most advanced deep sub-micron IC fabs.

Key Product Features

- 179 Standard cells
- Low voltage operation (down to 1.0V)
- Cells designed in "Branch-Based-Logic" style
- 3 X Power reduction at 3.3V
- 9 X Power reduction at 1.2V
- Ported on TSMC 0.5μ, 0.35μ, 0.25μ
- Ported on Tower 0.5μ
- <6nW/MHz/Gate (TSMC0.25μ/1.2V/27°C@10%)
- Combinatorial and memory cells, complex gates

Memory Features

The CooLIB 4.1 is equipped with a low power RAM / ROM generator enabling custom size memories.

Single port RAM:

- Common or separate data bus
- Up to 64K x 64-bits
- Global and local decoding to reduce switching

ROM:

- Common or separate data bus
- 256K x up to 1024-bit words
- Single or dual phase pre-charge
- Programmable in metal, diffusion or mask

Power Consumption, Size and Timings

Cell	Area [μm ²]	Power [nW/MHz]	Propagation Delay [ns]
DFF	207	132	1.2
NAND2	35	102	1.1
Full-Adder	173	110	1.5
Inverter	25	100	0.7

VDD = 1.8V; Temp. = 25°C; Input Slew = 1ns; Load = 0.1pF Technology = TSMC 0.25μ; Process = Typical.

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IP Deliverables

CooLIB 4.1 has been developed to match the industry's leading design tools.

Simulation models: VHDL/VITAL, Verilog

Synthesis: Synopsis

Symbols: Cadence, Mentor, Synopsis

Placement & Route: Cadence, Mentor

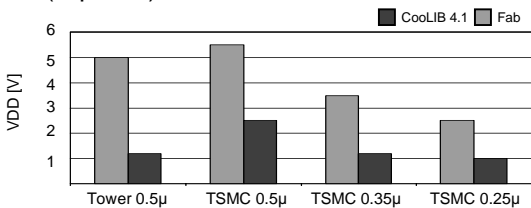
Net-list: SPICE, Eldo

Back-end: GDSII

Documentation: Datasheets with schematics, cell area, pins, delays and power consumption information.

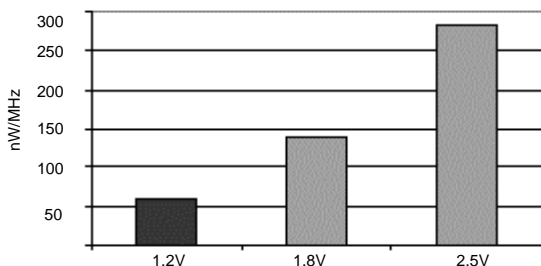
Ultra low voltage

For ultra low voltage battery operated products, CooLIB 4.1 can be characterized at different supply voltages. The characterization can start from $\text{Max}(V_{tp}, V_{tn}) + 200\text{mV}$



Ultra low power

The CooLIB 4.1 has been optimized for low power. Its highly compact layout structures produce gates that are up to 20% smaller than comparable libraries. Techniques were applied to improve speed and reduce overall capacitance. At 1.2V/27°C/TSMC0.25µ/10% activity, CooLIB 4.1 scores just below 6nW/MHz/gate



Applications

The CooLIB 4.1 is used internally to develop state of the art ultra low voltage and ultra low power products. CooLIB 4.1 is available in various technologies and processes. Other library developments can be made to order.

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Low Power Standard Cell Library

COMBINATORIAL CELLS*:

ARITHMETIC: (2 FUNCTIONS; 6 CELLS)

1-bit full adder (3)

1-bit incrementor (3)

BUFFERS: (4 FUNCTIONS; 26 CELLS)

inverter (4)

non-inverter, (6)

symmetric non-inverter for 2.2V (6)

tristate inverter (4)

tristate non-inverter (6)

COMPLEX GATES: (13 FUNCTIONS; 45 CELLS)

and 2 inputs, nor 2 inputs (3)

and 3 inputs, nor 2 inputs (3)

and 2 inputs, nor 3 inputs (3)

and 2 inputs, or 2 inputs (4)

and 3 inputs, or 2 inputs (4)

and 2 inputs, or 3 inputs (4)

or 2 inputs, and 2 inputs (4)

or 3 inputs, and 2 inputs (4)

or 2 inputs, and 3 inputs (4)

or 2 inputs, nand 2 inputs (3)

or 3 inputs, nand 2 inputs (3)

or 2 inputs, nand 3 inputs (3)

majority function (2/3) (3)

DECODERS: (1 FUNCTIONS; 3 CELLS)

decoder 2:4 output inverted (3)

MULTIPLEXERS: (4 FUNCTIONS; 13 CELLS)

mux 2:1 (4)

mux 2:1 output inverted (3)

mux 2:1 input 0 inverted (3)

mux 2:1 input 1 inverted (3)

SIMPLE GATES: (14 FUNCTIONS; 46 CELLS)

and 2 inputs (4)

and 3 inputs (4)

nand 2 inputs (3)

nand 3 inputs (3)

nand 2 inputs, 1 inverted input (3)

nand 3 inputs, 1 inverted input (3)

nor 2 inputs (3)

nor 3 inputs (3)

or 2 inputs (4)

or 3 inputs (4)

or 2 inputs, 1 input inverted (3)

or 3 inputs, 1 input inverted (3)

xor 2 inputs (3)

xnor 2 inputs (3)

MEMORY CELLS*:

DFFLIP-FLOPS: (4 FUNCTIONS; 16 CELLS)

d-flip-flop neg. edge, preset and clear (4)

d-flip-flop neg. edge, clear (4)

d-flip-flop neg. edge, preset (4)

d-flip-flop neg. edge (4)

LATCHES: (6 FUNCTIONS; 24 CELLS)

latch enable high, preset, clear (4)

latch enable high, preset (4)

latch enable high, clear (4)

latch enable high (4)

latch enable low, clear (4)

latch enable low (4)

TOTAL MEMORY: 10 FUNCTIONS; 40 CELLS

TOTAL COMBINATORIAL: 38 FUNCTIONS; 139 CELLS

TOTAL LOW POWER LIBRARY: 48 FUNCTIONS; 179 CELLS

*Numbers in () represent the number of different strengths for each function

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