Application Note
ADC20013
Broadcast Satellite Tuner MMIC
Rev 1

INTRODUCTION

The ADC20013 downconverter is intended for use in the indoor receiver portion of the DBS (Direct Broadcast Satellite) System. ANADIGICS' 0.5 μm. depletion-mode GaAs process is used to fabricate this device. The chip downconverts inputs in the 950-2050 MHz band to a fixed IF at 480 MHz. The device typically dissipates 300 mW from a standard 16 pin SOIC surface mount package. The ADC20013 ushers in a new era in low cost MMIC applications for consumer electronics.

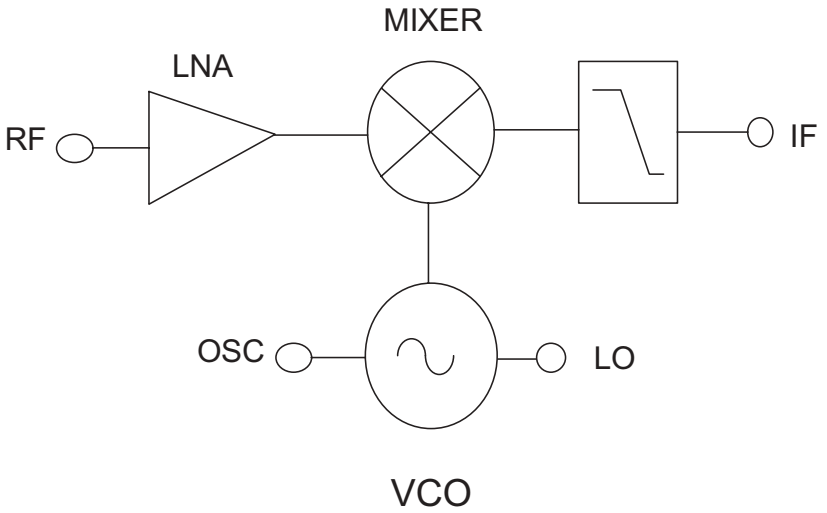


Figure 1: BS Tuner IC Block Diagram

FUNCTIONAL DESCRIPTION

A functional block diagram of the downconverter is shown in Figure 1. The chip is comprised of three basic elements: a single-stage LNA, a mixer, and a VCO. In addition, there is an IF filter which provides some degree of RF & LO rejection. Gain is typically distributed within the device as follows:

LNA	13	dB
Mixer	-2	dB
Filter	-1	dB
Total	10	dB

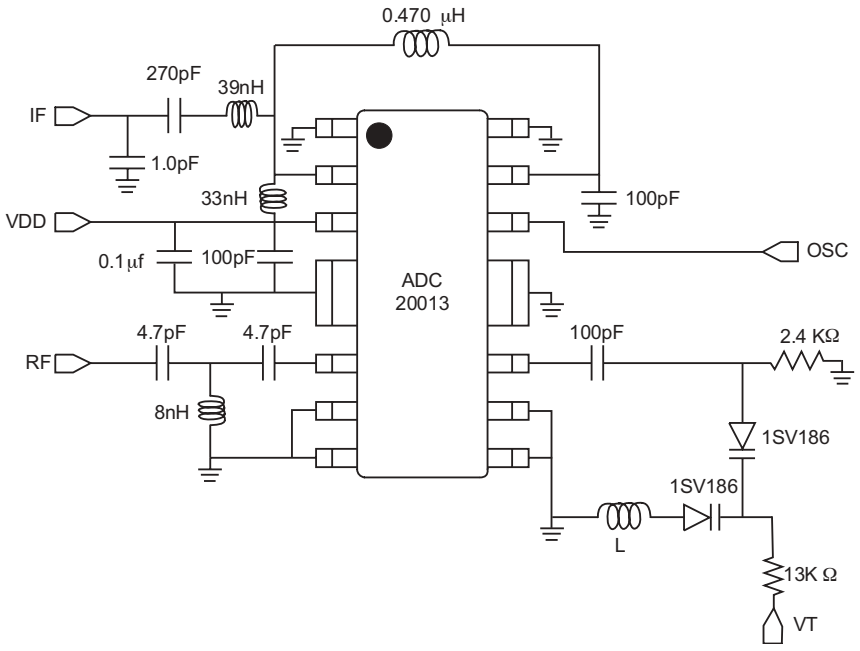


Figure 2: External Circuit Configuration

USING THE IC

The external circuit configuration is shown in Figure 2. It consists of bypass capacitors, a high pass filter, resonator circuit and output matching circuit. All capacitors must be of good RF quality, and bypass capacitors should be placed as close to the supply pins of the device as possible.

The position of the 100 pF bypass capacitor at pin 3 can be varied to optimize the gain performance at 950 MHz. Since the exact position of the capacitor will vary depending on the circuit layout, some initial tuning will be required.

Moving the capacitor closer to or further from pin 3 changes the series inductance between the capacitor and the device, which could affect the LO frequency response. When the optimal position for the capacitor is being determined, the LO frequency response should be carefully evaluated.

The high pass filter should be placed as close to the RF input pin of the IC as possible. This 3 pole high pass filter serves two functions. First, it prevents IF noise from reaching the RF input of the device. Secondly, it provides a capacitive impedance at the IF frequency, which is essential for good noise performance.

The resonator may consist of either one or two varactors, depending on the application. A single varactor resonator provides ample tuning range for applications in the 950-1750 MHz RF band (Figure 3A).

However, for the broadband 950-2050 MHz applications, a dual varactor resonator is required (Figure 3B).

ELECTRICAL CHARACTERISTICS

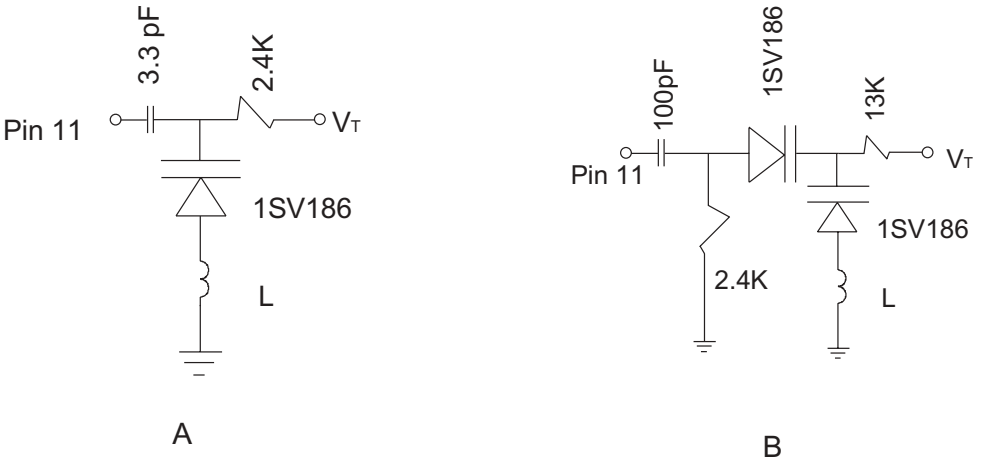


Figure 3: Resonator Implementation

The location of the varactor(s) relative to the local oscillator port (pin 11) of the MMIC is important for proper tuning range and frequency. Moving the varactor farther away from the LO port of the device increases the inductance which lowers the LO frequency and causes the tuning range to increase. Similarly, the opposite effect occurs when the varactor is moved closer to the LO port. It is therefore recommended that this position be optimized for the application at hand.

Note that the appropriate series inductance, L, must be determined and is typically in the range of 2-3 nH. The Toshiba 1SV186 is recommended for use with this downconverter.

As with all RF circuits, good RF grounding is important to the proper operation of the device. Via holes to a backside ground plane should be positioned directly beneath ground pins 1,4,5,7-10, 12,13 and 16.

OUTPUT MATCHING CIRCUIT

The IF output circuit shown in Figure 2 serves three purposes. First, it gives approximately 4 dB improvement in conversion gain by matching the output of the device at 480 MHz. Other IF frequencies can be matched by using the Smith Chart data shown on the data sheet. Secondly, the circuit makes the device less sensitive to load pulling. The device may oscillate without this circuit, depending on the load presented at the output. The third benefit provided is additional RF and LO rejection at the IF port.

Ideally, the frequency response of the circuit should peak at 480 MHz and decrease monotonically at all other frequencies (See Figure 4A). Peaks in the response at other frequencies between 480 MHz and 3 GHz can cause nulls in the LO frequency response. (See Figure 4B). Proper component selection is necessary to preclude the occurrence of this problem. Quality RF components that have high self resonant frequencies and low parasitics should be chosen. Surface mount inductors made by Coilcraft (Cray, Illinois) have such properties. The part number for the 33 nH inductor is 0805CS-330-XMBC, and 0805CS-390-XMBC for the 39 nH inductor. Air wound coils can also be used.

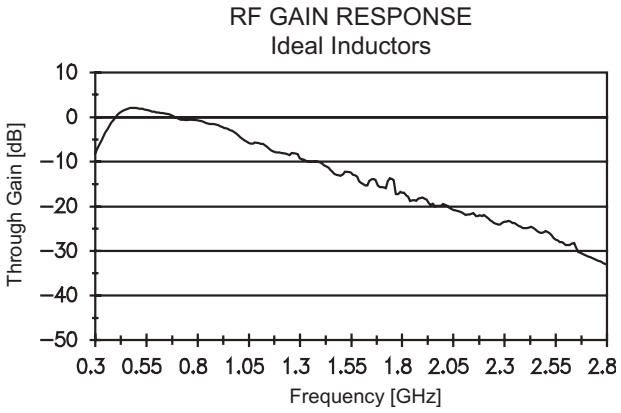


Figure 4A

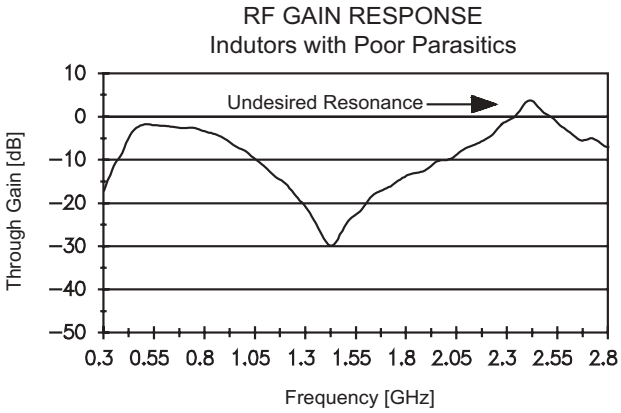


Figure 4B

BIASING PRECAUTIONS

The device is based on a 0.5μm MESFET process, and as a result, generally accepted electrostatic discharge (ESD) and over voltage precautions are essential in the handling and biasing of the chip.

It is recommended that the runs to the bias pins include 0.01 μF bypass capacitors to ground, placed as close to the device package pins as possible. Additionally, a 7V zener diode on the positive supplies can provide added protection.

Additional precautions recommended during testing are as follows:

Voltage overshoots above + 8 Volts and - 8 Volts should be avoided. This includes any large transient 'kicks' that can very easily be induced by removing and reattaching leads with power on. If the device must be powered by long leads from bench power supplies, be sure the power supplies are zeroed before turning them ON/OFF.

Device failures could be induced by simply shorting a supply pin to ground (sometimes done accidentally when 'turning' or manipulating parts with tweezers). Although the short to ground in itself does no harm to the device, the large voltage spike that is induced when

the short is removed certainly does. The source of this large voltage, estimated to be as high as 10000 Volts, is the stored energy in the power supply leads. There is sufficient inductance and often sufficient short circuit power supply current, for Ldi/dt to exceed 10Kv - enough to damage any microwave FET's gate. We have noticed that failures are very infrequent if coax or twisted wire pairs for power lines are used in experimental set-ups.

Standard ESD prevention techniques should be followed. A wrist strap is certainly an adequate protection against static build up, particularly in dry weather. Antistatic mats on work benches are recommended. In work areas, besides wrist straps and antistatic mats, well grounded soldering irons should be used; in fact, any tool that can come in contact with semiconductor device leads should have a discharge path to ground.

INTEGRATING THE IC

A typical tuner front end is shown in Figure 5A. A tracking lowpass filter is used to complete the RF section. The tracking lowpass filter is recommended because it provides lower loss than a tracking bandpass filter, eliminates image noise, and reduces LO leakage levels at the RF input (tuner). The tracking filter shown in Figure 5A typically has less than 3 db of insertion loss while providing better than 15 db of LO rejection.

TRACKING BANDPASS FILTER

While a tracking lowpass filter has less insertion loss and uses fewer components, a tracking bandpass filter is ideal for wider bandwidth applications. A properly designed bandpass filter will give good LO and image rejection, while reducing both harmonic distortion and second order intermodulation distortion. Such a filter is shown in Figure 5B. Using this filter eliminates the need for the highpass filter normally used with the device. It is important, however, to use a dc block between the output of the filter and the input of the downconverter. A nominal value for the dc block is 680 pF.

The circuit, which uses four Toshiba 1SV245 varactors with a coupled line section, has a typical tuning range of 950 MHz to 2050 MHz for a voltage range of 1 to 20 volts. The insertion loss varies from 6dB at the low end of the RF band to 2.5 dB at the high end. LO rejection is between 25 and 30 dB, while image rejection is better then 30 dB.

A printed circuit board layout for the bandpass filter is shown in Figure 5C. Although the length of the coupled section (L in Fig 5B) is nominally 0.350 inch, some tuning will be required to optimize the response. The filter is fabricated on 0.032 inch thick FR4 material, with a relative dielectric constant of 4.8. Other substrates can be used if the microstrip lines and spacings are scaled accordingly.

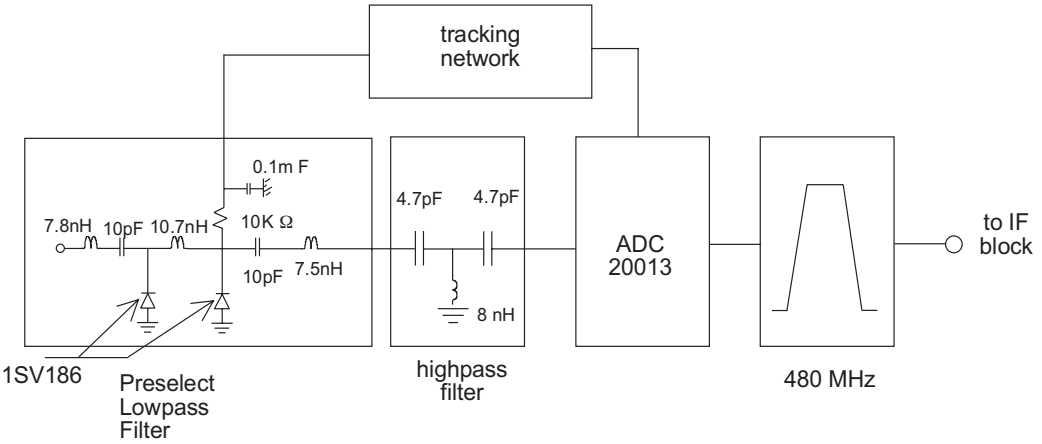
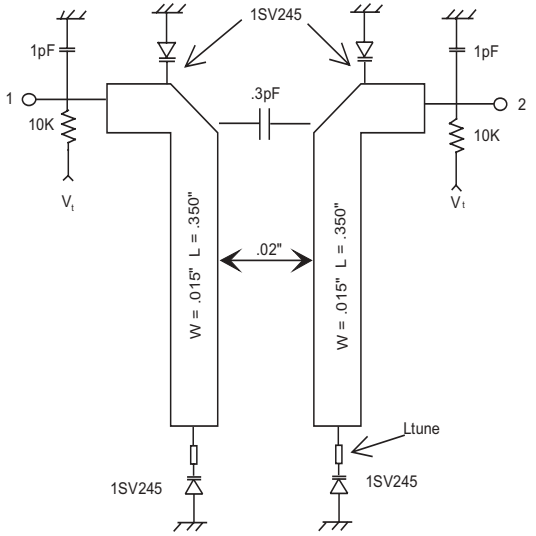
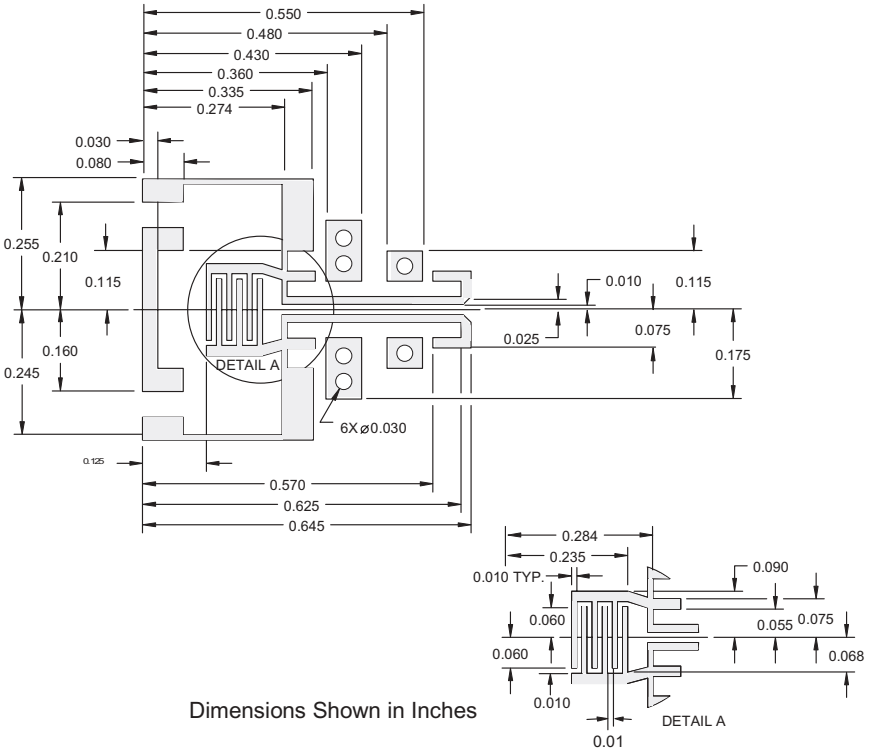


Figure 5A: BS Tuner RF Front End



Dimensions Shown in Inches

Figure 5B: Tracking Filter



Dimensions Shown in Inches

Figure 5C

RECOMMENDED LAYOUT

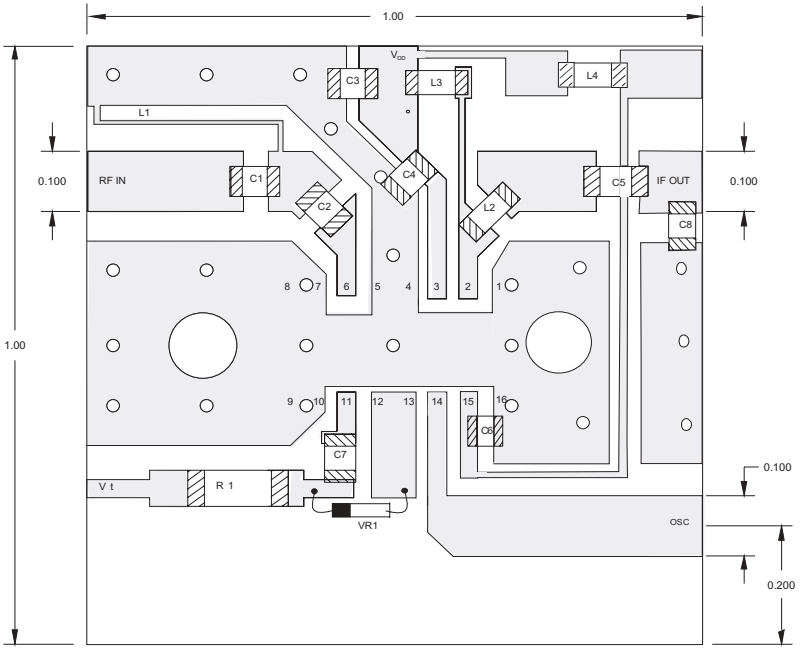
Recommended layouts showing component placement for the ADC20013 using a single varactor diode and dual varactor diode tuning circuit are shown in Figures 6A and 6B, respectively. The layout includes the recommended highpass filter and the output matching circuit.

TEST AND MEASUREMENT

Figure 7A & B shows ANADIGICS' typical test setups for gain, noise figure, LO phase noise, LO to RF leakage, LO output power (prescalar), and IMD3 .

Be sure to follow the recommended procedure under "Biasing Precautions" when testing the IC. Failure to do so may result in damage to the device.

It is important to use only linear power supplies with low ripple content when making oscillator phase noise measurements. Switch mode power supplies may create sidebands or modulation of the oscillator.

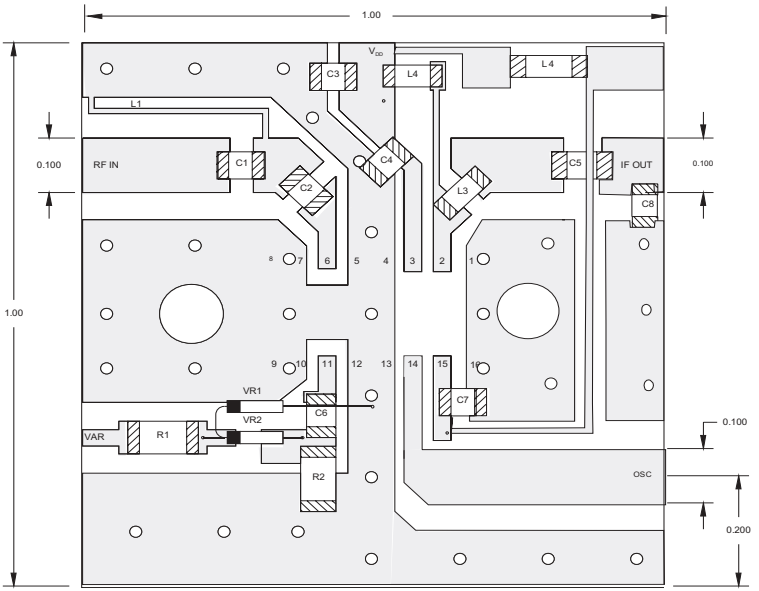


ADC20014S3C EXTERNAL CIRCUIT LAYOUT

PARTS LIST		
SYMBOL	DESCRIPTION	PART NO.
C1,C2	4.7 pF CHIP CAPACITOR	VJ0805A4R7DXA
C3	0.1 μF CHIP CAPACITOR	200B104KCA50X
C4,C6	100 pF CHIP CAPACITOR	VJ0805A101JXA
C5	270 pF CHIP CAPACITOR	VJ0805A271JXA
C7	3.3 pF CHIP CAPACITOR	VJ0805A3R3DXA
C8	1 pF CHIP CAPACITOR	V30805AIR0DXA
VR1	VARACTOR	1SV186
R1	2.4 KΩ CHIP RESISTOR	ER5-8GEY-J242
L1	8nH PRINTED INDUCTOR	NA
L2	39 nH INDUCTOR	0805CS-390-XMBC
L3	33 nH INDUCTOR	0805CS-330-XMBC
L4	0.470 μH INDUCTOR	380NB-R47M

NOTES:
1. SCALE 5:1
2. COMPONENTS NOT TO SCALE
3. SUBSTRATE MATERIAL: FR4 Er 4.8
   TAN δ = 0.020 AT 1 MHz
4. SUBSTRATE THICKNESS: 0.062
5. DIMENSIONS IN INCHES

Figure 6A



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C4,C6 C7	100 pF CHIP CAPACITOR	VJ0805A101JXA
C5	270 pF CHIP CAPACITOR	VJ0805A271JXA
C8	1 pF CHIP CAPACITOR	V30805AIR0DXA
VR1,VR2	VARACTOR	1SV186
R1	13 KΩ CHIP RESISTOR	ER5-8GEY-J133
R2	2.4 KΩ CHIP RESISTOR	ER5-8GEY-J242
L1	8nH PRINTED INDUCTOR	NA
L2	~ 0.3 μH INDUCTOR 2 TURNS, 28 GAUGE WIRE FAIR-RITE BEAD	2643001501 00000
L3	39 nH INDUCTOR	0805CS-390-XMBC
L4	33 nH INDUCTOR	0805CS-330-XMBC

NOTES:

1. SCALE 5:1
2. COMPONENTS NOT TO SCALE
3. SUBSTRATE MATERIAL: FR4 Er 4.8
   TAN δ = 0.020 AT 1 MHz
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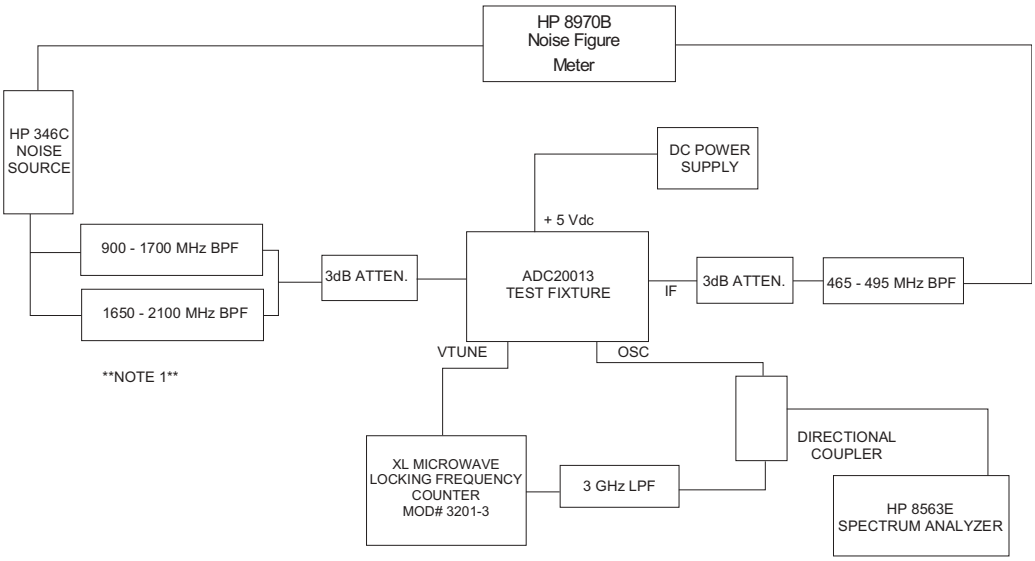
5. DIMENSIONS IN INCHES

Figure 6B



NOTE 1: ONLY ONE FILTER IS USED DEPENDING ON RF FREQUENCY

Figure 7A

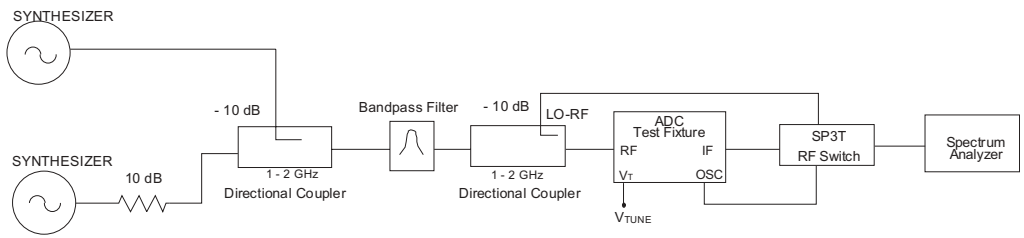


Figure 7B

USING AN EXTERNAL OSCILLATOR

While the ADC offers low oscillator phase noise and broadband tuning capabilities, some applications may require the use of an external oscillator.

There are two methods of using an external oscillator with this device. The first method is recommended since it allows for lower current operation with no sacrifice in performance. In this application the external oscillator used should have at least +10 dBm output power. The second method is for use in applications where the external oscillator output power is 0 dBm or less.

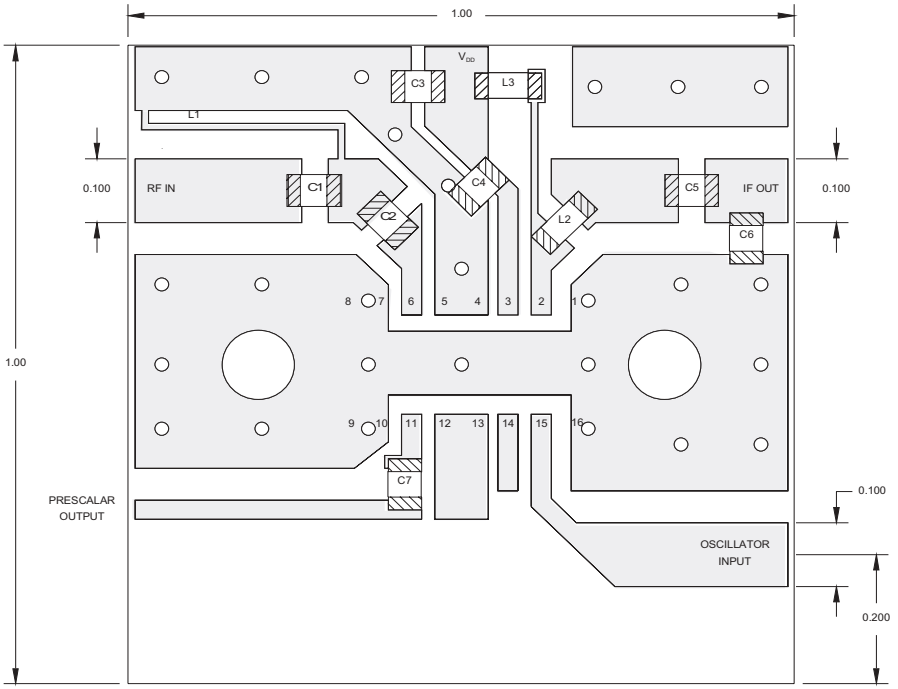
Method 1

This is intended for use with oscillators which have +10 dBm to +15 dBm output power, although the device will operate at lower drive levels with some trade off in performance. Table 1 shows the variation in gain, current, and IMD2 as a function of various oscillator drive levels. Implementation of this method requires disabling the onboard local oscillator of the IC and injecting the external oscillator signal into pin 15 of the IC. To disable the on chip local oscillator, simply remove the RF choke which is normally across pins 3 and 15 in the external circuitry. Figure 8 shows a typical layout for this application.

Table 1

EXTERNAL OSCILLATOR DRIVE LEVEL (dBm)	GAIN (dB)	I_{DD} (mA)	IMD2 (dBc)
6	4.8	62.4	
7	6.0	61.9	- 24
8	7.1	61.2	
9	8.1	60.4	- 26.9
10	8.9	59.5	
11	9.6	58.4	- 31.3
12	10.4	57.4	
13	11.0	56.3	- 34
14	11.5	55.4	
15	11.9	54.7	-35.5

(Measured @ 950 MHz, IF=480 MHz, Pin = - 20 dBm/Tone, Tc = 25˚C)



ADC Forced LO Circuit Layout - Method 1

PARTS LIST		
SYMBOL	DESCRIPTION	PART NO.
C1,C2	4.7 pF CHIP CAPACITOR	VJ0805A4R7DXA
C3	0.1 μF CHIP CAPACITOR	200B104KCA50X
C4,C7	100 pF CHIP CAPACITOR	VJ0805A101JXA
C5	270 pF CHIP CAPACITOR	VJ0805A271JXA
C6	I.0 pF CHIP CAPACITOR	V30805AIRODXA
L1	8 nH PRINTED INDUCTOR	NA
L2	39 nH INDUCTOR	0805CS-390-XMBC
L3	33 nH INDUCTOR	0805CS-330-XMBC

NOTES:

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2. COMPONENTS NOT TO SCALE
3. SUBSTRATE MATERIAL: FR4 Er 4.8
   TAN δ = 0.020 @ 1MHz
4. SUBSTRATE THICKNESS: 0.062
5. DIMENSIONS IN INCHES

Figure 8

Method 2

This method should be used with oscillators which have output power levels of 0 dBm or less. Table 2 shows the effect of lower oscillator drive levels on gain and IMD2. Implementation of this method is simple in that it only requires removing the varactor from the external resonator circuit, adding a 1pF capacitor (C9) between pin 11 & ground, and applying the external oscillator signal to the port (pin 11 of the IC) which would otherwise be used for the local oscillator tuning voltage. A typical layout is shown in Figure 10.

USING THE DEVICE AS A VCO

The ADC offers low phase noise and a broad tuning range while requiring very few external components. As a VCO, power dissipated is typically less than 65mW from its standard 16 pin SOIC surface mount package. The device requires an external resonator, which should be implemented as shown in Figure 3A or 3B, depending on the application.

Figure 9 shows a plot of tuning voltage versus frequency for the dual varactor configuration.

Table 2

EXTERNAL OSCILLATOR DRIVE LEVEL (dBm)	GAIN (dB)	IMD2 (dBc)
0	11.6	- 26.6
- 2	11.4	- 27.0
- 4	10.7	- 28.3
- 6	9.8	- 29.4
- 8	8.5	- 29.3
- 10	7.1	- 28.7

(Measured @ 950 MHz, IF = 480 MHz, Pin = - 20 dBm/Tone, Tc = 25˚C)

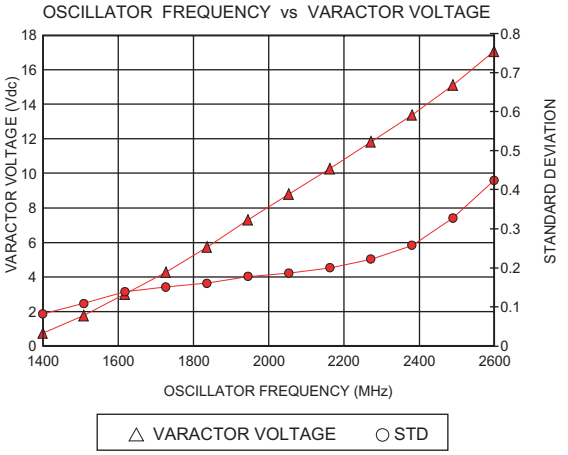
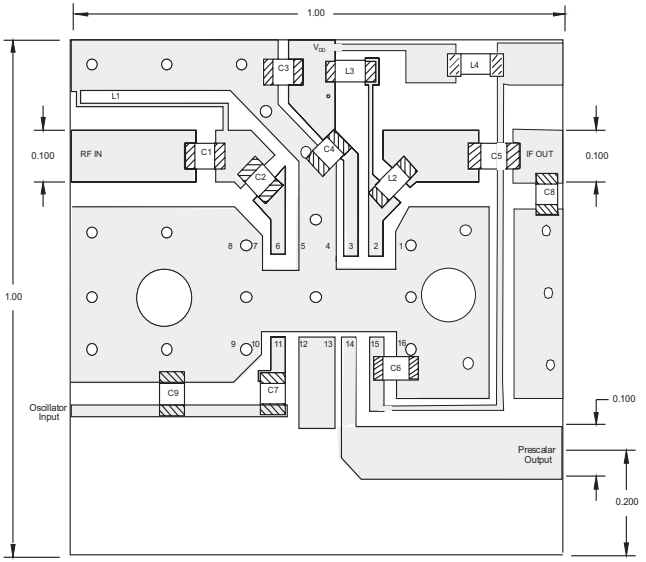


Figure 9



ADC Forced LO Circuit Layout - Method 2

PARTS LIST		
SYMBOL	DESCRIPTION	PART NO.
C1,C2	4.7 pF CHIP CAPACITOR	VJ0805A4R7DXA
C3	0.1 μF CHIP CAPACITOR	200B104KCA50X
C4,C7 C6	100 pF CHIP CAPACITOR	VJ0805A101JXA
C5	270 pF CHIP CAPACITOR	VJ0805A271JXA
C8,C9	1 pF CHIP CAPACITOR	V30805AIR0DXA
L1	8nH PRINTED INDUCTOR	NA
L2	39 nH INDUCTOR	0805CS-390-XMBC
L3	33 nH INDUCTOR	0805CS-330-XMBC
L4	0.470=μH INDUCTOR	380NB-R47M

NOTES:
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2. COMPONENTS NOT TO SCALE
3. SUBSTRATE MATERIAL: FR4 Er 4.8 TAN δ = 0.020 AT 1 MHz
4. SUBSTRATE THICKNESS: 0.062
5. DIMENSIONS IN INCHES

Figure 10

Good RF grounding is important, and via holes to a backside ground plane should be positioned directly beneath pins 1-10,12,13,& 16.

Power (+5Vdc) is supplied to pin 15 of the IC via an RF choke. Oscillator output (pin 14) power is generally in the range of -7 to - 4 dBm, but can be increased approximately 5 dB by removing the 100pF bypass capacitor on pin 15. For narrow band VCO applications, the output power level may be increased further by adding an L-C matching circuit to Pin 14. The ADC20013 phase noise is typically -70 dBc/Hz @ 10 KHz offset and -100 dBc/Hz @ 100KHz offset. A plot of LO power versus frequency (with pin 15 by passed) is shown in Figure 11.

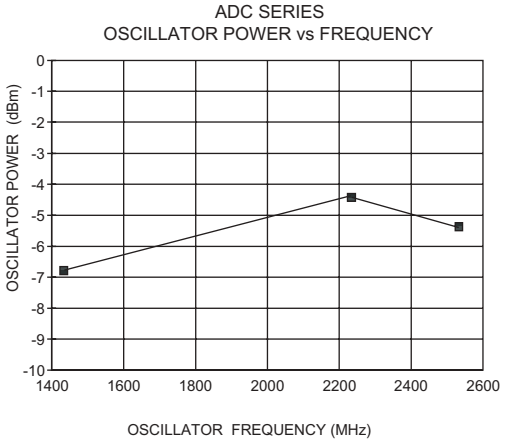

Figure 11

NOTES

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微波光电部专业代理经销高频、微波、光纤、光电元器件、组件、部件、模块、整机；电磁兼容元器件、材料、设备；微波 CAD、EDA 软件、开发测试仿真工具；微波、光纤仪器仪表。欢迎国外高科技微波、光纤厂商将优秀产品介绍到中国、共同开拓市场。长期大量现货专业批发高频、微波、卫星、光纤、电视、CATV 器件： 晶振、VCO、连接器、PIN 开关、变容二极管、开关二极管、低噪晶体管、功率电阻及电容、放大器、功率管、MMIC、混频器、耦合器、功分器、振荡器、合成器、衰减器、滤波器、隔离器、环行器、移相器、调制解调器；光电子元器件和组件：红外发射管、红外接收管、光电开关、光敏管、发光二极管和发光二极管组件、半导体激光二极管和激光器组件、光电探测器和光接收组件、光发射接收模块、光纤激光器和光放大器、光调制器、光开关、DWDM 用光发射和接收器件、用户接入系统光光收发器件与模块、光纤连接器、光纤跳线/尾纤、光衰减器、光纤适 配器、光隔离器、光耦合器、光环行器、光复用器/转换器；无线收发芯片和模组、蓝牙芯片和模组。

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