HEWLETT PACKARD

APPLICATION NOTE 970

A 6 GHz Amplifier Using the HFET-1101 GaAs FET

INTRODUCTION

The GaAs field effect transistor is establishing its performance superiority in most microwave low noise receiver designs. Even at frequencies as low as 1GHz the GaAs FET can be used with non-conventional stabilization circuitry[1]. The GaAs FET is a unique device with numerous applications, for example: amplifiers, oscillators; mixers; modulators; parametric-amplifier replacements; and RF switches.

The Hewlett-Packard HFET-1101 is a device designed for good noise, gain and power output characteristics when used as an amplifier. The purpose of this application note is to highlight some of the design tradeoffs when using a GaAs FET. The example is an amplifier for use in the 5.9 to 6.4 GHz telecommunications band. The amplifier's performance over this band is excellent, with a maximum noise figure of 3.3 dB, a minimum associated gain of 10.9 dB, a flatness of ±0.4 dB and a 9.5 dBm minimum power output at 1dB gain compression. The maximum input and output SWR are 2.67:1 and 1.90:1 respectively.

DESIGN TRADE-OFFS

The first choice facing a designer is biasing. In comparison to silicon bipolars, GaAs FETs require more current at a lower voltage, with the net result being about the same power dissipation. Power supply requirements should reflect this characteristic.

With any single stage amplifier design, there are three performance parameters that require different optimum bias settings.

They are:

1. Minimum noise figure
   V_{DS} = 3.5 Volts, I_{DS} = 15% I_{DSS}
2. Linear power output
   V_{DS} = 4.0 Volts, I_{DS} = 50% I_{DSS}
3. Maximum Gain
   V_{DS} = 4.0 Volts, I_{DS} = 100% I_{DSS}

For the three critical bias settings above, the input and output matching data are available from the scattering[2], noise[3], power[3] and gain[4] parameters. The linear power bias point of V_{DS} = 4.0 Volts and I_{DS} = 50% I_{DSS} provides a good compromise between minimum noise figure and maximum gain. At this bias point the scattering, noise, power and gain parameters can be measured by various known techniques[5]. Typical parameters at 6 GHz for the HFET-1101 are:

Scattering Parameters

S_{11} = 0.641/-171.3°
S_{12} = 0.057/16.3°
S_{21} = 2.058/28.5°
S_{22} = 0.572/-95.7°

Gain Parameters

K = 1.504
G_a (max.) = 11.38 dB
Γ_{MS} = 0.762/177.3°
Γ_{ML} = 0.718/103.9°

Noise Parameters

F_{MIN} = 2.9 dB
R_n = 9.42 ohms
Γ_O = 0.542/141°
Γ_L = 0.575/104.5°

Power Parameters @ P_{TUNE} = 5 dBm

P_{1dB} = 15.5 dBm
G_p = 8.2 dB
Γ_{PS} = 0.729/166°
Γ_{PL} = 0.489/101°

Even at this compromise bias point, the input matching network has four performance trade-offs that can be juggled. They are: noise figure; available power gain; power output; and input SWR. Table I gives the conditions when the input impedance is chosen for, respectively: lowest noise figure; highest available power gain; and greatest linear power output.

TABLE I

Noise Figure	Gain	Power Output
Γ_O= 0.542/141°	Γ_{MS}=0.762/177.3°	Γ_{PS}=0.729/166°
Γ_L=0.575/104.5°	Γ_{ML}=0.718/103.9°	Γ_{PL}=0.489/101°
F_{MIN}=2.90 dB	F = 4.44 dB	F = 3.69 dB
G_a=9.33 dB	G_a (max.)=11.38 dB	G_p=8.2 dB
P_{1dB}=9.3 dBm	P_{1dB}=13.4 dBm	P_{1dB}=15.5 dB

When the input impedance is chosen for either lowest noise or maximum gain, the output is assumed to be conjugately matched. The noise figure and gain at the three conditions shown above are calculated from the parameters given, while the power output (P_{1dB}) performance is experimentally measured.[3] [4]

The data for the power output was taken at an input drive level of 8.3 dBm. As we approach large signal conditions, i.e. 5 dBm or greater, it becomes difficult to predict compromises between noise, gain and input SWR. Since noise and gain are small signal parameters and are not functions of input drive level it is possible to predict input SWR trends over a wide dynamic range.

Since most low noise receivers work in a small signal environment, the design engineer is typically concerned with compromising gain and input SWR for noise figure. To demonstrate this, Γ_O and Γ_{MS}, the source reflection coefficients for lowest noise figure and highest available gain are plotted on a Smith Chart in Figure 1.

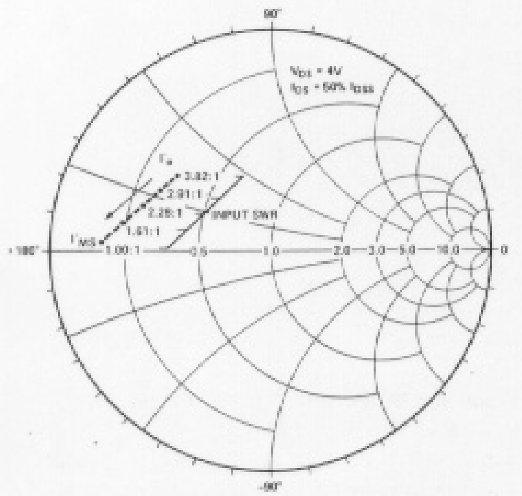


Figure 1. Source Reflection Coefficient Vs. Noise Figure.

Moving from Γ_O toward Γ_{MS} along a straight line, input SWR improves to 1.0:1 at Γ_{MS}, assuming the output to be conjugately matched. At the same time, noise figure and available gain are increasing. Table II shows corresponding values for noise, gain and input SWR.

TABLE II

	Γ_S Mag/Ang	Γ_L Mag/Ang	N.F. [dB]	Ga [dB]	Input SWR	Output SWR
Γ_o →	0.542/141°	0.575/104°	2.90	9.33	3.82:1	1.00:1
	0.572/152°	0.601/105°	2.97	10.04	2.91:1	1.00:1
	0.614/160°	0.627/106°	3.14	10.56	2.28:1	1.00:1
	0.678/169°	0.667/105°	3.57	11.10	1.61:1	1.00:1
Γ_{MS} →	0.762/177°	0.718/104°	4.44	11.38	1.00:1	1.00:1

From Table II, a very good compromise input match condition is Γ_S = 0.614/160° and the corresponding output conjugate match condition is Γ_L=0.627,106°. In comparison to the minimum noise match conditions the noise figure is increased by 0.24 dB but the associated gain is increased by 1.22 dB and the input, SWR is improved by 40% to 2.28:1. Of course, other compromises can also be chosen. For example, the optimum bias for noise figure may be chosen and the source impedance compromised between minimum noise figure and maximum gain at that bias. Values of noise figure and gain may be calculated and compared for each of these compromises.

With the choice of Γ_S and Γ_L discussed above, it is now possible to synthesize the input and output matching networks.

INPUT MATCHING NETWORK

1. The impedance Z_S, corresponding to Γ_S = 0.614/160° is:

$$Z_S = \frac{(1 - |\Gamma_S|^2)\,50}{1 + |\Gamma_S|^2 - 2\,|\Gamma_S|\cos\angle\Gamma_S} + j\,\frac{100\,|\Gamma_S|\sin\angle\Gamma_S}{1 + |\Gamma_S|^2 - 2\,|\Gamma_S|\cos\angle\Gamma_S}$$

$$Z_S = 12.31 + j8.30$$

2. $Y_S = \dfrac{1}{Z_S} = 0.056 - j0.038$

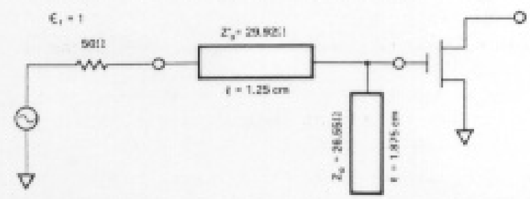
3. An open circuited stub looks like a shunt admittance $Y = jY_o \tan \beta\ell$. Therefore, an open circuited stub that is three-eighths wavelength long looks like a shunt inductor of admittance $-jY_o$. Hence:

$$Z_o = \frac{1}{Y_o} = \frac{1}{I_m\left[Y_S\right]} = 26.55\Omega$$

4. Since the driving source impedance is 50Ω, a quarter-wave transformer of characteristic impedance

$$Z'_o = \sqrt{50\left[\frac{1}{R_e\left[Y_S\right]}\right]} = 29.92\Omega$$

completes the input matching network.



OUTPUT MATCHING NETWORK

1. The impedance Z_L, corresponding to Γ_L = 0.627/106° is:

$$Z_L = \frac{(1 - |\Gamma_L|^2)\,50}{1 + |\Gamma_L|^2 - 2\,|\Gamma_L|\cos\angle\Gamma_L} + j\,\frac{100\,|\Gamma_L|\sin\angle\Gamma_L}{1 + |\Gamma_L|^2 - 2\,|\Gamma_L|\cos\angle\Gamma_L}$$

$$Z_L = 17.45 + j34.66$$

2. $Y_L = \dfrac{1}{Z_L} = 0.012 - j0.023$

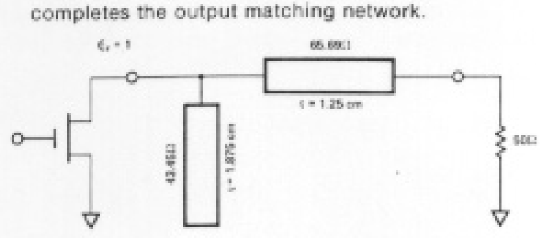
3. The output matching network is similar to the input matching network. An open circuited stub that is three-eighths wavelength long looks like a shunt inductor of admittance $-jY_o$. Hence:

$$Z_o = \frac{1}{Y_o} = \frac{1}{I_m\left[Y_L\right]} = 43.45\Omega$$

4. Since the load impedance is 50Ω, a quarter-wave transformer of characteristic impedance:

$$Z'_o = \sqrt{50\left[\frac{1}{R_e\,Y_L}\right]} = 65.69\Omega$$

completes the output matching network.



PERFORMANCE

An amplifier was constructed using the design derived above. A comparison of the computer simulation with measured amplifier performance at 6 GHz is shown below.

Parameter	Measured Performance	Computer Simulation
Gain	11.50 dB	10.55 dB
Input SWR	2.67:1	2.28:1
Output SWR	1.90:1	1.00:1
Isolation	-23 dB	-20.60 dB
Noise Figure	3.27 dB	3.14 dB

The performance of the amplifier was measured over the 5.9 to 6.4 GHz band. Figures 2, 3, 4, 5, and 6 show the room temperature performance.

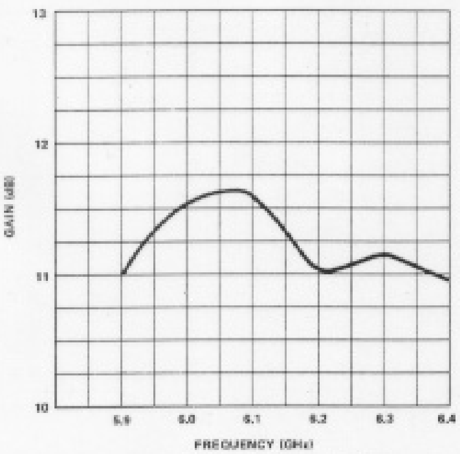


Figure 2. Gain Performance.

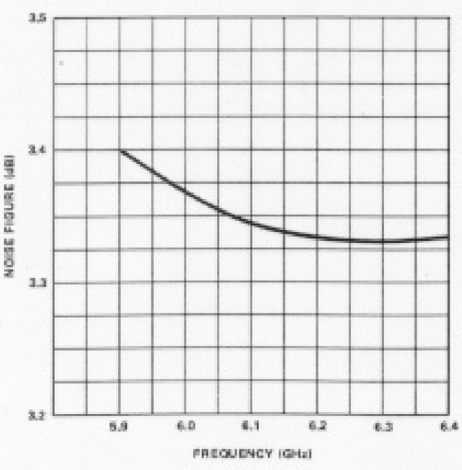


Figure 3. Noise Performance.

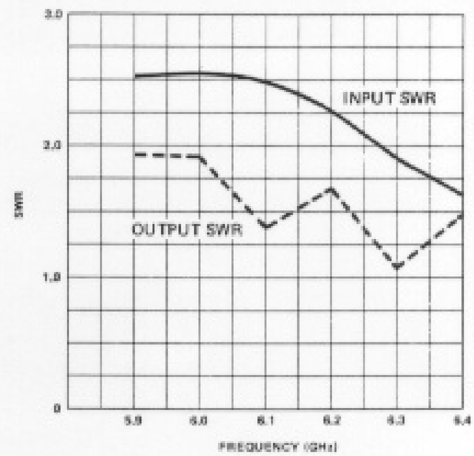


Figure 4. Input-Output SWR Performance.

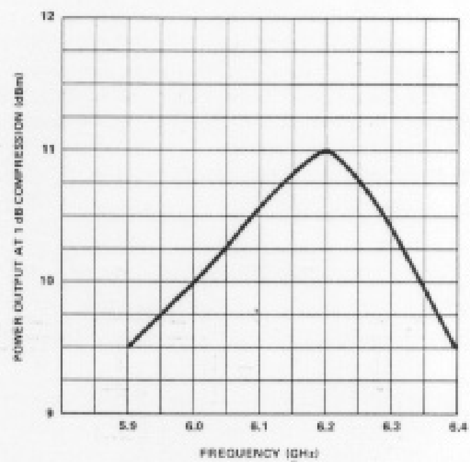


Figure 5. Power Output Performance.

Isolation — Isolation is better than -23 dB over the entire 5.9 to 6.4 GHz band.

Phase Linearity — Phase linearity is ±6° over the entire 500 MHz bandwidth.

AM to PM Conversion — With an output power level of -13 dBm, the input power level is referenced. At this input reference level, the input power is varied ±10 dB. Over the 5.9 to 6.4 GHz band, the average AM to PM conversion is 0.055°/dB.

Third Order Intercepts — With two fundamental signals injected into the input at 5.95 and 6.05 GHz, the output power level for each fundamental signal is set for 0 dBm. The third order intermodulation products are both 44 dB below the two fundamentals at the output. Therefore, the third order intercept point is +22 dBm.

The wideband gain performance is plotted on the following page.

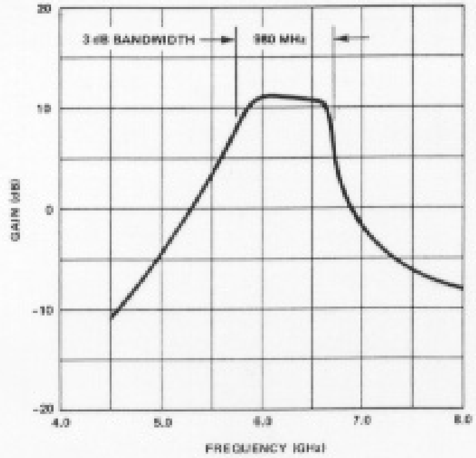
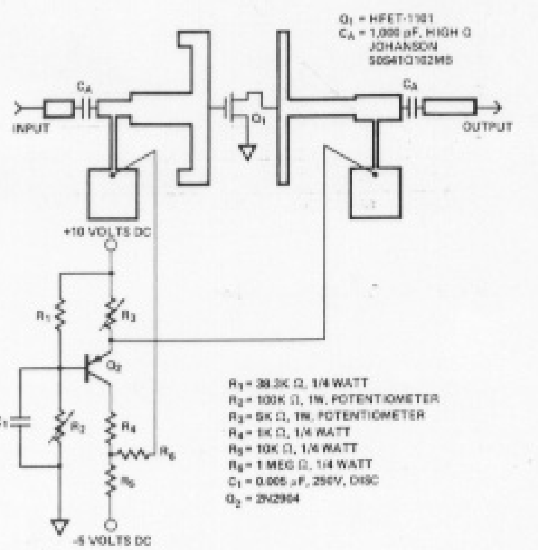


Figure 6. Wideband Gain Performance.

CONSTRUCTION

The board material is 0.031" RT/Duroid 120-061 (D5880) (Manufactured by Roger Corp. in Chandler, AZ), with 1oz. copper clad on two sides. The relative dielectric constant (ϵ_r) is 2.23. Duroid was chosen because of its low loss tangent. The thickness of 0.031" was chosen so the source top cap could be soldered to the RF ground, thereby taking advantage of the low source inductance.



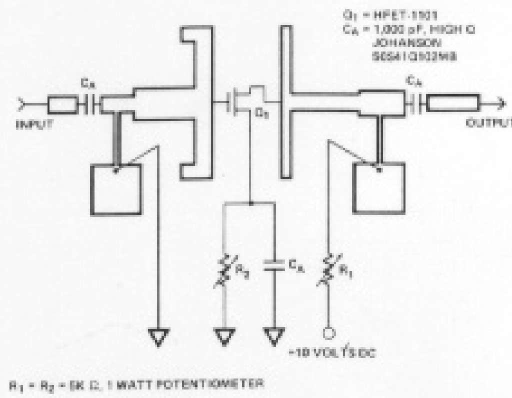
The quiescent point is controlled by R_2 and R_3. R_2 is adjusted to provide the proper V_{DS} and R_3 is adjusted to supply the correct drain current (I_{DS}).

Schematic I Complete Amplifier

To minimize transition interactions the shunt stubs were balanced along the series transmission lines. The bias network is fed at the quarter-wavelength point of a half-wavelength open circuited stub.

Two different types of biasing networks were used with the same result. A schematic of the complete amplifier and biasing circuit can be seen in the diagram that follows. The differences between the biasing networks are:

1. Schematic I is an active network which requires a dual polarity supply with an active pulse recovery loop.
2. Schematic II is a self-biasing network which requires a very good source by-passing capacitor. It has a lower component count with a single supply requirement. It is, however, more subject to oscillations.



The quiescent point is controlled by R_1 and R_2. R_1 is adjusted to provide the proper V_{DS} and R_2 is adjusted to supply the correct drain current (I_{DS}).

Schematic II Complete Amplifier

REFERENCES

1. Hewlett-Packard E.M.A.C.C. '77 Technical Session Paper, "Low Noise Amplifier Design Techniques at 1.5 GHz" by Arthur Woo, Ottawa, May 3, 1977.
2. HFET-1101, Microwave GaAs FET, data sheet.
3. Hewlett-Packard Application Bulletin 19, "Noise and Power Parameters for the HFET-1101".
4. Hewlett-Packard Application Note 95-1, "S-Parameter Techniques for Faster, More Accurate Network Design", September 1968.
5. Hewlett-Packard Application Bulletin 10, "Transistor Noise Figure Measurements".

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