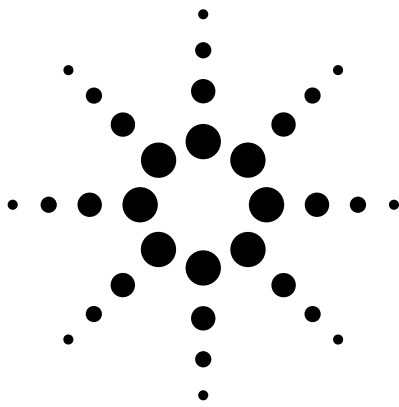


Agilent HCPL-3140/HCPL-0314

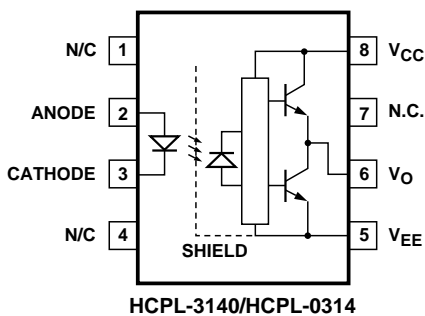
0.6 Amp Output Current IGBT

Gate Drive Optocoupler

Data Sheet



Functional Diagram



Truth Table

LED	V_O
OFF	LOW
ON	HIGH

Description

The HCPL-3140/HCPL-0314 family of devices consists of a GaAsP LED optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the

output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving small or medium power IGBTs. For IGBTs with higher ratings, the HCPL-3150 (0.6 A) or HCPL-3120 (2.5 A) optocouplers can be used.

Features

- 0.6 A maximum peak output current
- 0.4 A minimum peak output current
- High speed response: 0.7 μ s maximum propagation delay over temperature range
- Ultra high CMR: minimum 10 kV/ μ s at $V_{CM} = 1$ kV
- Bootstrappable supply current: maximum 3 mA
- Wide operating temperature range: -40°C to 100°C
- Wide V_{CC} operating range: 10 V to 30 V over temp. range
- Available in DIP8 and SO8 package
- Safety approvals: UL approval, 3750 V_{rms} for 1 minute. CSA approval. IEC/EN/DIN EN 60747-5-2 approval $V_{IORM} = 630 V_{peak}$ (HCPL-3140)

Applications

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drives
- Inverters for home appliances
- Industrial inverters
- Switch Mode Power Supplies (SMPS)

A 0.1 μ F bypass capacitor must be connected between pins V_{CC} and V_{EE} .

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.



Ordering Information

Specify part number followed by option number (if desired).

Example:

HCPL-3140#XXXX

- No option = Standard DIP package, 50 per tube.
- 300 = Gull Wing Surface Mount Option, 50 per tube.
- 500 = Tape and Reel Packaging Option.
- 060 = IEC/EN/DIN EN 60747-5-2, $V_{IORM} = 630 V_{PEAK}$.
- XXXE = Lead Free Option.

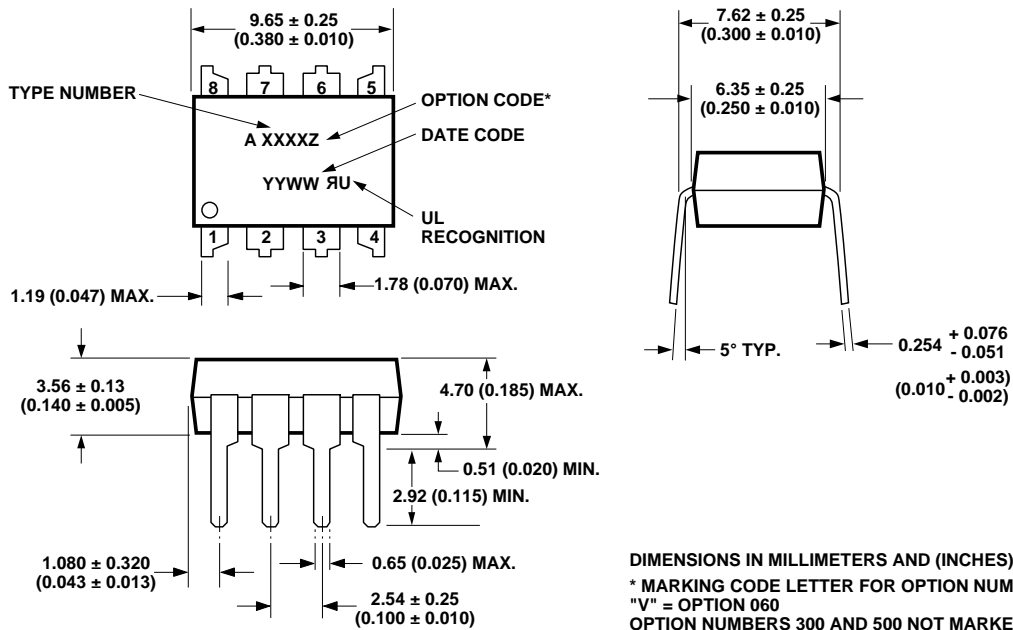
HCPL-0314#XXXX

- No option = SOIC-8 surface mount in tube, 100 per tube.
- 500 = Tape and Reel Packaging Option.
- 060 = IEC/EN/DIN EN 60747-5-2, $V_{IORM} = 566 V_{PEAK}$.
- XXXE = Lead Free Option.

Remarks: The notation “#” is used for existing products, while (new) products launched since 15th July 2001 and lead free option will use “-”

Package Outline Drawings

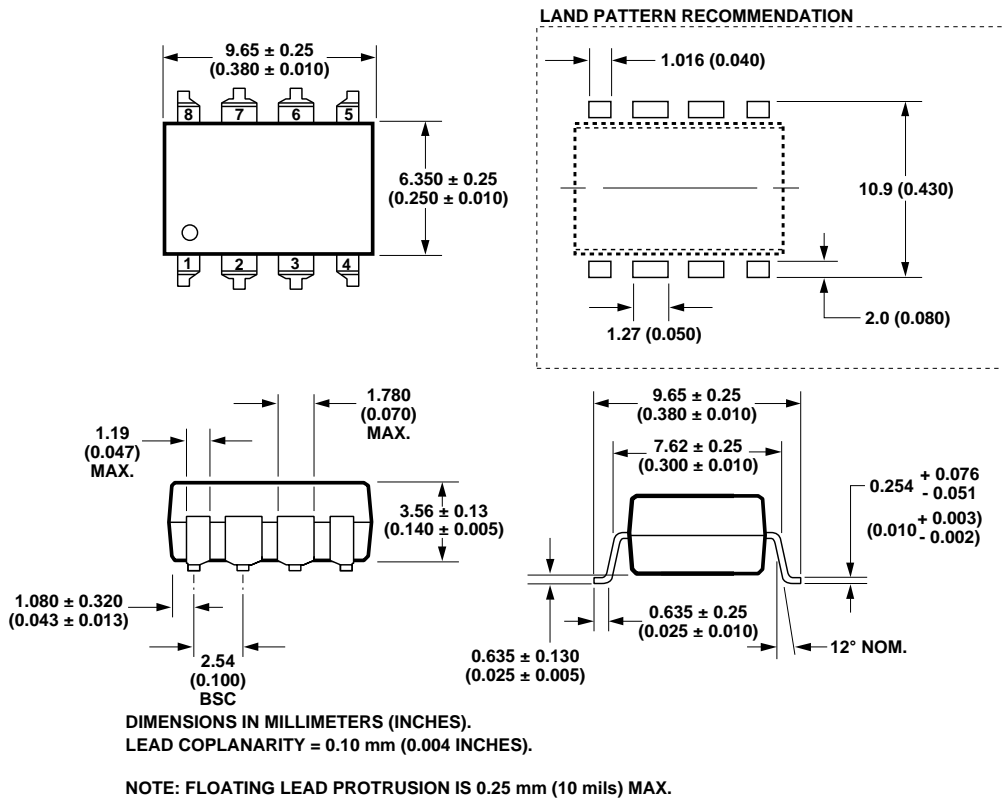
HCPL-3140 Standard DIP Package



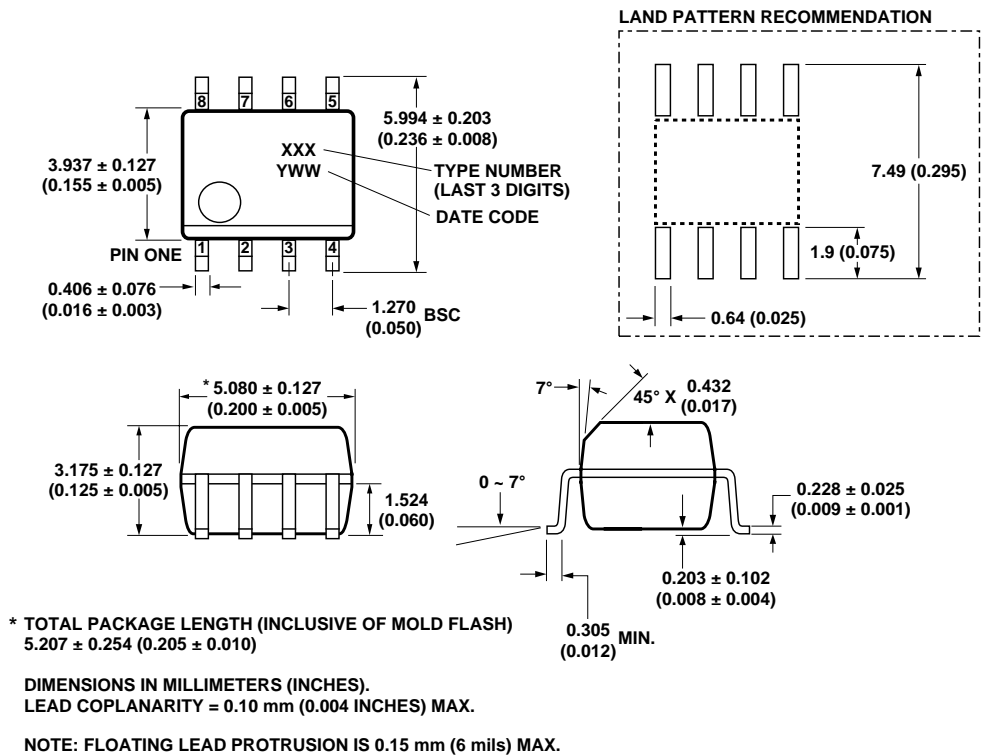
DIMENSIONS IN MILLIMETERS AND (INCHES).
 * MARKING CODE LETTER FOR OPTION NUMBERS
 "V" = OPTION 060
 OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

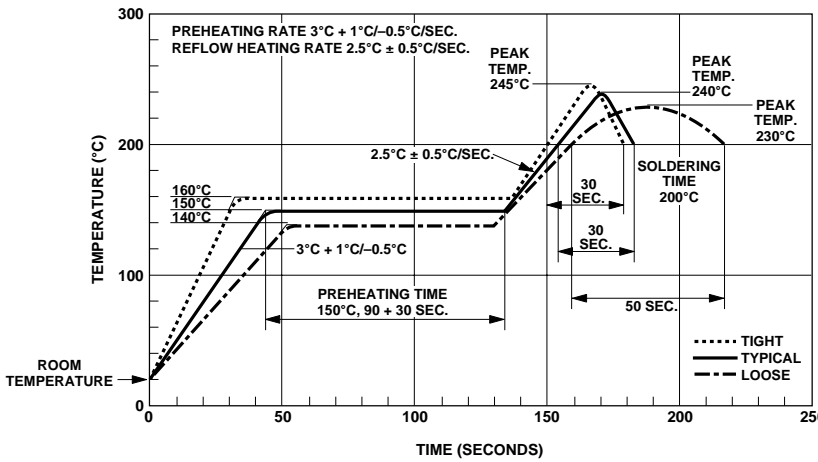
HCPL-3140 Gull Wing Surface Mount Option 300 Outline Drawing



HCPL-0314 Small Outline SO-8 Package



Solder Reflow Temperature Profile



Regulatory Information

The HCPL-3140/HCPL-0314 have been approved by the following organizations:

IEC/EN/DIN EN 60747-5-2

Approved under:
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01
(Option 060 only)

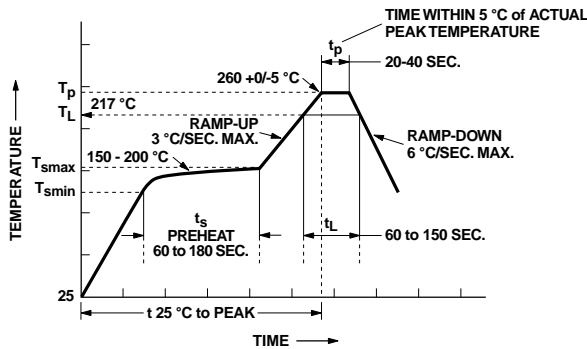
UL

Approval under UL 1577, component recognition program up to $V_{ISO} = 2500 V_{RMS}$. File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Recommended Pb-Free IR Profile



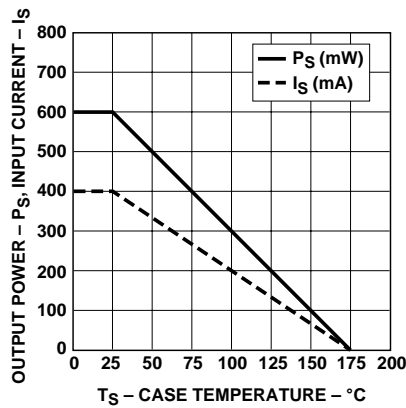
NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
 $T_{smax} = 200 °C$, $T_{smin} = 150 °C$

IEC/EN/DIN EN 60747-5-2 Insulation Characteristics (HCPL-3140 Option 060)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage $\leq 150 V_{RMS}$ for rated mains voltage $\leq 300 V_{RMS}$ for rated mains voltage $\leq 600 V_{RMS}$		I - IV I - III I-II	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ sec, Partial discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.5 = V_{PR}$, Type and Sample Test, $t_m = 60$ sec, Partial discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 10$ sec)	V_{IOTM}	6000	V_{peak}
Safety-limiting values - maximum values allowed in the event of a failure.			
Case Temperature	T_s	175	°C
Input Current**	$I_{S, INPUT}$	230	mA
Output Power**	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_s , $V_{IO} = 500$ V	R_s	$> 10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2 for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of P_s and I_s on ambient temperature.



Insulation and Safety Related Specifications

Parameter	Symbol	HCPL-3140	HCPL-0314	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T _S	-55	125	°C	
Operating Temperature	T _A	-40	100	°C	
Average Input Current	I _{F(AVG)}		25	mA	1
Peak Transient Input Current (<1 μs pulse width, 300pps)	I _{F(TRAN)}		1.0	A	
Reverse Input Voltage	V _R		5	V	
"High" Peak Output Current	I _{OH(PEAK)}		0.6	A	2
"Low" Peak Output Current	I _{OL(PEAK)}		0.6	A	2
Supply Voltage	V _{CC-V_{EE}}	-0.5	35	V	
Output Voltage	V _{O(PEAK)}	-0.5	V _{CC}	V	
Output Power Dissipation	P _O		250	mW	3
Input Power Dissipation	P _I		105	mW	4
Lead Solder Temperature		260°C for 10 sec., 1.6 mm below seating plane			
Solder Reflow Temperature Profile		See Package Outline Drawings section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply	$V_{CC}-V_{EE}$	10	30	V	
Input Current (ON)	$I_{F(ON)}$	8	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-3.0	0.8	V	
Operating Temperature	T_A	-40	100	°C	

Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	0.2			A	$V_o = V_{CC} - 4$	2	5
		0.4	0.5			$V_o = V_{CC} - 10$	3	2
Low Level Output Current	I_{OL}	0.2	0.4		A	$V_o = V_{EE} + 2.5$	5	5
		0.4	0.5			$V_o = V_{EE} + 10$	6	2
High Level Output Voltage	V_{OH}	$V_{CC} - 4$	$V_{CC} - 1.8$		V	$I_o = -100$ mA	1	6,7
Low Level Output Voltage	V_{OL}		0.4	1	V	$I_o = 100$ mA	4	
High Level Supply Current	I_{CCH}		0.7	3	mA	$I_o = 0$ mA	7,8	14
Low Level Supply Current	I_{CCL}		1.2	3	mA	$I_o = 0$ mA		
Threshold Input Current Low to High	I_{FLH}			7	mA	$I_o = 0$ mA, $V_o > 5$ V		9,15
Threshold Input Voltage High to Low	V_{FHL}	0.8			V			
Input Forward Voltage	V_F	1.2	1.5	1.8	V	$I_F = 10$ mA	16	
Temperature Coefficient of Input Forward Voltage	DV_F/DT_A		-1.6		mV/°C			
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10$ μA		
Input Capacitance	C_{IN}		60		pF	$f = 1$ MHz, $V_F = 0$ V		

Switching Specifications (AC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.1	0.2	0.7	μs	$R_g = 47 \Omega$, $C_g = 3 \text{ nF}$,	10,11, 12,13,	14
Propagation Delay Time to Low Output Level	t_{PHL}	0.1	0.3	0.7	μs	$f = 10 \text{ kHz}$, Duty Cycle =	14,17	
Propagation Delay Difference Between Any Two Parts or Channels	PDD	-0.5		0.5	μs	50%, $I_F = 8 \text{ mA}$, $V_{CC} = 30 \text{ V}$		10
Rise Time	t_R		50		ns			
Fall Time	t_F		50		ns			
Output High Level Common Mode Transient Immunity	$ CM_H $	10			kV/ μs	$T_A = 25^\circ C$, $V_{CM} = 1 \text{ kV}$	18	11
Output Low Level Common Mode Transient Immunity	$ CM_L $	10			kV/ μs		18	12

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	3750			V_{rms}	$T_A = 25^\circ C$, RH<50% for		8,9
Input-Output Resistance	R_{I-O}		10^{12}		Ω	$V_{I-O} = 500 \text{ V}$		9
Input-Output Capacitance	C_{I-O}		0.6		pF	Freq=1 MHz		

Notes:

- Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.
- Maximum pulse width = 10 μs , maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.4 A. See Application section for additional details on limiting I_{OL} peak.
- Derate linearly above 85°C, free air temperature at the rate of 4.0 mW/°C.
- Input power dissipation does not require derating.
- Maximum pulse width = 50 μs , maximum duty cycle = 0.5%.
- In this test, V_{OH} is measured with a DC load current. When driving capacitive load V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
- Maximum pulse width = 1 ms, maximum duty cycle = 20%.
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 4500 V_{rms}$ for 1 second (leakage detection current limit $I_{I-O} \leq 5 \mu A$). This test is performed before 100% production test for partial discharge (method B) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table, if applicable.
- Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
- PDD is the difference between t_{PHL} and t_{PLH} between any two parts or channels under the same test conditions.
- Common mode transient immunity in the high state is the maximum tolerable $|dV_{cm}/dt|$ of the common mode pulse V_{CM} to assure that the output will remain in the high state (i.e. $V_o > 6.0 \text{ V}$).
- Common mode transient immunity in a low state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM} , to assure that the output will remain in a low state (i.e. $V_o < 1.0 \text{ V}$).
- This load condition approximates the gate load of a 1200 V/25 A IGBT.
- The power supply current increases when operating frequency and Q_g of the driven IGBT increases.

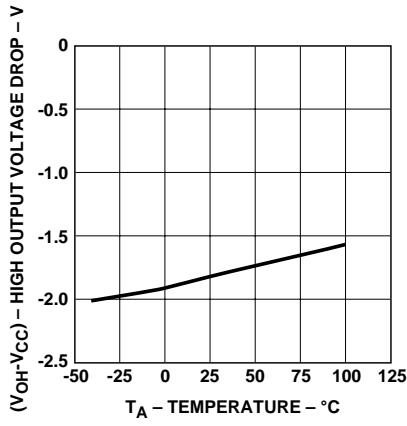


Figure 1. V_{OH} vs. Temperature.

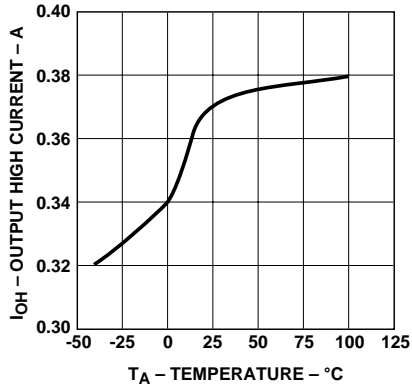


Figure 2. I_{OH} vs. Temperature.

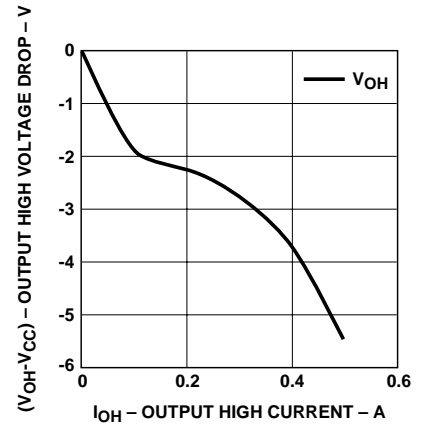


Figure 3. V_{OH} vs. I_{OH} .

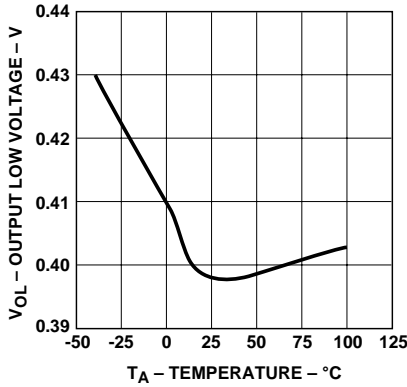


Figure 4. V_{OL} vs. Temperature.

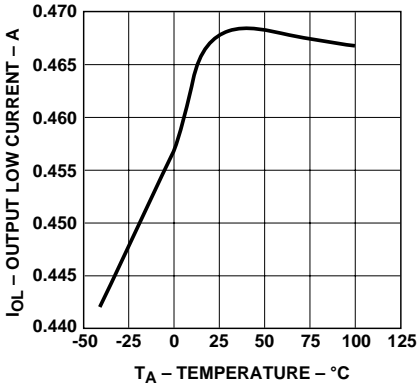


Figure 5. I_{OL} vs. Temperature.

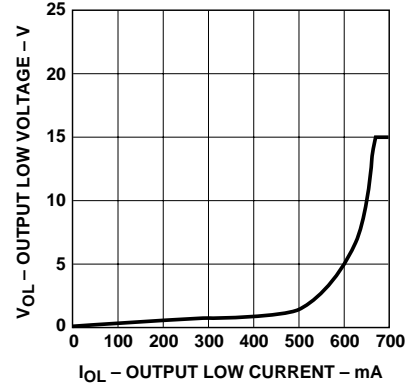


Figure 6. V_{OL} vs. I_{OL} .

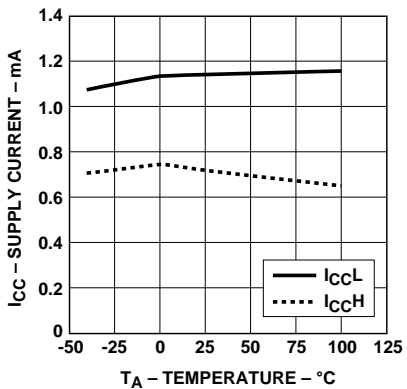


Figure 7. I_{CC} vs. Temperature.

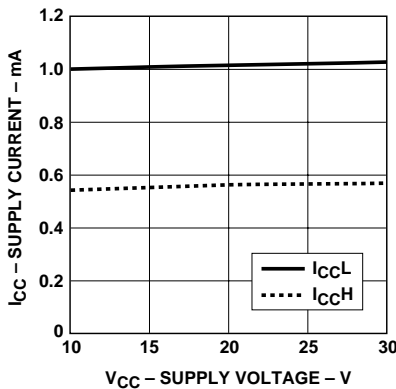


Figure 8. I_{CC} vs. V_{CC} .

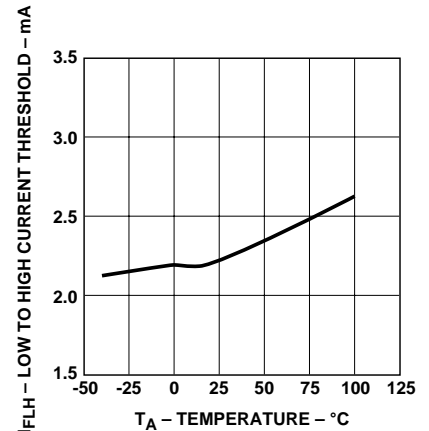


Figure 9. I_{FLH} vs. Temperature.

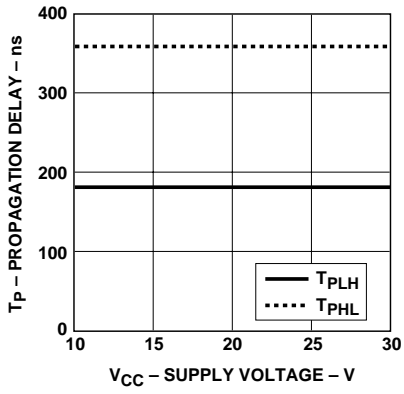


Figure 10. Propagation Delay vs. V_{CC} .

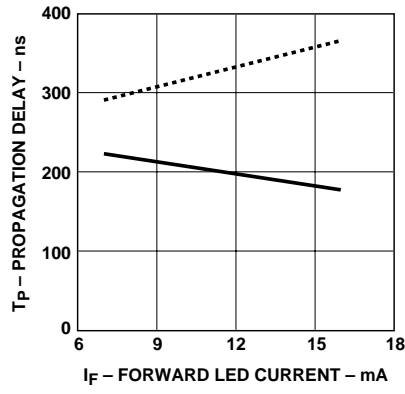


Figure 11. Propagation Delay vs. I_F .

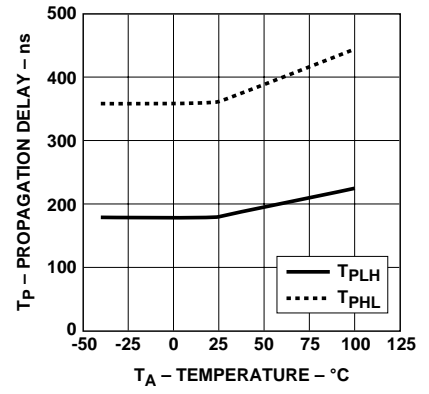


Figure 12. Propagation Delay vs. Temperature.

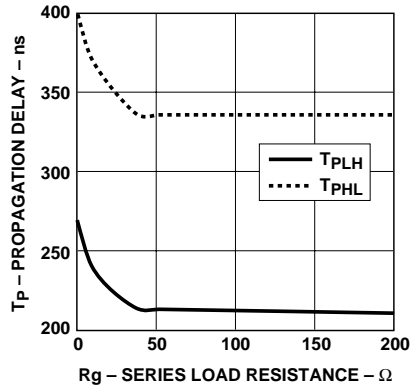


Figure 13. Propagation Delay vs. R_g .

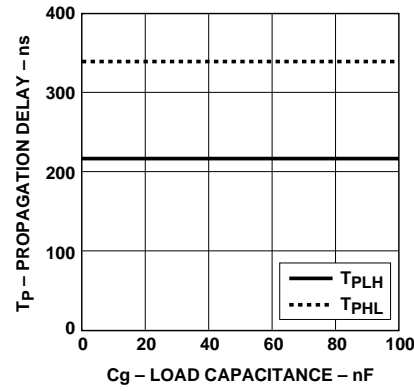


Figure 14. Propagation Delay vs. C_g .

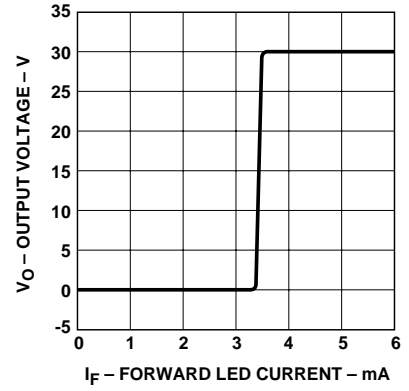


Figure 15. Transfer Characteristics.

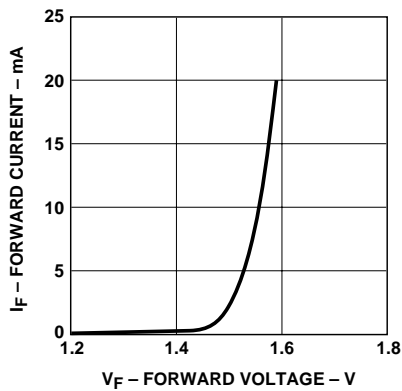


Figure 16. Input Current vs. Forward Voltage.

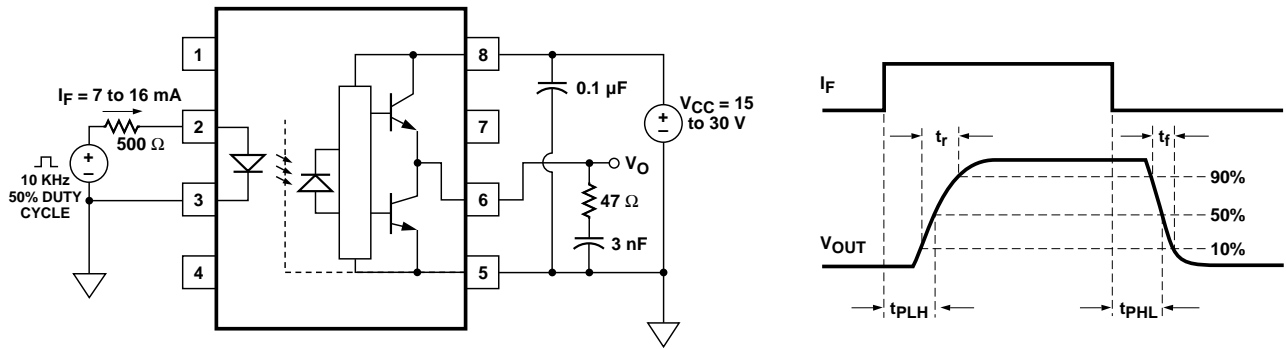


Figure 17. Propagation Delay Test Circuit and Waveforms.

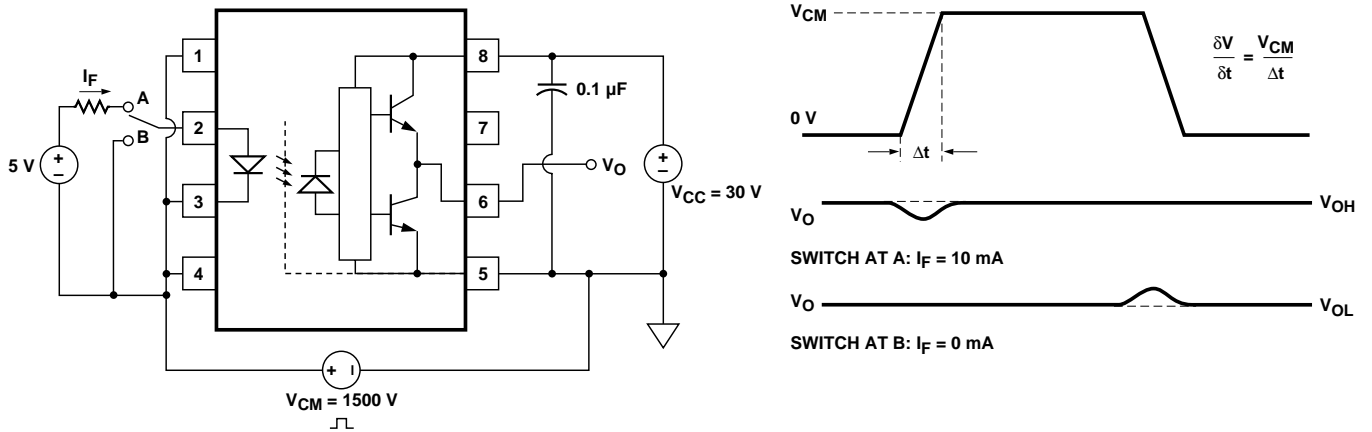


Figure 18. CMR Test Circuit and Waveforms.

Applications Information
Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-3140/HCPL-0314 has a very low maximum V_{OL} specification of 1.0 V. Minimizing R_g and the lead inductance from the HCPL-3140/HCPL-0314 to the IGBT gate and emitter (possibly by mounting the

HCPL-3140/HCPL-0314 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 19. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-3140/HCPL-0314 input as this can result in unwanted

coupling of transient signals into the input of HCPL-3140/HCPL-0314 and degrade performance. (If the IGBT drain must be routed near the HCPL-3140/HCPL-0314 input, then the LED should be reverse biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-3140/HCPL-0314.)

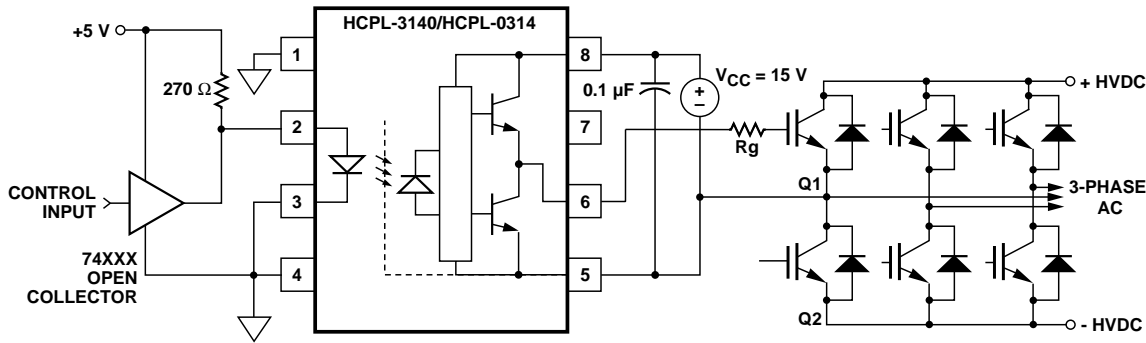


Figure 19. Recommended LED Drive and Application Circuit for HCPL-3140/HCPL-0314.

Selecting the Gate Resistor (R_g)

Step 1: Calculate R_g minimum from the I_{OL} peak specification. The IGBT and R_g in Figure 19 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3140/HCPL-0314.

$$\begin{aligned} R_g &\geq \frac{V_{CC} - V_{OL}}{I_{OLPEAK}} \\ &= \frac{24\text{ V} - 5\text{ V}}{0.6\text{ A}} \\ &= 32\ \Omega \end{aligned}$$

The V_{OL} value of 5 V in the previous equation is the V_{OL} at the peak current of 0.6A. (See Figure 6).

Step 2: Check the HCPL-3140/HCPL-0314 power dissipation and increase R_g if necessary. The HCPL-3140/HCPL-0314 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$$P_T = P_E + P_O$$

$$P_E = I_F \cdot V_F \cdot \text{Duty Cycle}$$

$$\begin{aligned} P_O &= P_{O(BIAS)} + P_{O(SWITCHING)} = I_{CC} \cdot V_{CC} + E_{SW}(R_g, Q_g) \cdot f \\ &= (I_{CCBIAS} + K_{ICC} \cdot Q_g \cdot f) \cdot V_{CC} + E_{SW}(R_g, Q_g) \cdot f \end{aligned}$$

where $K_{ICC} \cdot Q_g \cdot f$ is the increase in I_{CC} due to switching and K_{ICC} is a constant of 0.001 mA/(nC*kHz). For the circuit in Figure 19 with I_F (worst case) = 10 mA, R_g = 32 Ω, Max Duty Cycle = 80%, Q_g = 100 nC, f = 20 kHz and T_{AMAX} = 85°C:

$$P_E = 10\text{ mA} \cdot 1.8\text{ V} \cdot 0.8 = 14\text{ mW}$$

$$P_O = (3\text{ mA} + (0.001\text{ mA}/(\text{nC} \cdot \text{kHz})) \cdot 20\text{ kHz} \cdot 100\text{ nC}) \cdot 24\text{ V} + 0.4\ \mu\text{J} \cdot 20\text{ kHz} = 80\text{ mW}$$

$$< 260\text{ mW} (P_{O(MAX)} @ 85^\circ\text{C})$$

The value of 3 mA for I_{CC} in the previous equation is the max. I_{CC} over entire operating temperature range.

Since P_O for this case is less than P_{O(MAX)}, R_g = 32 Ω is alright for the power dissipation.

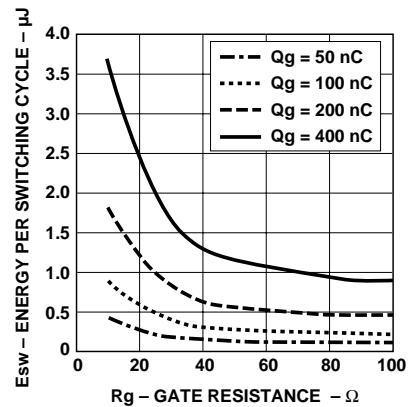


Figure 20. Energy Dissipated in the HCPL-0314 and for Each IGBT Switching Cycle.

LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 21. The HCPL-3140/HCPL-0314 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and opto-coupler pins 5-8 as shown in Figure 22. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 19), can achieve 10 kV/μs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

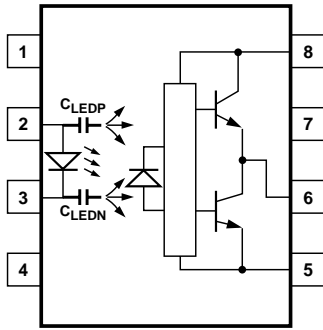


Figure 21. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

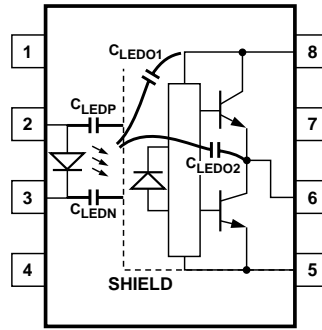


Figure 22. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

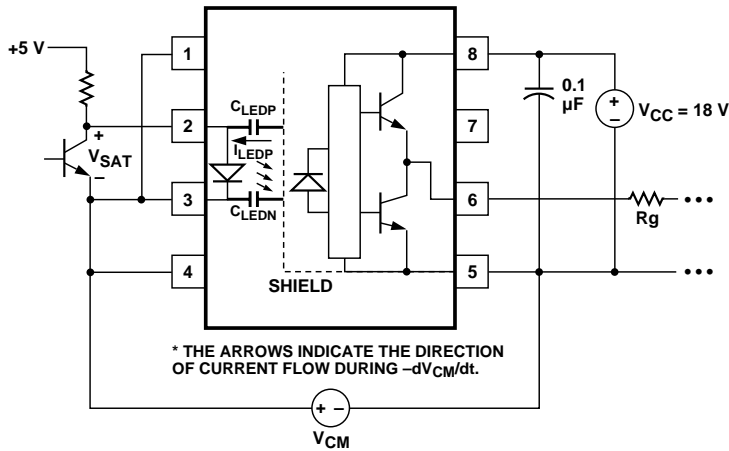


Figure 23. Equivalent Circuit for Figure 17 During Common Mode Transient.

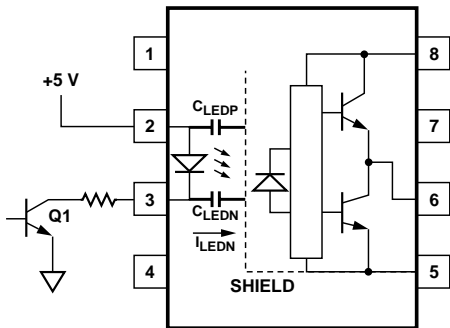


Figure 24. Not Recommended Open Collector Drive Circuit.

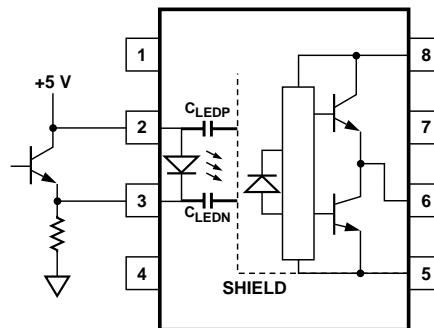


Figure 25. Recommended LED Drive Circuit for Ultra-High CMR IPM Dead Time and Propagation Delay Specifications.

CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 8 mA provides adequate margin over the maximum I_{FLH} of 5 mA to achieve 10 kV/μs CMR.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{CM}/dt$ transient in Figure 23, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than V_{F(OFF)} the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 24, can not keep the LED off during a $+dV_{CM}/dt$ transient, since all the current flowing through C_{LEDN} must be

supplied by the LED, and it is not recommended for applications requiring ultra high CMR₁ performance. The alternative drive circuit which like the recommended application circuit (Figure 19), does achieve ultra high CMR performance by shunting the LED in the off state.

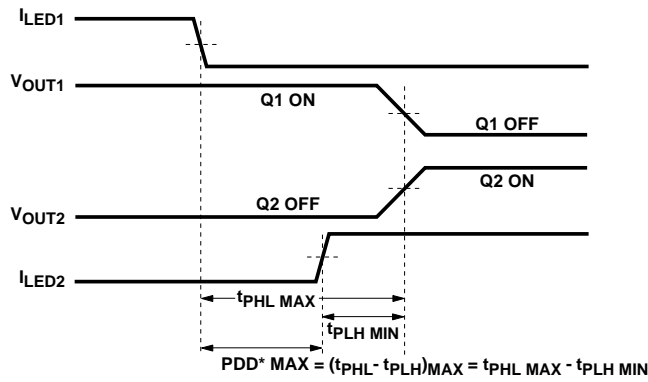
IPM Dead Time and Propagation Delay Specifications

The HCPL-3140/HCPL-0314 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time high and low side power transistors are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices from the high-voltage to the low-voltage motor rails. To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 26. The amount of delay necessary to achieve this

condition is equal to the maximum value of the propagation delay difference specification, PDD max, which is specified to be 500 ns over the operating temperature range of -40° to 100°C.

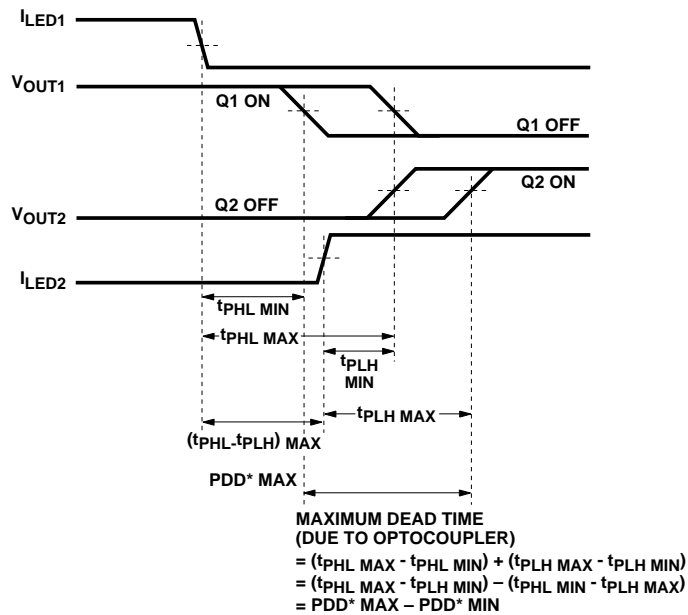
Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 27. The maximum dead time for the HCPL-3140/HCPL-0314 is 1 μs (= 0.5 μs - (-0.5 μs)) over the operating temperature range of -40°C to 100°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.



*PDD = PROPAGATION DELAY DIFFERENCE
 NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 26. Minimum LED Skew for Zero Dead Time.



*PDD = PROPAGATION DELAY DIFFERENCE
 NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 27. Waveforms for Dead Time.

www.agilent.com/semiconductors

For product information and a complete list of distributors, please go to our web site.

For technical assistance call:

Americas/Canada: +1 (800) 235-0312 or (916) 788-6763

Europe: +49 (0) 6441 92460

China: 10800 650 0017

Hong Kong: (+65) 6756 2394

India, Australia, New Zealand: (+65) 6755 1939

Japan: (+81 3) 3335-8152 (Domestic/International), or 0120-61-1280 (Domestic Only)

Korea: (+65) 6755 1989

Singapore, Malaysia, Vietnam, Thailand, Philippines, Indonesia: (+65) 6755 2044

Taiwan: (+65) 6755 1843

Data subject to change.

Copyright © 2005 Agilent Technologies, Inc.

Obsoletes 5989-2138EN

April 21, 2005

5989-2940EN



Agilent Technologies

SUNSTAR 商斯达实业集团是集研发、生产、工程、销售、代理经销、技术咨询、信息服务等为一体的高科技企业，是专业高科技电子产品生产厂家，是具有 10 多年历史的专业电子元器件供应商，是中国最早和最大的仓储式连锁规模经营大型综合电子零部件代理分销商之一，是一家专业代理和分销世界各大品牌 IC 芯片和电子元器件的连锁经营综合性国际公司，专业经营进口、国产名厂名牌电子元件，型号、种类齐全。在香港、北京、深圳、上海、西安、成都等全国主要电子市场设有直属分公司和产品展示展销窗口门市部专卖店及代理分销商，已在全国范围内建成强大统一的供货和代理分销网络。我们专业代理经销、开发生产电子元器件、集成电路、传感器、微波光电元器件、工控机/DOC/DOM 电子盘、专用电路、单片机开发、MCU/DSP/ARM/FPGA 软件硬件、二极管、三极管、模块等，是您可靠的一站式现货配套供应商、方案提供商、部件功能模块开发配套商。商斯达实业公司拥有庞大的资料库，有数位毕业于著名高校——有中国电子工业摇篮之称的西安电子科技大学（西军电）并长期从事国防尖端科技研究的高级工程师为您精挑细选、量身订做各种高科技电子元器件，并解决各种技术问题。

微波光电部专业代理经销高频、微波、光纤、光电元器件、组件、部件、模块、整机；电磁兼容元器件、材料、设备；微波 CAD、EDA 软件、开发测试仿真工具；微波、光纤仪器仪表。欢迎国外高科技微波、光纤厂商将优秀产品介绍到中国、共同开拓市场。长期大量现货专业批发高频、微波、卫星、光纤、电视、CATV 器件：晶振、VCO、连接器、PIN 开关、变容二极管、开关二极管、低噪晶体管、功率电阻及电容、放大器、功率管、MMIC、混频器、耦合器、功分器、振荡器、合成器、衰减器、滤波器、隔离器、环行器、移相器、调制解调器；光电子器件和组件：红外发射管、红外接收管、光电开关、光敏管、发光二极管和发光二极管组件、半导体激光二极管和激光器组件、光电探测器和光接收组件、光发射接收模块、光纤激光器和光放大器、光调制器、光开关、DWDM 用光发射和接收器件、用户接入系统光收发器件与模块、光纤连接器、光纤跳线/尾纤、光衰减器、光纤适配器、光隔离器、光耦合器、光环行器、光复用器/转换器；无线收发芯片和模组、蓝牙芯片和模组。

更多产品请看本公司产品专用销售网站：

商斯达微波光电产品网：[HTTP://www.rfoe.net/](http://www.rfoe.net/)

商斯达中国传感器科技信息网：<http://www.sensor-ic.com/>

商斯达工控安防网：<http://www.pc-ps.net/>

商斯达电子元器件网：<http://www.sunstare.com/>

商斯达消费电子产品网：<http://www.icasic.com/>

商斯达实业科技产品网：<http://www.sunstars.cn/> 射频微波光电元器件销售热线：

地址：深圳市福田区福华路福庆街鸿图大厦 1602 室

电话：0755-83396822 83397033 83398585 82884100

传真：0755-83376182 (0) 13823648918 MSN: SUNS8888@hotmail.com

邮编：518033 E-mail:szss20@163.com QQ: 195847376

深圳赛格展销部：深圳华强北路赛格电子市场 2583 号 电话：0755-83665529 25059422

技术支持：0755-83394033 13501568376

欢迎索取免费详细资料、设计指南和光盘；产品凡多，未能尽录，欢迎来电查询。

北京分公司：北京海淀区知春路 132 号中发电子大厦 3097 号

TEL: 010-81159046 82615020 13501189838 FAX: 010-62543996

上海分公司：上海市北京东路 668 号上海赛格电子市场 D125 号

TEL: 021-28311762 56703037 13701955389 FAX: 021-56703037

西安分公司：西安高新开发区 20 所(中国电子科技集团导航技术研究所)

西安劳动南路 88 号电子商城二楼 D23 号

TEL: 029-81022619 13072977981 FAX:029-88789382