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Agilent HCPL-8100/0810 In 7Vpp Isolated Powerline Communications

Application Note 5087

Introduction

While 3.5Vpp output voltage of HCPL-8100/0810 line driver at full load is sufficient for most powerline communications, some applications such as AMR (Automated Meter Reading) call for higher carrier signal voltages. Class-122 of EN50065-1 regulation allows up to 7Vpp signal voltage at the powerline mains for carrier frequency between 95kHz and 148.5kHz. A simple method to double (increase by 6dB) the output voltage yet without sacrificing the current driving capability exists – it is done through cascading 2 line drivers in series as shown in the above schematic drawing (Figure 1). For carrier frequencies <70kHz, more than 7Vpp powerline signal voltage is allowable under the same CENELEC Regulation. This is still achievable by increasing the turns-ratio of the signal transformer T1.

Detailed description of the configuration is given below:

A 3x gain is set for the first line driver (U1) assuming maximum input signal is 1.75Vpp. Vout1 will be 3.5Vpp. Due to inverting effect of HCPL-8100/0810, the output of U2 at Vout2 is also 3.5Vpp but at 180° out of phase with Vout1. The effective signal level will be 7Vpp across the primary winding of T1. For different input signal levels at Vin, Gain of U1 (R2/R1) stage can be adjusted to get 3.5Vpp at Vout1. But to achieve 180° matching effect between Vout1 and Vout2, gain of U2 (R4/R3) should always be fixed at unity.

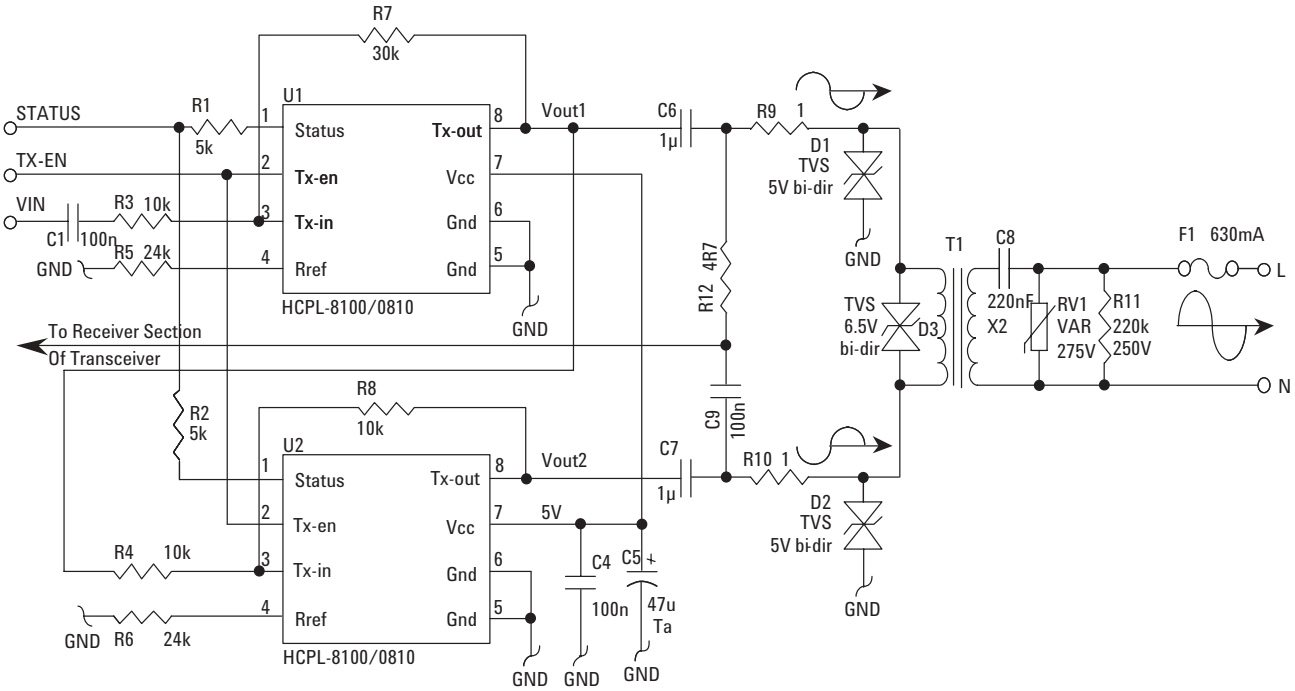

Figure 1. 7Vpp Applications Through Cascading 2 devices of HCPL-8100/0810 in Series

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External resistors R9 & R10 are recommended if the powerline impedance is lower than 7Ω in order to limit the output current within 1App.

Surge/transient protections are provided with RV1 MOV (275Vac rated Metal Oxide Varistor), D1/D2 TVS (5V rated bi-directional transient voltage suppressor) and D3 TVS (6.5V rated/bi-directional). Fuse is selected according to MOV's rating. 6.5V rated D3 TVS (with minimum breakdown voltage of 7.22V) across powerline terminals is sufficient as the full-load signal level is only 7Vpp. For powerline application, it should be able to withstand 4kV of transient/ surge voltages according to EN50065-4-2 requirements. At such high transient/surge voltages, the terminal voltage of the D3 TVS will increase to a maximum voltage of 11V and the primary side voltage of T1 is protected at <11Vpp. Therefore, the maximum transient voltage experienced by both U1 & U2 devices is still within the acceptable 5.5V absolute maximum limit. No additional rail-rail diode protection is needed.

Powerline status such as short circuits or over-current will be available to the microcontroller through the STATUS pin. This pin acts as early warning system to prevent both U1 and U2 devices from catastrophic failures.

One important consideration before adopting the configuration as shown in Figure 1 is the phase delay of U2. If the phase delay displays by U2 is significant, the circuit will not work properly. It has been found from bench test that the standard phase delay is only about 30ns at 400kHz carrier frequency. This is negligible for most of the applications.

The close loop response of the circuit is as shown in Figure 2. Thick line represents the close loop voltage gain while the thin line shows the frequency response of the open loop voltage gain. The close loop response is flat for a carrier frequency range of 9kHz ~ 400kHz, makes it suitable for both CENELEC EN50065 and FCC Part 15 requirements.

As expected, harmonics (HD2 & HD3) performance of the configuration are still acceptable - both at -62dBc for 100kHz carrier frequency. Tested at 50Ω CISPR 16 load with 7Vpp signal & 5V supply.

Figure 3 shows the typical load curve of the circuit taken at 120kHz carrier signal with varying loads from 0Ω to 100Ω.

Characteristics of the above circuit configurations

Vout = 7Vpp;
Iout = 1App maximum;
Freq. range: 9kHz ~ 400kHz;
U1 Gain: 3 (adjustable);
U2 Gain: 1 (fixed);
Phase Delay: 4.3º @ 400kHz;

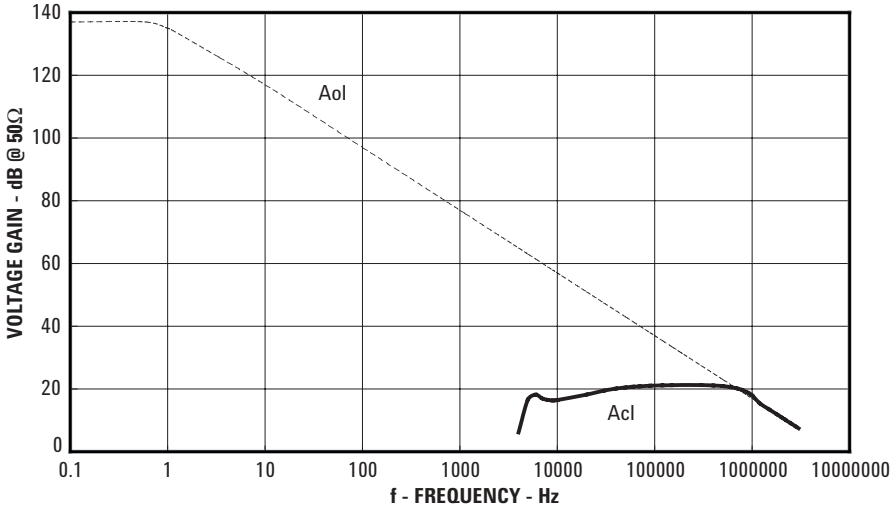

Figure 2. Close-loop Frequency Response of Figure 1

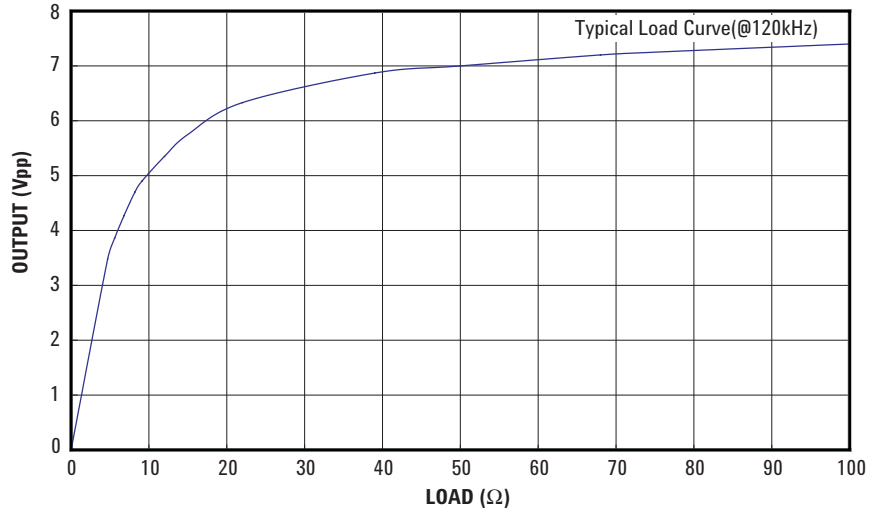

Figure 3. Typical Load Curve (0-100Ω)

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