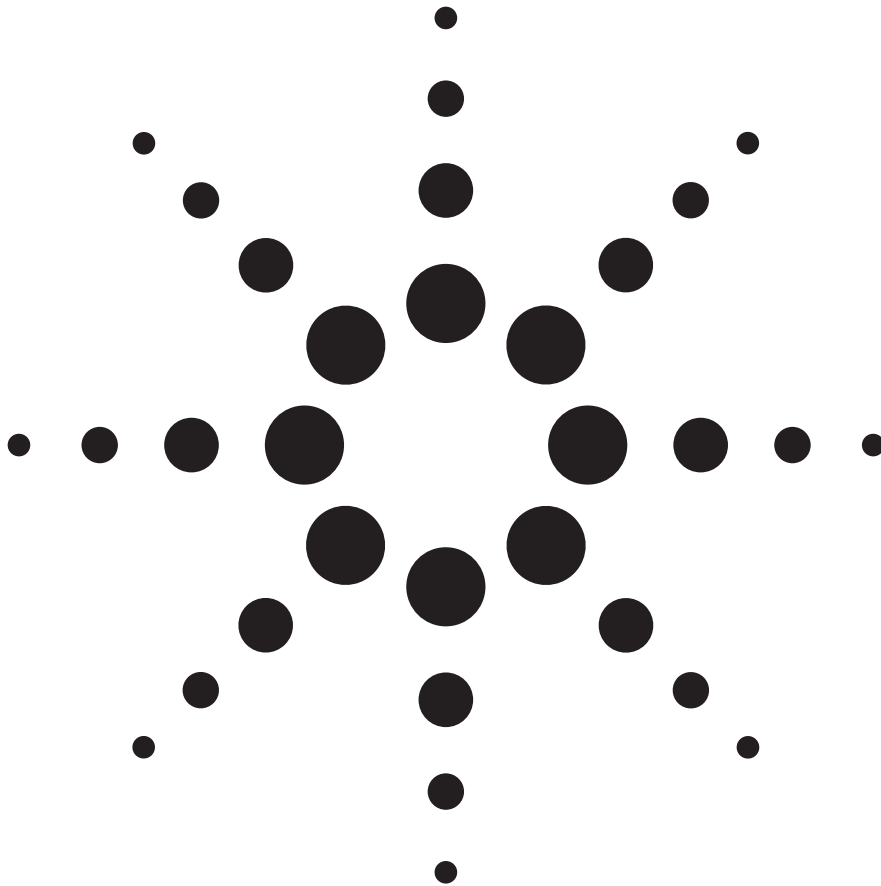


# Using 10 and 15 MBd Optocouplers and Optically- isolated Gate Drivers with AC Plasma Display Panels

White Paper



Agilent Technologies  
Semiconductor Products Group



## Introduction

A plasma display panel (PDP) is essentially a matrix of tiny fluorescent tubes that are controlled in a sophisticated fashion. There are two main types, DC and AC. The AC PDP has become the most commonly used because of its simpler structure and longer lifetime.

## Fundamentals of the AC Plasma Display Panel

A basic display cell shown in Fig. 1 comprises a pair of sustaining electrodes, Xi and Yi, surrounded by a dielectric. Located on the opposite glass substrate and running perpendicular to electrodes Xi and Yi is the addressing electrode Aj. Cells are filled with a mixture of neon and xenon gas that is ionized when the applied voltage exceeds its breakdown voltage. Ions with positive charges and electrons with negative charges collide when accelerated under the high-voltage electric field. Such collisions produce ultraviolet photons that excite phosphors to emit visible light. For color plasma display panels, in which the phosphors are vulnerable to damage from a positive charge, the discharge is controlled mainly between Xi and Yi electrodes, avoiding charges impinging directly on the phosphors deposited on top of the addressing electrode Aj.

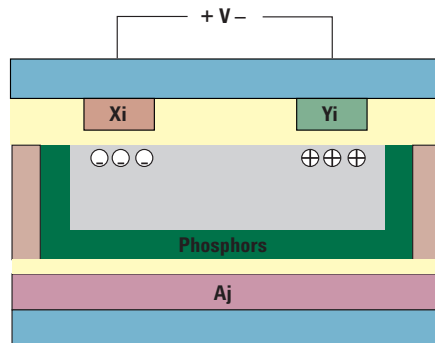


Figure 1. A Basic Display Cell.

Such a cell has only two states: ON and OFF. To display 256 gray scales an ADS (Address-Display-Separate) method is used to divide one frame into eight subframes whose display periods are sized in the ratio of 1:2:4:8:16:32:64:128. By selecting appropriate combinations of subframes the display intensity can be set to any one of the 256 levels of brightness.

Three phases—reset, write and sustain—are involved in displaying one subframe of an image. In the reset phase cells are initialized and the wall charges are cleared. In the write phase subframe data is written into the panel by write discharge to accumulate wall charges in the selected cells. In the sustain phase sustaining pulses are applied on all X and Y electrodes alternatively to cause AC current discharge in the panel and display the image.

A simplified representation of the electrode drive waveforms is shown in Fig. 2.  $V_{\text{reset}}$  is the reset pulse,  $V_a$  represents the image data,  $-V_{\text{sc}}$  is the row scan pulse and  $V_{\text{sus}}$  is the display sustaining pulse.

A timing allocation chart for the ADS technique is shown in Fig. 3. Each subframe is driven with the reset, write and sustain phases as shown.

In the NTSC system the video image is refreshed at a frequency of 60 Hz, with each frame lasting 16.7 ms. There are a total of 512 sustaining pulses in each frame, with two of them in the first subframe. If each sustain pulse lasts 5  $\mu\text{s}$  the total time for a display period in one frame is 2.6 ms. The remaining 14.1 ms is left for the reset and write periods. The reset and write period in each subframe should be  $14.1 \text{ ms}/8 = 1.8 \text{ ms}$ . If the reset period needs about 50  $\mu\text{s}$  the write period will take 1.75 ms, during which all rows have to be scanned. For high-resolution large panel displays involving 1920 x 1080 pixels there are 1080 rows to be scanned in 1.75 ms, thus the maximum pulse width of a row scan pulse is  $1.75 \text{ ms}/1080 = 1.6 \mu\text{s}$ .

For a high-contrast and high-brightness image best results are obtained when light is only emitted during the sustain phase—and the period of that phase should be as long as possible. However both reset and write pulses will cause discharge resulting in reduced contrast. Research has shown that the luminance is proportional to the rise and fall time of the driving pulse. Slow ramping of the reset pulse reduces the luminance created by such an unwanted discharge and improves the image contrast. Speeding up the ramping of the sustaining pulses and increasing the sustaining period enhances the image brightness. This means that the period of the write phase should be as small as possible so long it does not cause any write defects. Many methods have been found for the high-speed writing operation without compromising image quality.

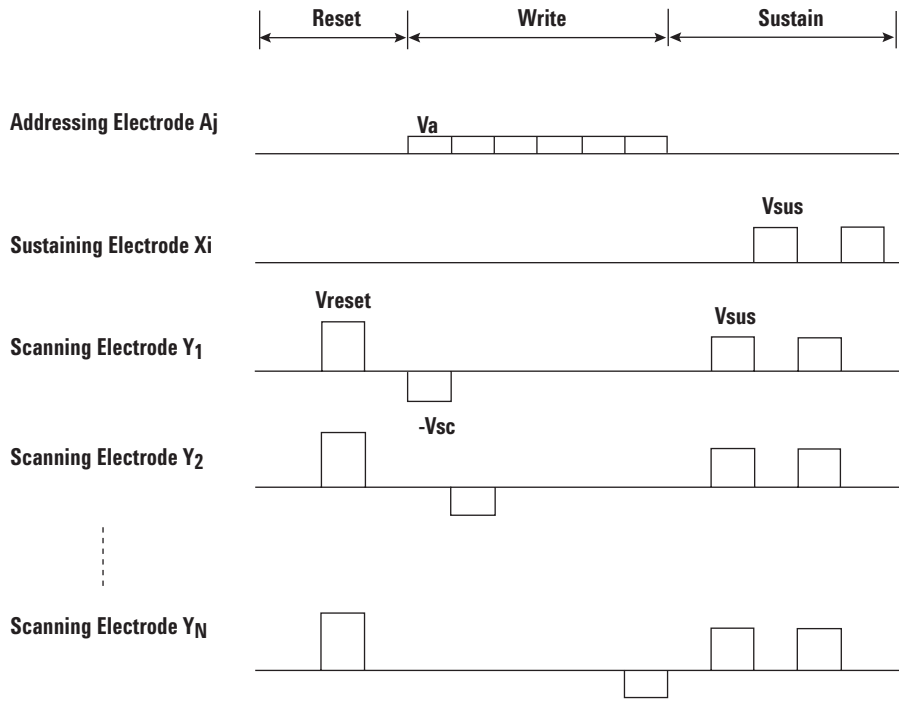


Figure 2. Basic Electrode Drive Waveforms.

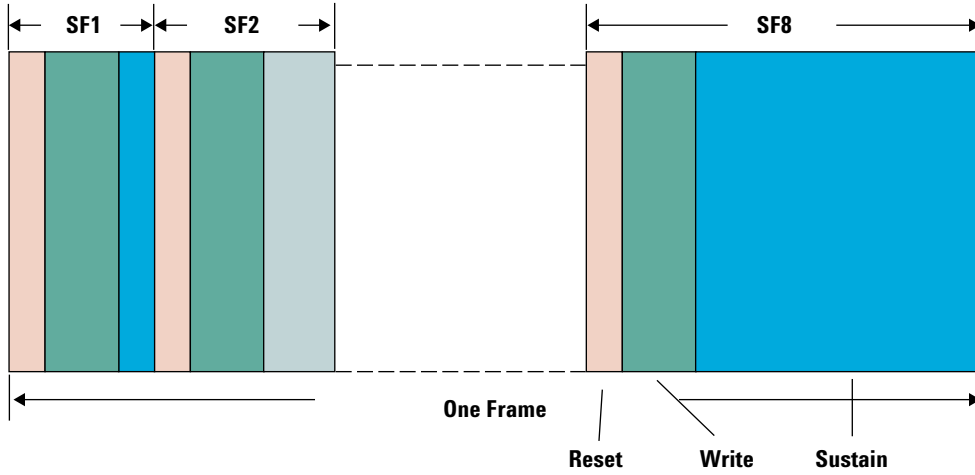


Figure 3. ADS Timing Allocation Chart.

### Panel Driving Circuitry

The electronic control and driving block diagram is shown in Fig. 4.

Scan electrodes  $Y_i$ , controlled by the scan controller and driver, run horizontally to scan the frame data row sequentially. Electrodes  $A_j$  run vertically to write column display data into the display cell at each intersection. Electrodes  $X_i$ , running in parallel with  $Y_i$ , are connected at

one end and controlled by a common sustain driver to apply high voltage pulses to the whole panel to display the image data.

### Design Considerations for Scan Driver IC Interface

The scan driver comprises several ICs capable of switching high voltage from the  $V_{pwr}$  node or  $V_{sub}$  node to each output  $Y_i$ , as shown in Fig. 5.

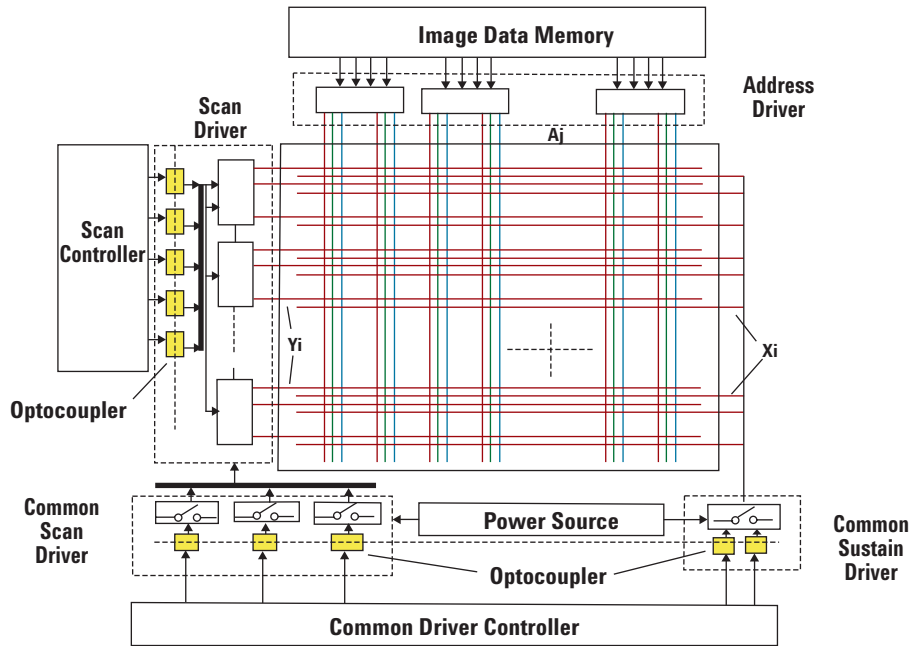


Figure 4. PDP Panel Block Diagram.

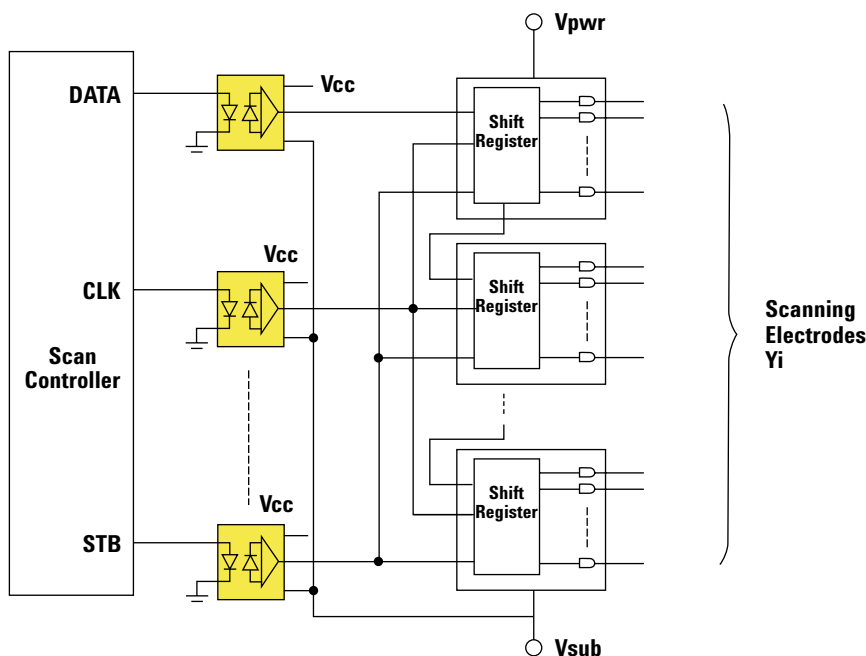


Figure 5. Scan Driver Block Diagram.

The scan driver ICs are floating on the  $V_{sub}$  node that can switch between various voltage potentials. Typically optocouplers are needed to level-shift the data, clock, strobe and other control signals from the control logic circuits to the scan driver ICs. The main considerations for choosing an appropriate optocoupler are speed, power dissipation, size, common-mode noise immunity and fanout capability.

The data rate of the row scan signal is approximately 1 MBd if the scan pulse width is 1  $\mu$ s, with the clock being 2 MBd for a 1-MBd data signal. Since the data signal and the clock signal are transmitted through the isolation boundary in parallel, the propagation delay difference between channels should be kept low to allow sufficient margin for the data to settle down before the clock signal can safely latch-in the data. Agilent Technologies HCPL-0738 dual-channel and HCPL-0708 single-channel 15 MBd optocouplers, and HCPL-0630 or HCPL-0631 10 MBd dual-channel optocouplers all have a maximum propagation delay skew which assures that the difference between channels will be less than 40 ns. For the Agilent HCPL-0600 or HCPL-0601 single-channel optocouplers, the propagation delay skew is typically higher. The HCPL-0630/0631 has an open collector output, and a pull-up resistor is needed for proper switching.

The image display of the plasma panel involves high frequency, high current charging and discharging, which means that a large amount of power is dissipated through the power switches. As an isolation and level-shifting device for the power electronics, the optocoupler has to be placed close to the power driver ICs. This means that the environmental temperature for the optocoupler is normally high at about +70°C to +85°C. Ideally the optocoupler should consume the least-possible amount of power to maintain the junction temperatures of both the LED and photo detector below a value that would cause deterioration in performance or lifetime. The total power consumption of an optocoupler can be calculated by:

$$P_T = P_{LED} + P_{Detector} = P_{LED} + P_{Static} + P_{Switching}$$

$$= I_{F(Average)} \cdot V_F + V_{cc} \cdot I_{cc} + C_{Load} \cdot V_{cc}^2 \cdot f$$

The total power dissipation is a function of the combination of steady-state supply current, LED driving current, switching frequency and load capacitance. In the typical PDP scan drive application the load is the capacitance of all the gates it is driving. At 1 MHz the switching power is typically less than 10 mW. The LED average current is about 5 mA given a 50% turn-on time. Therefore the power dissipated from the LED is around 7.5 mW with  $V_F$  at around 1.5 V. The dominant source of heat is the steady state power dissipation of the detector. The supply current of the HCPL-0738 is 16 mA maximum, resulting in less than 80 mW of total detector power dissipation. For the HCPL-0630/0631 the supply current is less than 11 mA, resulting in a power dissipation of less than 55 mW.

Demand for high resolution and large panel displays has required a greater number of driver ICs to be packed in the limited PCB board space, meaning that the size of the components in the PDP driver becomes more and more critical. Agilent Technologies dual-channel SO-8 optocouplers represents at least a 40 percent space saving compared with two single-channel devices.

### New 15 MBd CMOS Optocoupler Technology

Agilent now offers the industry's only dual-channel 15 MBd CMOS Optocoupler in a SOIC-8 package.

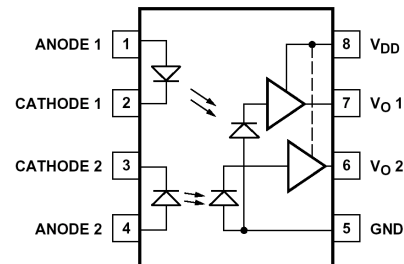


Figure 6. Functional Diagram of HCPL-0738.

The breakthrough combination of small size with low current consumption of 16 mA maximum at 5V nominal, 10 kV/ $\mu$ s minimum common-mode rejection and operation over the  $-40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$  temperature range is ideal for the drive circuits of plasma display panels. These optocouplers interface directly with conventional 5V CMOS logic circuitry,

To assure electrical safety, the HCPL-0738 optocoupler is UL recognized (3750  $V_{\text{RMS}}$  for 1 min. per UL 1577), recognized under CSA Component Acceptance Notice #5, and with a specified option (option 060) are IEC/EN/DIN EN 60747-5-2 approved. Agilent also offers the HCPL-0708, with the same performance in a single-channel version and integrated gate drive optocouplers for sustain driver applications.

In addition, the typical 20 kV/ $\mu$ s input-to-output common-mode transient immunity of the Agilent optocouplers ensures that row scan control data is transmitted error free across the isolation boundary. Without good CMR performance, signal corruption can lead to an erroneous row address, corrupting the displayed data for the entire row.

Currently available scan ICs typically have 40 to 64 outputs. For a large panel with very high resolutions of 1920 x 1080 pixels, one PDP would require 17 scan ICs. The clock signal is distributed after the isolation barrier to reduce the number of isolation devices required. Today most of the scan driver ICs are based on a CMOS process, thus the input driving current needed is very small, in the range of less than 10  $\mu\text{A}$ . To drive 17 gates the optocoupler has to deliver 170  $\mu\text{A}$ , which is well within the output driving capability of the Agilent high-speed optocouplers. Detailed specifications appear in Table 1.

Features	HCPL-0631	HCPL-0738 (CMOS Optocoupler)
General		
Area/Channel	15 mm <sup>2</sup>	15 mm <sup>2</sup>
Pull-up Resistor	Yes	Not Applicable
Operating Temp. Range	-40 to 85°C	-40 to 100°C
DC Parameters		
LED $I_{\text{th}}$	5 mA (max)	9 mA (max)
LED $BV_{\text{R}}$	5 V	5 V
$I_{\text{CCH}}$	15 mA (max)	15 mA (max)
$I_{\text{CCL}}$	21 mA (max)	18 mA (max)
$V_{\text{OL}}$	0.35 V (typ)	0.003 V (typ)
AC Parameters		
$T_{\text{PHL}}$	50 ns (typ)	35 ns (typ)
$T_{\text{PLH}}$	48 ns (typ)	20 ns (typ)
PWD	35 ns (max)	30 ns (max)
PD Skew	40 ns (max)	40 ns (max)
CMR	10kV/ $\mu$ s (typ)	15kV/ $\mu$ s (typ)

**Table 1. High-speed Optocoupler Specifications.**

### Design Considerations for Reset and Row Scan Pulses

The row scanning voltage  $-V_{sc}$  and reset voltage  $V_{reset}$  are connected to the scan driver IC via switch SW4 and SW2 respectively, as shown in Fig. 7. Such a switch can be implemented using a power MOSFET driven by an isolated gate driver optocoupler, as shown in Fig. 8.

For reset voltage pulses  $V_{reset}$ , switch SW2 needs to switch typically 100 A to 200 A of peak current as the voltage pulse is applied to the entire panel consisting of hundreds of rows of cells. Delivering a peak output current of 2 A, the Agilent HCPL-3120 2.0 A output current IGBT gate drive optocoupler could be used to directly drive such a MOSFET. If more output driving current is needed, a push-pull pair of power transistors, as shown in Fig. 9, can be used to boost the output drive capability.

### Design Considerations for Sustain Driver

The X and Y electrode sustaining pulses are applied to the whole panel to display data that has already been written into the cell during the write phase. Depending on the panel size the total charging current is between 100 A and 200 A. The power MOSFET used to switch such large amount of current usually has a large gate capacitance and requires a large amount of gate charge to turn on. There are two solutions to the MOSFET gate driver, the use of high-voltage integrated circuits (HVIC) or an optocoupler with a discrete MOSFET driver.

To increase the brightness of the displayed image the sustaining pulse should have a fast rise time. Thus the switching MOSFET needs to be driven by high gate charging current. The peak output current of an HVIC driver is typically 2 A, which may not be sufficient to turn on the MOSFET fast

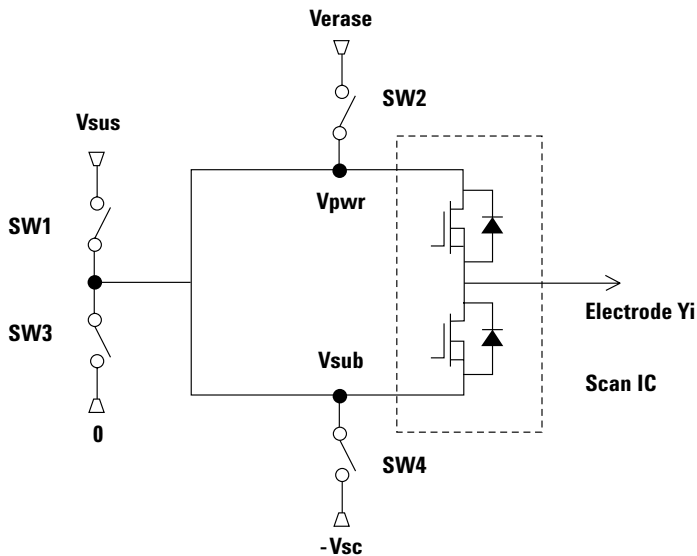


Figure 7. Scan Driver Circuitry.

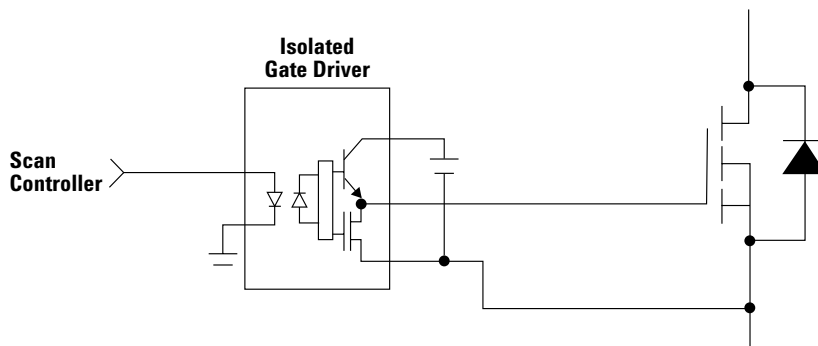


Figure 8. A MOSFET Switch Driven by an Isolated Gate Driver.

enough. To boost the driving capability a pair of power transistors, as shown in Fig. 9, can be inserted between the HVIC gate driver and the MOSFET. However such a solution requires more board space.

A single-channel MOSFET gate driver MIC4451/4452 from MICREL is capable of delivering a peak output current up to 12A, which is often sufficient for the sustain drivers. Together with the HCPL-0738 or HCPL-0631 dual-channel optocoupler, the MIC4451/4452 offers a space saving solution.

Another advantage of using an optocoupler is that it provides true isolation between logic ground and power ground. As the gate control signal is optically coupled to the power side there is no electrical connection between the logic side and power side. Thus the power ground bounce caused by high current and high frequency switching will not affect the logic ground and the control signal. This ground isolation greatly simplifies the PCB layout and component placement. In designs where an HVIC is used as a gate driver the layout of power ground and logic ground has to be carefully considered and tested, which is often not a trivial task.

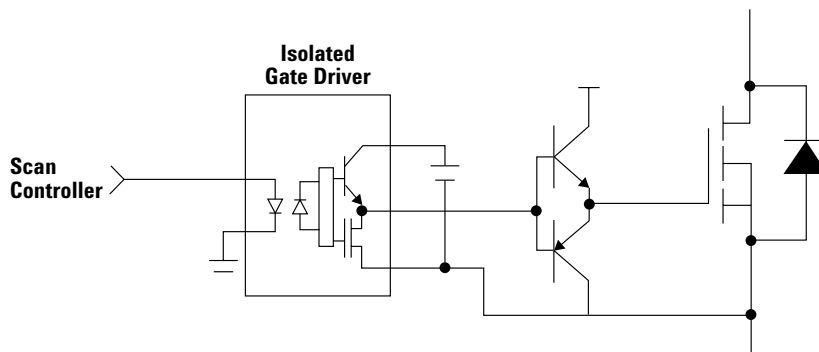


Figure 9. Gate Driver with Push-Pull Transistor Configuration.

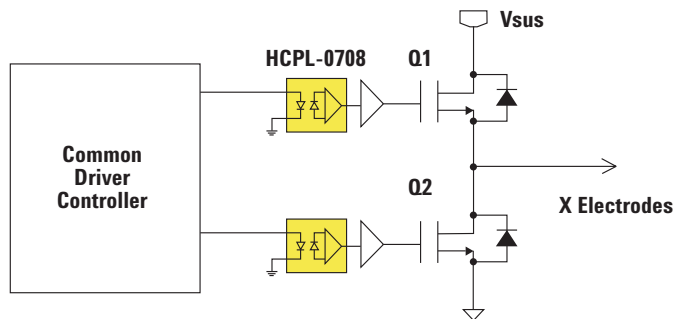


Figure 10. Sustain Driver Block Diagram.

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Obsoletes 5988-7010EN

March 2, 2004

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