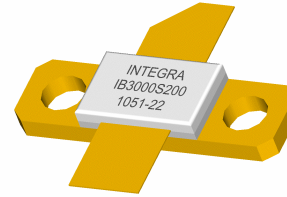


# Part Number: IB3000S200



## S-Band Radar Transistor

The high power pulsed transistor part number IB3000S200 is designed to operate in class C mode. This common base device supplies a minimum of 200 watts of peak pulse power under the conditions of 12 $\mu$ s pulse width and 1% duty cycle. All devices are 100% screened for large signal RF parameters. Excellent spectral stability into output mismatch over a broad input power range make it ideal for use in reliable high power solid state amplifiers.



- Silicon Bipolar
  - Ultra-high  $f_T$
- Class C Operation
  - High Efficiency
- Common Base Configuration
  - Single Power Supply
- Gold Metal
  - Maximum Reliability
- Emitter Ballasting
  - Optimum Thermal Distribution
- Internal Impedance Matching
  - Ease of Use
  - Ultra-low Loss Design
- BeO Package
  - Unmatched Thermal Reliability
- RF Test Fixture
  - Matched to 50 $\Omega$
  - Long-term Correlation
  - 100% Device RF Screening
  - No External Tuning Allowed
- US Patent Number
  - US 6181200 B1
  - US 6331931 B1

### TYPICAL DATA    TYPICAL DATA    TYPICAL DATA    TYPICAL DATA

General Information		Freq (GHz)	PW (us)	Duty (%)	V <sub>CC</sub> (V)	P <sub>IN</sub> (W)	IRL (dB)	P <sub>OUT</sub> (W)	G <sub>p</sub> (dB)	I <sub>c</sub> (A)	$\eta_c$ (%)	Droop (dB)
Date:	March 4, 2002	3.000	12	1	40.0	35.00	-24	281	9.0	16.20	43	-0.05
Assbly Lot - SN :	1256-1	3.000	12	1	40.0	31.19	-22	269	9.4	15.20	44	-0.10
Wafer :	940069-4	3.000	12	1	40.0	27.80	-22	247	9.5	13.80	45	-0.10
Test Fixture :	308/308	3.000	12	1	40.0	24.78	-21	231	9.7	13.00	45	-0.10
		3.000	12	1	40.0	22.08	-21	190	9.4	11.20	42	0.10
Date:	March 4, 2002	3.000	12	1	40.0	35.00	-26	240	8.4	16.40	37	-0.10
Assbly Lot - SN :	1256-3	3.000	12	1	40.0	31.19	-25	233	8.7	15.10	39	-0.05
Wafer :	940069-4	3.000	12	1	40.0	27.80	-25	223	9.0	13.70	41	-0.10
Test Fixture :	308/308	3.000	12	1	40.0	24.78	-24	214	9.4	13.00	41	0.10
		3.000	12	1	40.0	22.08	-24	193	9.4	11.40	42	0.10
Date:	March 4, 2002	3.000	12	1	40.0	35.00	-18	255	8.6	14.90	43	-0.10
Assbly Lot - SN :	1181-8	3.000	12	1	40.0	31.19	-17	254	9.1	13.60	47	-0.10
Wafer :	914301-2	3.000	12	1	40.0	27.80	-17	241	9.4	12.50	48	-0.10
Test Fixture :	308/308	3.000	12	1	40.0	24.78	-16	231	9.7	11.90	49	-0.10
		3.000	12	1	40.0	22.08	-15	202	9.6	10.50	48	0.10

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Collector-Emitter Voltage	$V_{CES}$	--	70	V	$V_{BE}=0V$ .
BD	Emitter-Base Voltage	$V_{EBO}$	--	3.5	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.10	°C/W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1$ .
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification.
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C.
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Collector-Emitter Breakdown Voltage	$BV_{CES}$	70	--	V	$I_C=40mA, V_{BE}=0V, T_F=25\pm5^\circ C$ .
100%	Zero Base Voltage Collector Leakage Current	$I_{CES}$	--	7.5	mA	$V_{CE}=40V, V_{BE}=0V, T_F=25\pm5^\circ C$ .
100%	DC Current Gain	$H_{FE}$	10	150	--	$V_{CE}=5V, I_C=0.1A, T_F=25\pm5^\circ C$ .

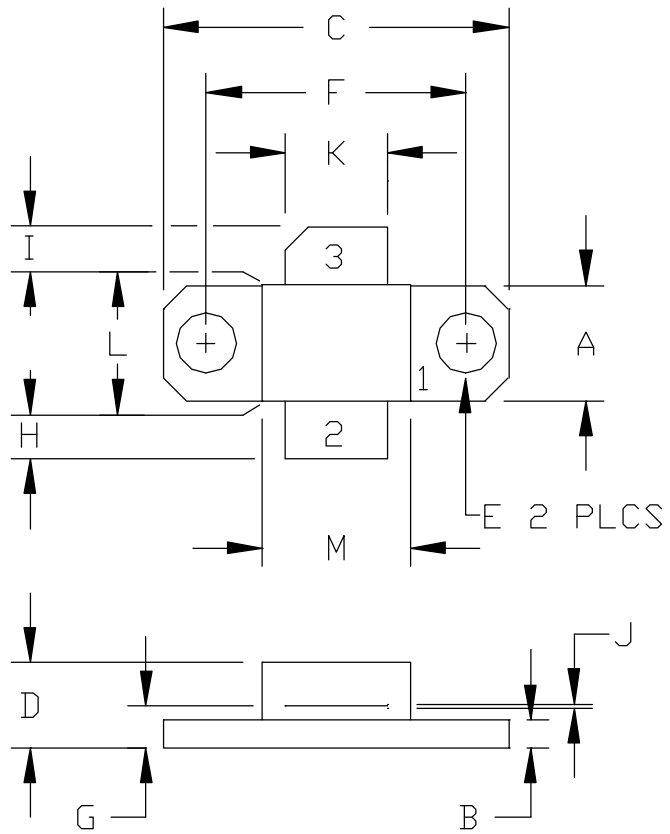
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	10	--	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Output Power	$P_{OUT}$	200	--	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Collector Efficiency ( $P_{OUT}/I_C/V_{CC}$ )	$N_C$	40	--	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Intra-Pulse Amplitude Droop	D	--	0.5	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Insertion Phase	IP	-30	+30	Deg	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Stability into 1.5:1 VSWR	VSWR-S	--	--	--	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$ Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
100%	3:1 Load Mismatch Tolerance	LMT	--	--	--	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$ Rotate 3:1 output VSWR through 360° phase. Post-test $P_{OUT} = \text{Pre-test } P_{OUT} \pm 10W.$
BD	Pulse Risetime	RT	--	100	ns	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$ Measure between 10% and 90% detected power points.
Note	$V1=40V; PW1=12\mu s; DF1=1\%; F1 = 3.000 \text{ GHz}, P_{IN1}=28.0W.$					
Note	$T_F = \text{Device flange temperature.}$					
Note	Screen 'BD' = parameter qualified By Design.					

**BROADBAND RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (GHz)	$Z_{IF}$ (W)	$Z_{OF}$ (W)
3.000	$2.0 - j4.9$	$0.9 - j4.0$
Impedance Definition		

**PACKAGE DIMENSIONAL OUTLINE DRAWING**



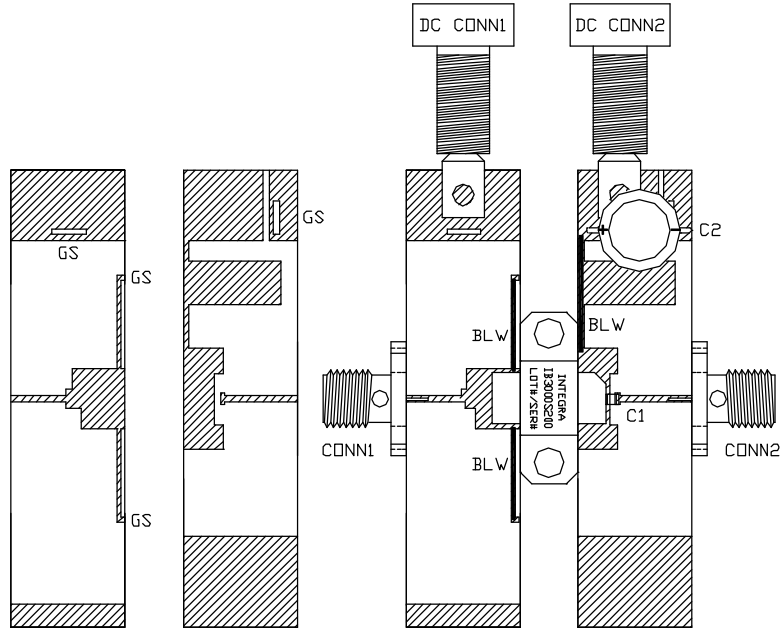
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.243	0.253	6.17	6.43
B	0.055	0.065	1.40	1.65
C	0.739	0.749	18.77	19.02
D	0.178	0.188	4.52	4.78
E	0.125	0.135	3.18	3.43
F	0.555	0.565	14.10	14.35
G	0.082	0.092	2.08	2.34
H	0.080	0.150	2.79	3.56
I	0.080	0.150	2.03	2.54
J	0.004	0.006	0.10	0.15
K	0.215	0.225	5.46	5.72
L	0.245	0.255	6.22	6.48
M	0.315	0.325	8.00	8.26

PIN SCHEDULE	
1	BASE
2	EMITTER
3	COLLECTOR

DOCUMENT NUMBER: IB3000S200	REV: PR1
SHEET NAME: 06-OUTLINE	REV: NC

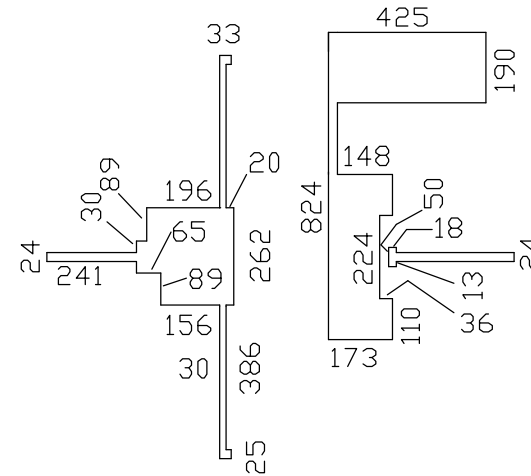
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**BROADBAND RF TEST FIXTURE**

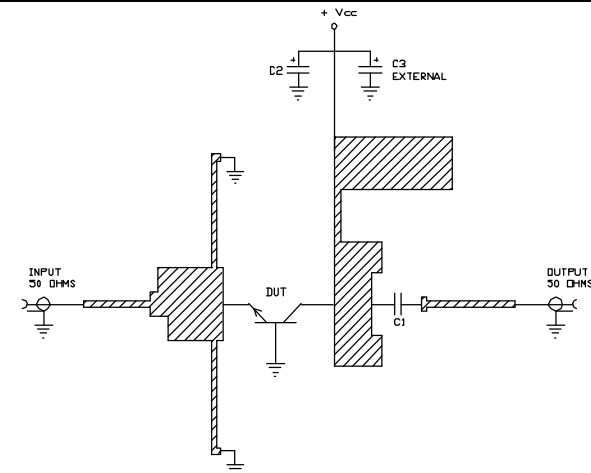


COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IB3000S200, MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #R03010, TH=0.025"
C1	CHIP CAPACITOR, TYPE ATC100A, 39 pF
C2	ELECTROLYTIC CAPACITOR, 68uF / 63V
C3	ELECTROLYTIC CAPACITOR, 4700uF / 50V
GS	GROUND SHIM, COPPER, TH=0.001"
CONN1, CONN2	SMA CONNECTOR, TYPE QS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS - 01
OUTPUT PC BOARD CARRIER	2 INCH BRASS - 01
TRANSISTOR CARRIER	2 INCH COPPER - 01
TRANSISTOR CLAMP	NORYL CLAMP -01
HEATSINK	2 INCH HEATSINK - 09
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
BLW	BIAS LINE WIRE - COPPER - 0.022" DIA TYPICAL
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

**ASSEMBLY AND PARTS LIST**



**CIRCUIT DIMENSIONS IN MILS (1 MIL = 0.001")**



**ELECTRICAL SCHEMATIC**

**DEFINITIONS****Data Sheet Status**

Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.

**Maximum Ratings**

Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

**WARNING****Product and environmental safety - toxic materials**

This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

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