FEATURED APPLICATION |

CMOS-Based Digital Step Attenuator Designs

DSAs are an elegant, natural interface between an A/D converter and the outside world.

|By Ray Baker

DSAs control RF levels through a processor-friendly interface. They find homes in many RF products such as wide dynamic range receivers, power amplifier distortion canceling loops, and throughout CATV distribution systems.

Usually "linear-in-dB," they are the natural interface between an ADC and the outside world. Compared to analog solutions, they offer higher accuracy, better temperature stability, and lower distortion. They also offer a smaller footprint, lower power, easier implementation, and are a more cost effective solution.

This article is based upon Peregrine Semiconductor's family of monolithic DSAs. While this article focuses on PE4302 and PE4304, 50 and 75Ω, 6-bit, DSAs, the technology is valid for all similar products. The article describes the general design methodology, the RF CMOS process, and performance of these devices.

Monolithic Attenuator Design

Figure 1 shows a classic step attenuator where each pad resides between two SPDT switches. Mechanical relays or switches offer practically lossless contacts, and with careful design, this structure can provide both low IL and excellent isolation.

Comparable performance in an integrated solution requires a solid-state switch with those same characteristics; metal-to-metal like resistance and sub pF open capacitance. FET based switches operated in their linear region can nearly fulfill this ideal. FET on-resistance (R_{ON}), though finite, can approach zero ohms with a large device. But large devices bring large cost. If there were a way to cut the number of series switches in half, i.e. replace each section's SPDT pair with a single SPST, then the performance and cost would improve.

Figure 2 shows an improved single-series-switch structure for a π-type attenuator. One series and two shunt SPST switches replace the two SPDT switches in each section. In practice, this technique indeed halves the IL of each section. SPST structures are also simpler than a SPDT and provide better performance, especially at high frequencies.

This series/shunt trick works analogously with other topologies such as the T and Bridged-T (see Figure 3), since all passive attenuators are three terminal networks. By training or tradition, engineers seem most comfortable with the π-type but in a monolithic circuit with wide resistor value spans, it may not be the best choice.

When doing a discrete design, resistor values are immaterial. In an IC, rectangular areas of a particular resistivity determine resistor values. About 200Ω/square is common in CMOS. The IC

GLOSSARY OF ACRONYMS

- ADC - analog-to-digital converter
- CAD - Computer Aided Design
- CATV - Cable Television
- CMOS - Complementary Metal Oxide Semiconductor
- C_{OFF} - OFF Capacitance of a FET
- dB - Decibel
- DSA - Digital Step Attenuator
- EEPROM - Electrically Erasable Programmable Read-only Memory
- ESD - Electrostatic Discharge
- FET - Field Effect Transistor
- GaAs - Gallium-Arsenide
- IC - Integrated Circuit
- IL - Insertion Loss
- IIP3 - Input 3rd Order Intercept Point
- IP3 - 3rd Order Intercept Point
- LSB - Least Significant Bit
- NVG - Negative Voltage Generator™
- P1 dB - One dB compression point
- pF - Picofarad
- PLL - Phase Lock Loop
- R_{ON} - On Resistance of a FET
- SPST - Single Pole Single Throw
- SPDT - Single Pole Double Throw
- SRAM - Static Random Access Memory
- UTSi® - Ultra thin silicon on sapphire process
- VCO - Voltage-Controlled Oscillator

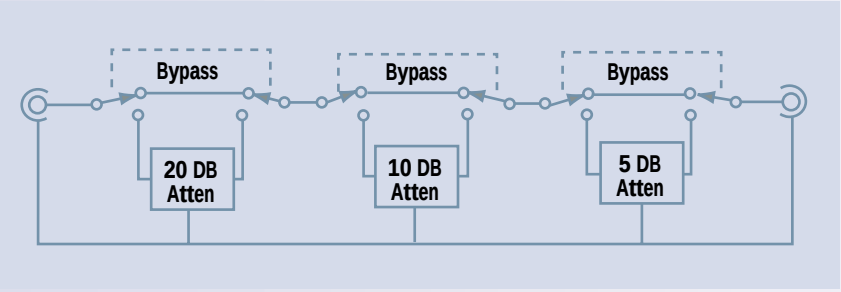

Figure 1. The classic step attenuator.

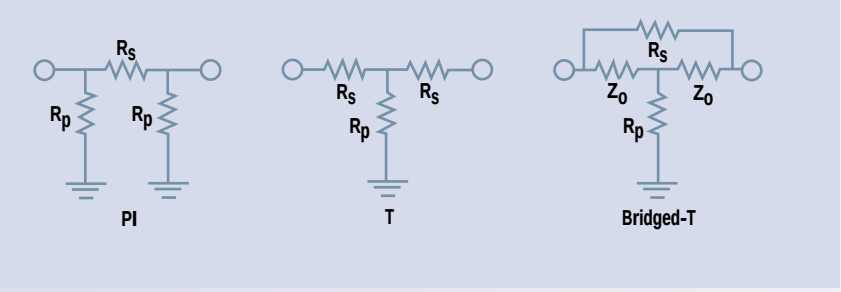

Figure 3. π, T, and Bridged-T circuits.

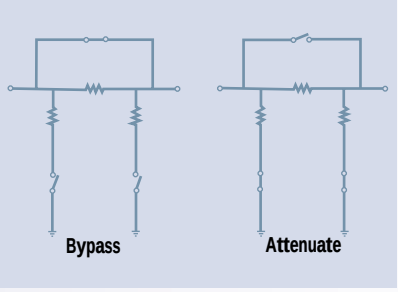

Figure 2. Single series switch π-attenuator.

Table 1. Resistor Values vs. dB and Topology.

	PI		T		Bridged-T	
dB	Rp	RS	RS	RP	RS	RP
0.5	1738	2.9	1.4	868	3.0	844
1	870	5.8	2.9	433	6.1	410
2	436	12	5.7	215	13	193
4	221	24	11	105	29	85
8	116	53	22	47	76	33
16	69	154	36	16	265	9.4

Table 2. UTSi® Performance vs. Geometry.

Geometry	F_T (GHz)	F_{MAX} (GHz)
0.25 micron	50	100
0.5 micron	15	40

dilemma is that resistor values, many multiples of or small fractions of, the 200Ω become a layout and manufacturing concern.

Both very large and very small resistor values claim large area and increase cost. Large values become long, thin rectangles, while small values grow wide to avoid tolerance problems. Table 1 shows the resistor values for a 50Ω 6-bit, binary attenuator with a 0.5 dB LSB. For each network R_p and R_s denote the values for the shunt and series resistors respectively.

Looking at the first row, 0.5 dB, the π- and T-networks require a ~600:1 (1738/2.9 and 868/1.4) resistor ratio. The Bridged-T requires half the resistor ratio, ~300:1 (844/3). At the 1 and 2 dB steps the Bridged-T retains this lower max/min ratio, cutting the resistor value span in half at the cost of one additional resistor.

At the larger steps, 4 dB or greater, the T-type R_p values shrink rapidly. Now the π becomes the preferred choice, thanks to a small resistance span (three resistors instead of four), and the larger R_p values in the shunt legs. This forms a general strategy: use the Bridged-T for small dB steps and the π for the larger increments.

In all cases, the best accuracy, linearity, process tolerance, and temperature tracking require that any resistor dominate the R_{ON} of an associated switch. For small dB values, the T configurations have a large R_p; hundreds of ohms. This large resistor value can absorb and dwarf the shunt switch R_{ON}, typically only a few ohms. Similarly, at the larger dB values, the π-type shunt resistor values are large and again dominate the shunt switch R_{ON}.

Optimization

Both low R_{ON} and low off capacitance (C_{OFF}) are essential for the series FET switch. Low R_{ON} gives best IL, but that implies a large device with significant C_{OFF}. High frequency operation requires a small C_{OFF} using a small device so that the series reactance and isolation is large. This contradiction can be satisfied by using the largest device that gives adequate isolation. For example, in a 1 dB section, 20 dB of series switch isolation is outstanding. With a section designed for 20 dB, that same 20 dB isolation gives a 17 dB net change for a 3 dB error. At this point a young Jedi engineer might say "OK, compensate with a larger attenuator value." That works in theory. But isolation is not very repeatable in practice and will vary greatly with small changes in C_{OFF}. Again, make sure each step has adequate but not excessive isolation.

Voltage rating is another optimization opportunity. Each series switch must handle a maximum voltage that is roughly proportional to its attenuation value. Small steps, for example, drop only a small portion of the incident voltage. The shunt switches are quite different. Imagine the attenuator in the zero dB configuration with all attenuators bypassed. Every shunt switch must then withstand the full input swing.

Whether series or shunt, any given switch may consist of one, two, three, or more FET devices in series. The expected voltage sets the number because multiple series FETs will divide and share the incident voltage swing to achieve a desired compression and intercept point. As the number of series devices grows, the transistor sizes must grow accordingly so that the composite R_{ON} and C_{OFF} remain about the same.

Looking inside the finished DSA product, the resistor values appear slightly higher than the Table 1 values. Each attenuator section adds a few tenths of a dB (the IL per section) to its designed value to give the correct net change. Finally, a few small valued, well-placed capacitors alongside the shunt resistors will counter the inherent high frequency corners. These high frequency tweaks degrade the return loss slightly but make a big improvement in flatness and accuracy.

Process Overview

The PE4302 and PE4304 are commercial digital step attenuator products fabricated with a proprietary ultra thin silicon on sapphire process under the moniker UTSi.

Geometry size is currently 0.5 micron with 0.25 micron on the horizon. Future UTSi RF CMOS products are challenging GaAs and other exotic recipes. Table 2 shows the measured F_T and F_{MAX} of the two UTSi geometries.

The sapphire substrate eliminates bulk effects (substrate capacitance) for outstanding RF performance and is inherently immune to latch-up. The insulating substrate enables large resistors and FET devices that are nearly free of

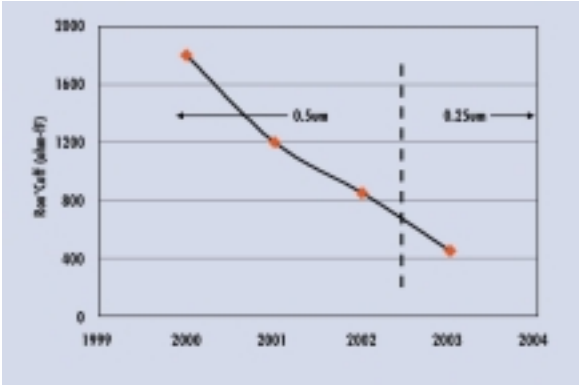

Figure 4. UTSi (R_{ON} / C_{OFF}) advancement vs. year.

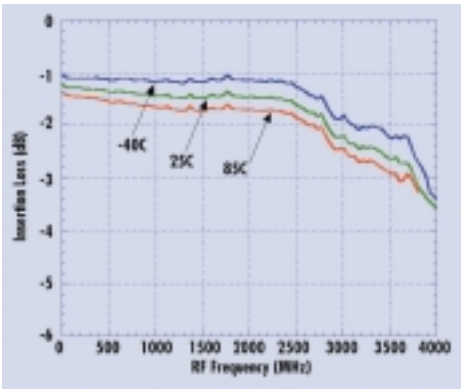

Figure 5. Typical IL vs. Temperature

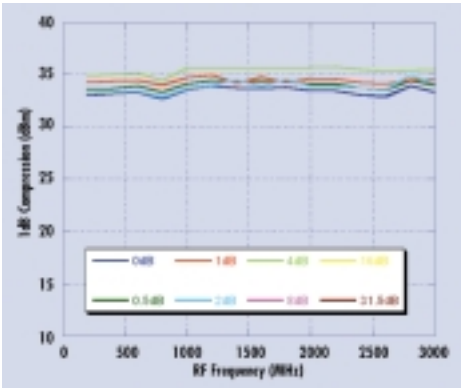

Figure 6. PE4302 one dB compression.

power and frequency robbing shunt capacitance. Sapphire also gives the necessary isolation for high accuracy, high attenuation DSAs.

RF CMOS also implies a plethora of monolithic mixed signal possibilities. Among the compatible, demonstrable blocks are: digital logic, EEPROM and SRAM memories, interface, linear, data-conversion, high IP3 mixers, low noise PLLs, VCOs, amplifiers, power management, and very high-Q RF passives. Specific capabilities in these the new DSA products include high ESD tolerance, high linearity to near DC, low IL, serial and parallel interface logic, and a proprietary ultra low noise negative voltage generator, all on a single die.

Most importantly, a high performance step attenuator requires a great RF switch and the (R_{ON}*C_{OFF}) product is the benchmark metric. The rapid design and process evolution described in Figure 4 brought Peregrine UTSi® to competitive parity in 2003.

PE4302 Measured Performance

Figure 5 shows the typical IL measured over the –40° C to +85° C temperature range. Imagine for a moment a DSA modeled as a single series resistor, a sensible approximation given the DSA switch arrangement.

Using the equation:

$$IL = -20\,Log\left[\frac{2Z_o}{2Z_o+R_{EQ}}\right]$$

the equivalent total series resistance, REQ, for 1.5 dB IL is about 18Ω, and represents the sum of six switches. Averaged, each switch is about 3Ω; a figure consistent with CAD models. Compared to other DSAs on the market today, this 1.5 dB IL performance leads the industry.

Figure 6 shows the 1 dB compression point (P1dB) vs. frequency for the major steps. These values represent the actual, instantaneous performance and are consistently better than +33 dBm.

Continuous duty thermal and reliability considerations set the somewhat lower datasheet maximum power limit. This distinction is important for high peak-to-average wireless waveforms and a better indicator of high linearity.

The IP3, is critical in almost every wireless and CATV application. Figure 7 shows the various devices' IIP3. Each device was operated at +3 V supply.

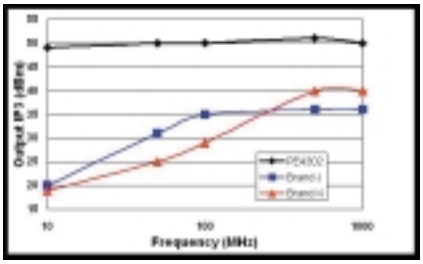

Figure 7. IIP3: Comparison at +3 volts and 0 dB (IL).

Observe the low frequency IIP3 roll off. Above 1 GHz, most DSA products indeed meet their marketing specs. But many DSA applications live in 10 to 300 MHz environments. CATV, for example, demands high linearity from as low as 5 MHz. While only a sampling of devices is presented, it is representative of GaAs parts in general (note low-end performance).

Return loss is another important specification. Many step attenuators operate alongside mixers and filters that are mismatch intolerant. Mismatch can also propagate through adjacent devices causing unexpected ripple, gain variations, and other problems.

Negative Voltage Generator™ Design

The devices focused on in this application (PE4302) include a selectable on-chip inverter that creates an internal –3 V reference. Unlike a classic flying capacitor charge pump, the Peregrine device uses a modified switching waveform and resistor/capacitor low pass filtering for low noise. These two strategies together create a circuit dubbed the Negative Voltage Generator™. Figure 8 shows the spurious energy of a GaAs DSA with a conventional charge pump. Spurs reach as high as –70 dBm across a wide bandwidth.

Figure 9 shows the spectrum of the Peregrine device under the same conditions. The set up consisted of a spectrum analyzer, with R_{BW} = V_{BW}= 10KHz, REFLVL = –70 dBm, preceded by a vintage Hewlett Packard 50 MHz low noise amplifier (plots are gain adjusted). Other than a barely visible component near DC, the plot reflects the measurement noise floor.

Figure 10 shows a close-in low frequency view using narrower filter bandwidths. This view subtracts the nominal powered-off noise floor, ~–135 dBm, to better show the NVG spurious components. With the NVG enabled and operating, power consumption of the whole device is only 10's of microamps at 3 V. An external –3 Volts at the Vss/GND pin completely disables the NVG.

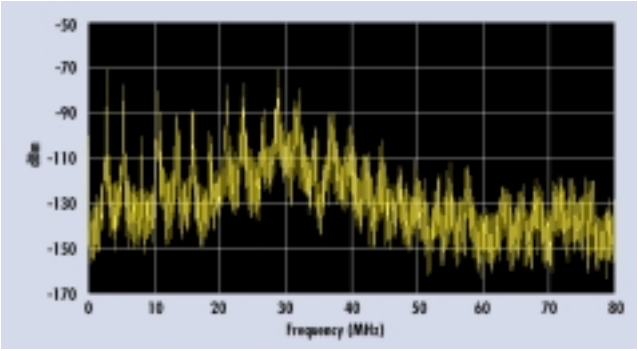

Figure 8. Typical GaAs / CMOS Hybrid DSA charge pump spurious.

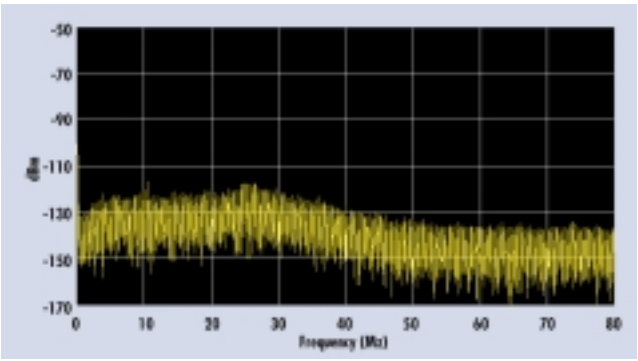

Figure 9. PE4302 NVG spurious.

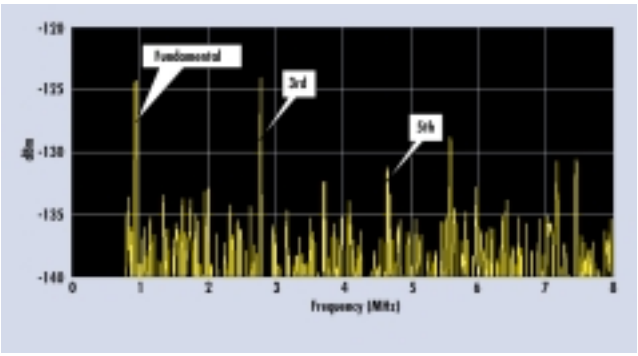

Figure 10. NVG spurious, expanded low frequency.

Added Functionality

Early during the design phase of the CMOS chip, two unused pins were identified. They were PUP1 and PUP2. It was decided to use them to set the power-up attenuation state to one of four values: 0, 8, 16, or 31 dB. This preset offers real advantages for transmitter lineups. Setting the power-up state to max attenuation inhibits the output while the controllers and various loops settle to their nominal, legal states. Potential spurious is blocked before it reaches the antenna and the A-I-R.

Monolithic CMOS is a huge advantage because the additional logic for this function is practically free.

Summary

This progressive DSA design demonstrates new levels of broadband linearity and accuracy. Unlike many RF parts such design can be expanded to include interfaces and features sure to pique the interest of both the digital and system design communities.

About the author

Ray Baker received a BSEE from the University of Illinois - Urbana in '82, a MSCSD from the University of Houston - Clear Lake in '87, and completed additional graduate work at the University of South Florida. Work history includes telemetry systems at the Johnson Space Center, military and space subsystem design at E-Systems/Raytheon, and PLL signal sources at TRAK Microwave. He can be reached at: rbaker@peregrine-semi.com

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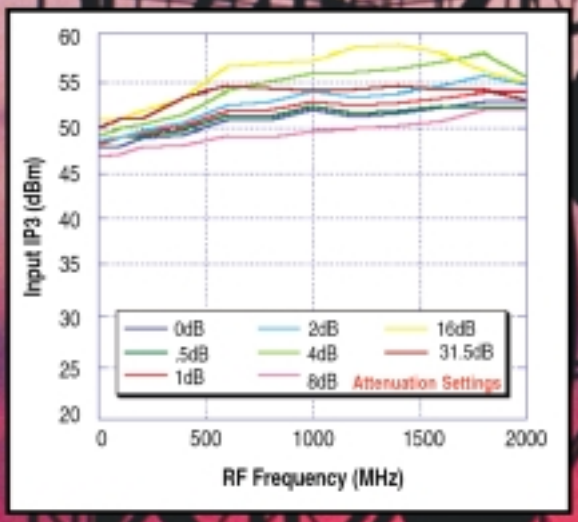

Parameter	Test Conditions	Frequency	Min.	Typ.	Max.	Units
Operation Frequency	—	—	DC	—	4000	MHz
Insertion Loss		DC-2.2 GHz	—	1.5	1.75	dB
Attenuation Accuracy	Any Bit or Bit Combination	DC<1.0 GHz	—	—	±(0.10 + 3% of atten setting)	dB
		1.0-2.2 GHz			±(0.15 + 5% of atten setting)	
1 dB Compression	—	10 MHz-2.2 GHz	30	34	—	dBm
Input IP3	Two-tone inputs up to +18 dBm	10 MHz-2.2 GHz	—	52	—	dBm

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