COVER STORY |

Integrating UltraCMOS Designs in GSM Front Ends

Today's handsets require an RF front-end that can select between transmit and receive, as well as select different frequency bands. New processes remove the size and bulk associated with traditional switching devices. |By Dylan Kelly

GLOSSARY OF ACRONYMS

ASM - Antenna switch module

BV_{DSS} - Breakdown voltage drain-to-source, gate shorted

CDMA - Code-division multiple access

CMOS - Complimentary metal oxide semi-conductor

GSM - Global System for Mobile Communications

ESD - Electrostatic discharge

HBM - Human body model

IC - Integrated Circuit

LTCC - Low Temperature Co-fired Ceramic

MEMS - Microelectromechanical System

PA - Power Amplifier

PAE - Power-added efficiency

pHEMT - Psuedomorphic High Electron Mobility Transistor

PIN - P+ - Intrinsic - N+

RX - Receive

SAW - Surface Acoustic Wave

SOI - Silicon-On-Insulator

SIMOX - Separation By Implantation of Oxygen

TX - Transmit

UMTS - Universal Mobile Communications System

Early handset designs could duplex between transmit and receive using a circulator (see Figure 1a). But supporting multiple bands, with the same design, requires multiple circulators. Such ferrite-based design makes the phone both bulky and expensive. And, in some cases, circulators will not work because their bandwidth is too limited.

Workable alternatives use RF switches (see Figure 1b) and banks of filters (see Figure 1c). But they too have have cost or size issue.

Today most CDMA phones have replaced the circulator with a duplexer filter, but multi-band CDMA requires an additional level of signal routing which is typically implemented with an RF switch in conjunction with duplex filters. Conversely, GSM phones operate on a time-duplexed basis, which lends itself naturally to a switch-only implementation of the front-end. This is due to duplex filters having much higher insertion loss than switches as the filters must split frequency bands, which are spaced by less than 3% of their frequency. In addition, duplex filters currently cannot tolerate GSM power levels.

Switching 101

There are many different switching technologies available, each with their own set of advantages and disadvantages. As GSM phones represent over 60% of worldwide handset sales and they are entirely based on switched front-ends, the remainder of this article will focus on the GSM system requirements and discuss how dif-

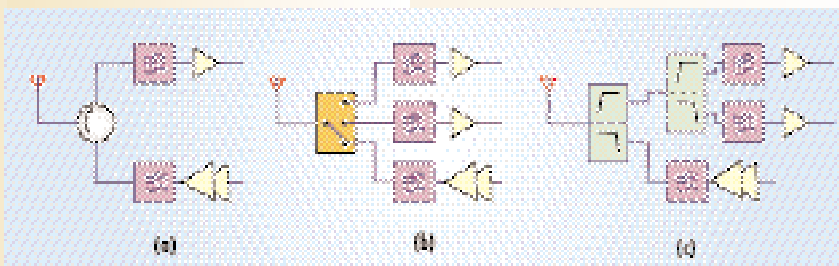


Figure 1. Duplexing can be implemented with a) a circulator b) a switch, or c) filter.

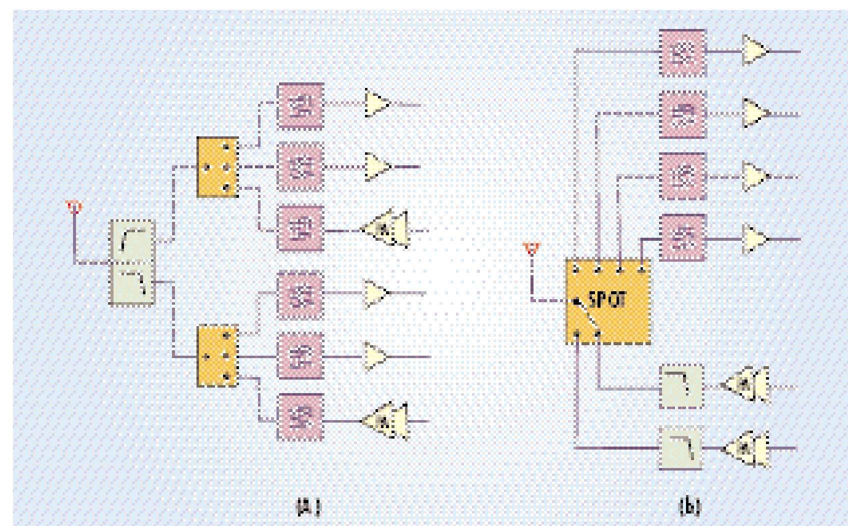
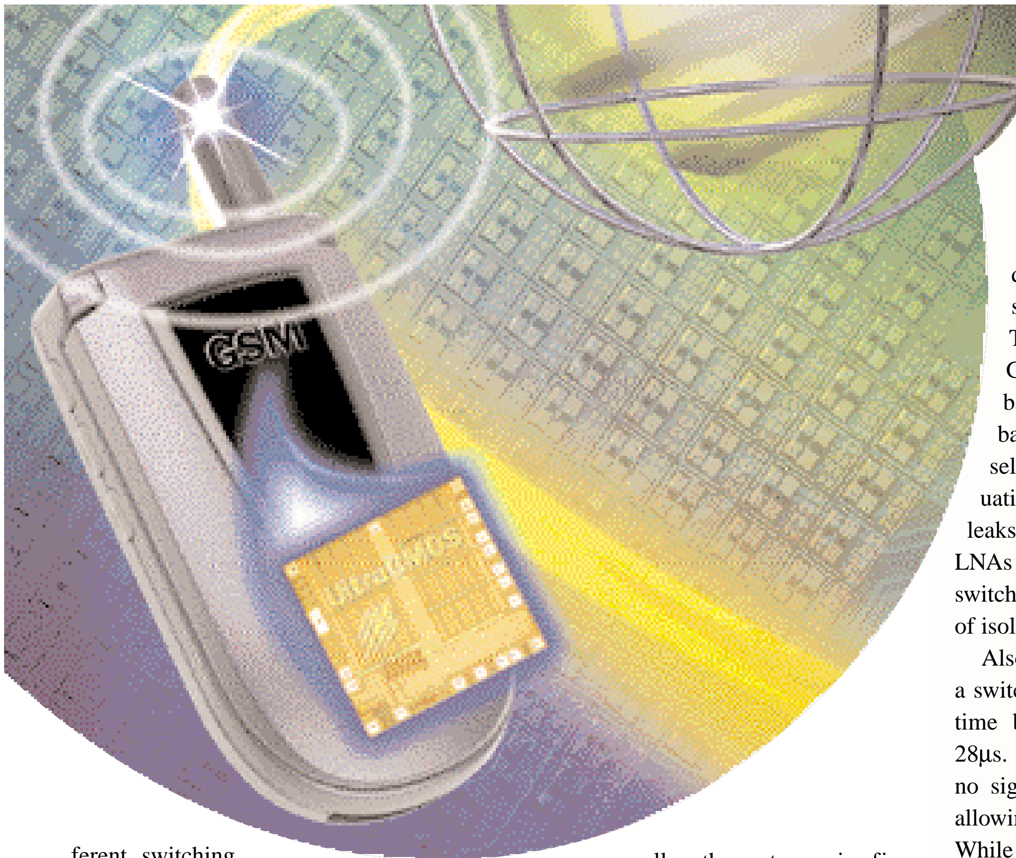


Figure 2. Example of front-end architectures for quad-band GSM.



ferent switching technologies address them. Also worth mentioning is integration of other standards, such as UMTS, into GSM handsets for next generation "World Phone" applications that will likely be handled through additional switched paths.

GSM Front-End Challenges

GSM phone functionality has expanded to support up to four different bands (see Table 1) of operation for coverage throughout the world, resulting in up to four transmit and four receive paths. Given the proximity of the adjacent TX bands, one power amplifier can cover GSM850 plus GSM while a second power amplifier covers the DCS and PCS bands. Each RX path requires an individual filters, typically a SAW filter, which results in a total of six paths. This configuration requires a single-pole, six throw switch. The simplest GSM handset only operates in a single band requiring only a single-pole, two throw switch.

In the quad-band phone designs, many different configurations of switches and filters can be combined to implement the single-pole, six throw function. While the configuration using a diplexer and two SP3Ts (see Figure 2a) has some benefits which will be discussed later, it results in higher insertion loss than the implementation with a true SP6T switch (see Figure 2b).

As the switching function occurs at the front-end of the phone, its insertion loss performance directly impacts both the effective PAE of the power amplifier as well as the system noise figure. While the increase in NF is directly equal to the insertion loss from the antenna to the LNA, the degradation in PAE is given by:

$$PAE = PAE \cdot 10^{[illegible]}$$

As GSM power amplifiers are run in saturation at up to two watts, their PAE is generally high at around 60%. This high efficiency is critical to the battery life of the handset since up to half of the total current drain is from the power amplifier. However, this high PAE can easily be wasted if a poor front-end architecture with high insertion loss is chosen. Figure 3 shows the effective power-added efficiency, PAE', versus insertion loss from the PA to the antenna for different power amplifier PAEs. An amplifier PAE of 60% is reduced to an effective PAE of only 42.5% if the insertion loss from the PA output to antenna is 1.5 dB. Any additional current consumption in the switching circuitry will further degrade the effective PAE.

Given the high output power requirement, up to +33 dBm ± 2 dB in the GSM band, the linearity requirements placed on the front-end are quite stringent. Linearity is specified in terms of harmonic suppression and all harmonics of the fundamental must be suppressed to below –30 dBm at frequencies up to 12.75 GHz.

While designers generally design for high isolation to unused paths to maintain low insertion loss, the triple and quad-band GSM systems present a special problem where the GSM TX band overlaps with the GSM850 RX band, and the PCS TX band overlaps with the DCS RX band. During transmit, the RX band-select filters do not provide any attenuation to the transmitted signal that leaks through the switch. To protect the LNAs which follow the RX filters, the switch itself must provide at least 35 dB of isolation.

Also specified in the GSM standard is a switching time requirement. The dwell time between transmit and receive is 28µs. When switching from RX to TX, no signal can be transmitted for 10µs, allowing for the switching event to occur. While 10µs is provided, system designers prefer switching times from 1 to 5µs to ensure the switch has reached steady state prior to the TX burst. Designers are conservative as the switch must meet the harmonic suppression requirement as soon as the PA is operating. Switching time from TX and RX is specified similarly, and the last 10µs of the 28µs dwell time is provided for switching states.

Since the front-end switch is connected directly to the antenna, the switch must have onerously high ESD tolerance. Handset designs must survive ± 8 kV contact discharge and ± 16 kV air discharge per the IEC 1000-4-2 specification. This ESD model has a series 330Ω resistor and 150 pF capacitor, making it significantly more damaging than the human-body model. The switch must withstand this stress, or additional protection components must be included.

Once all of the technical requirements have been addressed, there are additional constraints on size and cost of the front-end switching solution. Both area and height are restricted, with height requirements now dropping below 1.5 mm. As the front-end switch is usually integrated into multilayer substrates such as LTCC, industry-standard form factors have been established to provide a roadmap of size reduction. Technologies which shrink these ASMs are highly prized by phone manufacturers as the ASMs are generally the tallest package in the radio section. LTCC offers high quality-factor passive integration capability in the substrate, but adding passives requires additional LTCC layers which increase the thickness of the module. PA harmonic filters are integrated in the substrate, but frequently blocking capacitors and ESD protection are left outside of the module to reduce size and layer count. Some ASMs integrate a CMOS decoder as well as SAW filters on top of the LTCC.

There are several different switching technologies that can meet the technical requirements of GSM handsets. Each has its own set of advantages and disadvantages which are addressed in the next section.

Switching Solutions

The industry of solid-state switching was founded in the 1970s with PIN diode switches. Still the dominating technology in ASMs, PIN diodes achieve very low insertion loss and very low harmonic distortion. However, PIN diodes by themselves cannot complete an ASM. To bias the diodes, the module must include blocking capacitors and feed inductors. To build a multi-throw switch, series and shunt diodes are combined by quarter-wave transmission lines (see Figure 4a).

As a quarter-wavelength in LTCC at 900 MHz is several centimeters, these transmission lines drive the size of the diode-based ASMs.

GaAs pHEMT switches (see Figure 4b) have emerged as a viable replacement to PIN diodes by reducing the size and complexity of ASMs. Although PIN diode ASMs generally offer lower insertion loss, a market opportunity has opened for pHEMT switches as they reduce the size and hence cost of ASMs.

GaAs switches use multiple FETs per switching path and require one control line per path. Unlike PINs, pHEMT FETs cannot intrinsically tolerate the 17.8 V_{pk} GSM signal. By placing multiple FETs in series, the voltage can be divided across the devices to meet the power handling requirement. Shunt FETs can be added to improve isolation and increase immunity to load pulling from the isolated ports, but will double the number of control signals from six to twelve. To meet the GSM isolation requirement of 35 dB, shunt FETs or cascaded switches must be used.

To reduce the interface complexity with the pHEMT ASM, a CMOS

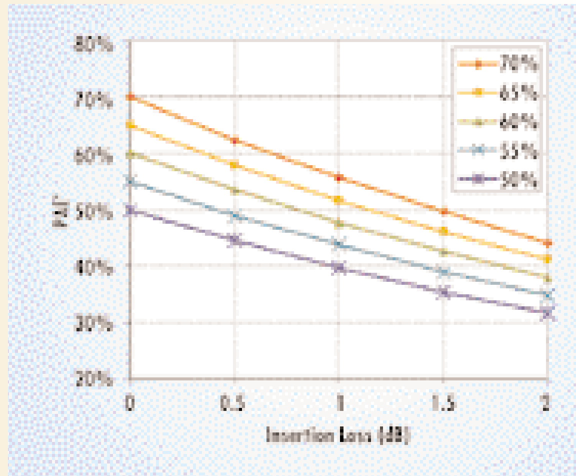


Figure 3. Effective PAE vs. insertion loss and different starting power amplifier PAEs.

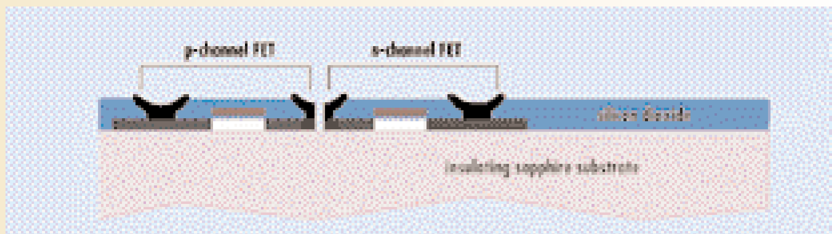


Figure 5. Construction of UltraCMOS devices.

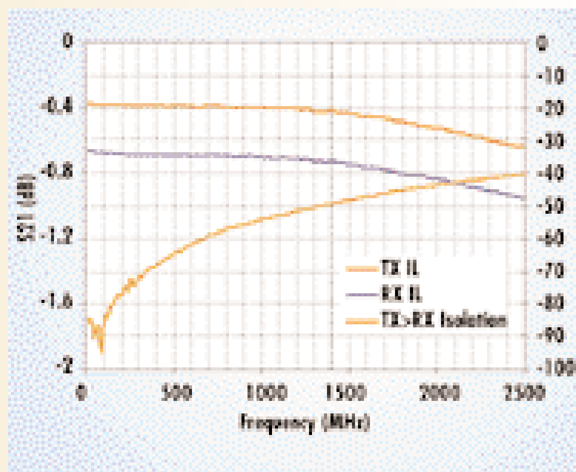


Figure 6. Insertion loss and isolation performance of SP6T switch.

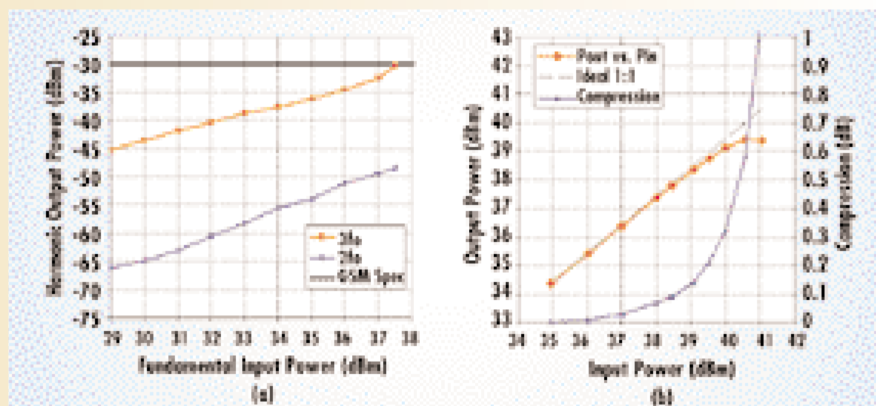


Figure 7. GSM linearity performance is shown by a) output harmonic powers versus input power and b) the compression behavior.

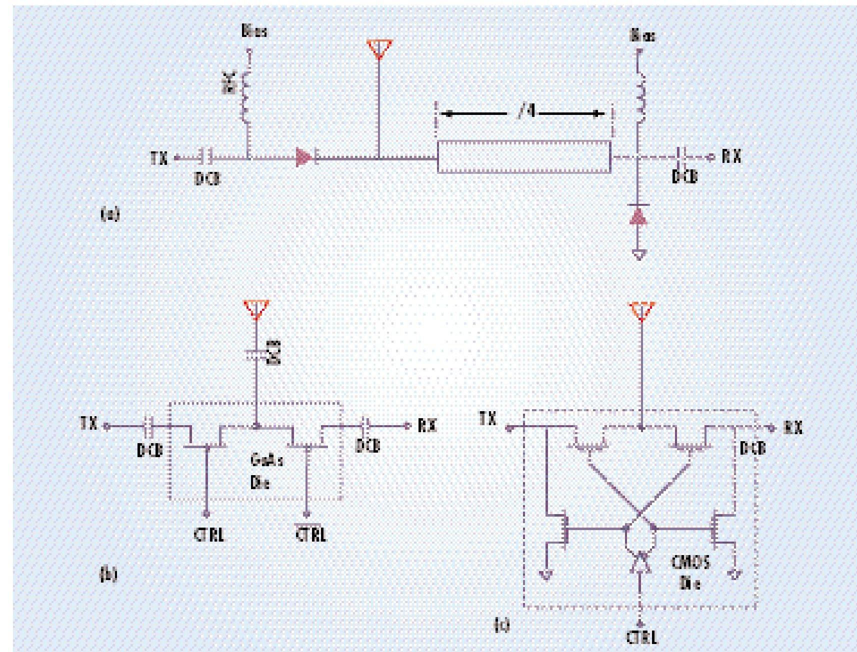


Figure 4. SP2T switches built with: a) PIN diodes, b) a GaAs IC, and c) an RF CMOS IC.

decoder chip is typically included in the ASM. While there are some pHEMT processes under development which include both enhancement and depletion mode devices, static digital logic still cannot be implemented because there is no complementary device in GaAs pHEMTs. The additional CMOS chip adds area and routing complexity. Care must be taken in the layout to prevent RF coupling to the control signals.

GaAs switches generally have low ESD tolerance, 250 to 500 V HBM, and require additional protection. This requirement in conjunction with difficulties in making a true SP6Ts has driven many ASM designers to use two SP3Ts combined with a diplexer. The diplexer provides ESD protection, but adds approximately 0.4 dB insertion loss to the design. An alternative implementation offered by several GaAs vendors is an SP4T switch cascaded with an SP3T on a single IC. The outputs of the SP4T are routed to the RX ports resulting in two switches in series between RX and TX. This provides adequate isolation to protect the LNAs in the band overlap region, but increases insertion loss and therefore noise figure.

GaAs switches are built with depletion-mode FETs which are on at 0 V_{GS}, and must have a negative V_{GS} lower than the pinch-off voltage to turn the device off. To work with positive control signals from CMOS logic, the FETs are DC blocked and the source and drains are biased up to VDD of the CMOS supply. This allows for 0 to V_{DD} signals to control the GaAs switch. The LTCC can integrate the blocking capacitors, although the capacitors add area and layers to the LTCC substrate.

MEMS are emerging as a potential solution for future front-end switching, although many challenges still stand in the way of MEMS replacing solid-state switches. Categorized as a passive technology, MEMS offer insertion loss as low as 0.1 dB in the GSM bands as well as adequate isolation. However, reliably handling the GSM power levels has yet to be demonstrated, and switching lifetime remains a concern. MEMS switching time, usually on the order of tens of microseconds, does not meet the GSM timing requirement. If the switching time can be reduced, the control interface is still problematic for GSM handsets.

Electrostatically controlled MEMS require tens of volts to switch states, and magnetostatically biased MEMS require tens to hundreds of mA. The final hurdles facing MEMS are size and cost reduction. Currently they must be packaged hermetically, so a new breakthrough is required in packaging to place MEMS on par with the existing solu-

Table 1. Worldwide GSM frequency bands.@cap:

	GSM850	GSM	DCS	PCS
	TX 824 - 849	880 - 915	1710 - 1765	1850 - 1910
	RX 869 - 894	925 - 960	1805 - 1880	1930 - 1990
Single Band		X		
Dual Band		X	X	
Triple Band		X	X	X
Quad Band	X	X	X	X

tions.

Recently RF CMOS has made inroads into front-end switching (see Figure 4c). Traditionally, RF CMOS has been relegated to only low voltage applications, but breakthroughs in device and circuit technologies have resulted in RF CMOS switches which meet all of the GSM requirements.

UltraCMOS* — CMOS on Steroids

RF CMOS processes today fall into two main categories — bulk silicon and silicon-on-insulator. Bulk CMOS has many disadvantages due to the drain and source to bulk diodes which lead most experts to believe that high power, high linearity switches can never be achieved in bulk. Unlike bulk, RF switches built in an SOI process place multiple FETs in series to handle high voltages much like GaAs switches.

A special subset of SOI is silicon-on-sapphire which is commonly referred to in industry as UltraCMOS. Unlike the silicon-based substrates used in bonded-wafer or SIMOX SOI processes, sapphire is essentially a perfect insulator. Parasitic capacitance to the substrate below incurs high insertion loss and low isolation. Very large RF FETs can be built in UltraCMOS with virtually no parasitic capacitance to ground for a nominal substrate thickness of 150 to 250 µm.

The basic construction of the UltraCMOS process is shown in Figure 5. The transistors are dielectrically isolated to provide latch-up immunity and high isolation. To achieve fully depleted operation, the silicon layer is very thin at approximately 1000 Å. With such thin silicon, the body terminal of the device is eliminated, making it a true three terminal device. UltraCMOS is manufactured on standard 6″ CMOS processing equipment, and fabrication on 8″ lines has been demonstrated. Demonstrated yields are comparable with other CMOS processes.

By stacking FETs in series, large voltages can be withstood despite the relatively low BV_{DSS} of a single off device. For example, a 3 V process can withstand 30 V if ten devices are stacked. However, to ensure correct voltage division across the stack, the parasitic capacitance from the FETs to the substrate must be negligible compared to the drain-to-source parasitic capacitance of the FETs, known as C_{OFF}. When device peripheries reach millimeters to achieve low total on resistance, a truly insulating substrate is required to ensure proper voltage division.

Loss and Isolation

Low insertion loss and high isolation can be achieved in UltraCMOS (see Figure 6). The SP6T architecture eliminates the diplexer requirement, significantly reducing the total insertion loss. To meet the IEC 1000-4-2 ESD requirement, a shunt 27 nH inductor followed by a series 33 pF capacitor at the antenna are sufficient. These values can be integrated into LTCC and contribute less than 0.1 dB to insertion loss.

Linearity Issues

The most difficult aspect of GSM switch design, particularly in a low voltage process, is meeting the linearity requirement. While arbitrarily high power handling can be realized by stacking as many devices as necessary, the stack should optimized to minimize die size while meeting the specification. This example switch has been designed to have P0.1 dB of +38.5 dBm and a P1dB compression point of +41 dBm. The harmonics versus input power as well compression behavior are shown in figure 7 with a supply voltage of 2.4 V.

At the maximum operating power of +35 dBm, the UltraCMOS switch has 6 dB of margin to the GSM specification of –30 dBm. The second harmonic is intrinsically low in UltraCMOS technology because distortion is symmetric on positive and negative voltage swings. This very low even order distortion is desirable in the GSM system as the second harmonic of the GSM transmit band lands in the DCS receive band.

Table 2. Performace Comparison of SP6T Implemented with Different Switch Technologies.

(Note that all specifications are maximum or minimum)

Parameter	Frequency (MHz)	PIN[1] Diodes	D-mode[2] pHEMT	Ultra CMOS	Units
RX Insertion Loss	1900	1.5	1.6	1.25	dB
	900	0.8	1.2	1.05	dB
TX Insertion Loss	1900	1.53[3]	0.9	0.85	dB
	900	1.23	0.7	0.75	dB
TX - RX Isolation	1900	20	-	37	dB
	900	30	40	45	dB
TX - TX Isolation	1900	20	-	23	dB
	900	20	22	26	dB
Harmonics	2fo	-32	-32	-43	dBm
(P_{in} = +35 dBm)	3fo	-32	-32	-35	dBm
Supply Voltage		2.4 - 2.8 V	2.5 - 5.0	2.4 - 2.8	V
Current Drain		10,000	80 per ctrl	20	µA
Integrated Decoder		no	no	yes	
Antenna ESD Tolerance (HBM)		-	0.5	4	kV

Note 1: PIN diode data is from a SP5T ASM
Note 2: GaAs SP6T is implemented as SP3T + SP4T
Note 3: Approximately 0.5 dB loss from PA harmonic filter is included

Sapphire — The Great Enabler

The sapphire substrate in the UltraCMOS process allows for unique flip-chip packaging capability. As sapphire is a ceramic, its coefficient of thermal expansion is well matched to LTCC. Sapphire is also the hardest substance after diamond, making it very tolerant of mechanical stress. Switches with these properties can easily be flip-chip mounted to an LTCC substrate without underfill, eliminating the area that had been required for wirebonding. True wafer-level chip-scale packaging is still under development and will ultimately produce switches which can be handled like a standard surface mount package.

The Final Analysis

The proprietary UltraCMOS SP6T switch described in this article performs comparably to PIN diode and pHEMT switches as is shown in Table 2. The pHEMT switch performance shown is for a SP6T implemented as an SP3T followed by an SP4T for the RX paths. The PIN diode data is for the case where the switch is built with series and shunt diodes combined by quarter-wave transmission lines.

UltraCMOS eliminates the decoder, blocking capacitors, and the diplexer. Combined with chip-scale packaging technology, UltraCMOS can dramatically reduce the size and thickness of LTCC ASMs. High inherent ESD tolerance and a three-control line interface simplify implementation and use. The high yield of UltraCMOS processes and scalability to additional switch throws provides a roadmap to higher levels of integration in the next generation of handsets.

***UltraCMOS is a trdemark of Peregrine Semi**

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Dylan Kelly leads large-signal IC design at Peregrine Semiconductor, a manufacturer of UltraCMOS-based products. During his tenure at Peregrine, he has developed high performance switching products for mobile wireless, infrastructure, broadband, and video applications. Dylan received his BSEE from the University of Texas at Austin in 2000 and is currently pursuing his MSEE at the University of California, San Diego. He can be reached at djkelly@psemi.com.

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