PEREGRINE SEMICONDUCTOR

AN3: Application Note

Using the PE3291 Fractional-N PLL in Narrow- Band / Paging Applications

Features

- Dual PLL, 1.2 MHz/550 MHz RF/IF capability
- Fractional ratios of 2, 4, 8, 16 or 32
- Excellent spurious output compensation
- Excellent phase noise when using small step sizes
- Very low operating power
- 3-wire serial port programming

Introduction

The PE3291 fractional-N PLL is well suited for use in low data rate (narrow channel spacing) applications below 1 GHz, such as paging, remote meter reading, inventory control and RFID. It offers superior phase noise for small step sizes, low spurious outputs and industry leading low power consumption.

Product Features

- Dual PLL, 1.2 GHz/550 MHz capability
- Fractional ratios of 2, 4, 8, 16 or 32
- Excellent spurious output compensation
  - Fractional spurs less than -65 dBc
  - No tuning or adjustment required
  - Stable across voltage, temperature and frequency
- Excellent phase noise when using small step sizes
  - 900 MHz with 12.5 kHz channel spacings
    - -78 dBc/Hz at 1 kHz offset
    - Less than 1 degree integrated phase error
- Very low operating power
  - < 7 mW from a 3-volt supply
  - < 6 mW from a 1.8-volt and 3-volt supply
  - < 4.0 mW from a 1.0-volt and 3-volt supply
- Standby current typically 5 µA
- 3-wire serial port programming

The PE3291 benefits for narrow-band/paging use

Improved phase noise at small step size / channel spacing

The fractional-N architecture of the PE3291 allows a factor of 32 increase in the comparison frequency, with a like decrease in the value of N, yielding a corresponding improvement in the phase noise inside the loop filter bandwidth. Standard integer-N PLLs require large values of N for small step sizes at high frequencies, leading to high phase noise inside the loop. The PE3291 is capable of a maximum division of 524,256. This gives a minimum step size of 2.289 kHz at the device's 1.2 GHz maximum output. Step sizes of 2.0, 2.5 and 3.125 kHz are practical in the 1 GHz region (even smaller step sizes can be done at lower frequencies).

Figures 1 through 4 show the results from the example circuit in Figure 5. The PLL conditions are given in Figure 5. Note that the loop was optimized to improve lock time, trading spurious suppression for wider loop bandwidth.

Figure 1. PE3291 PLL 1 Phase Noise

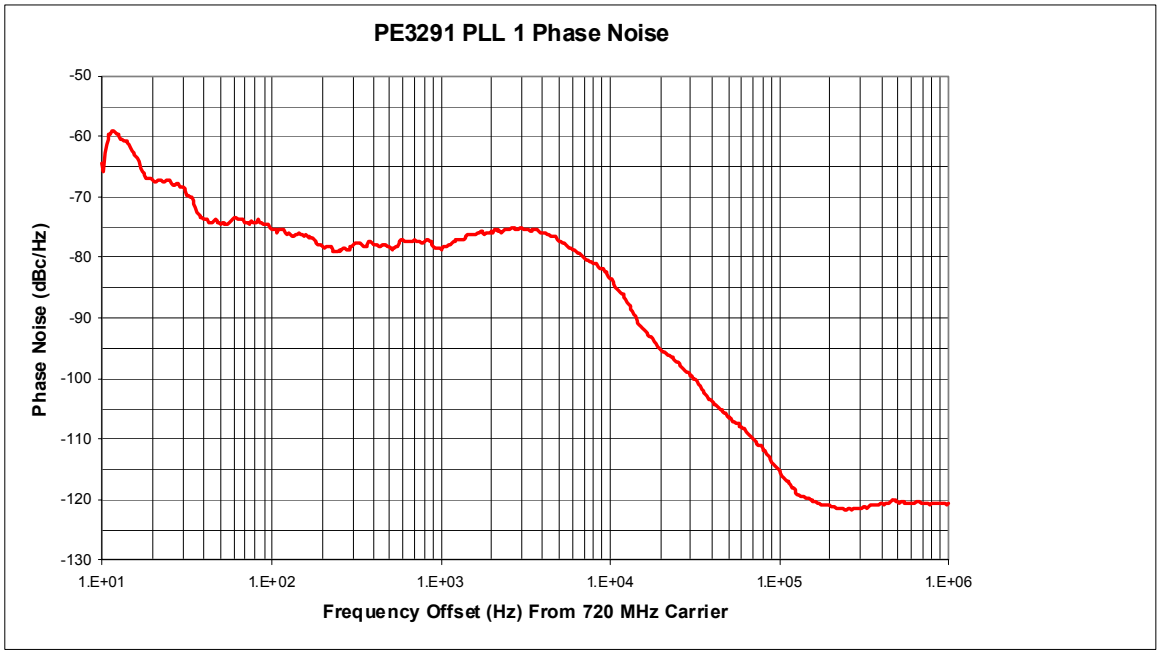
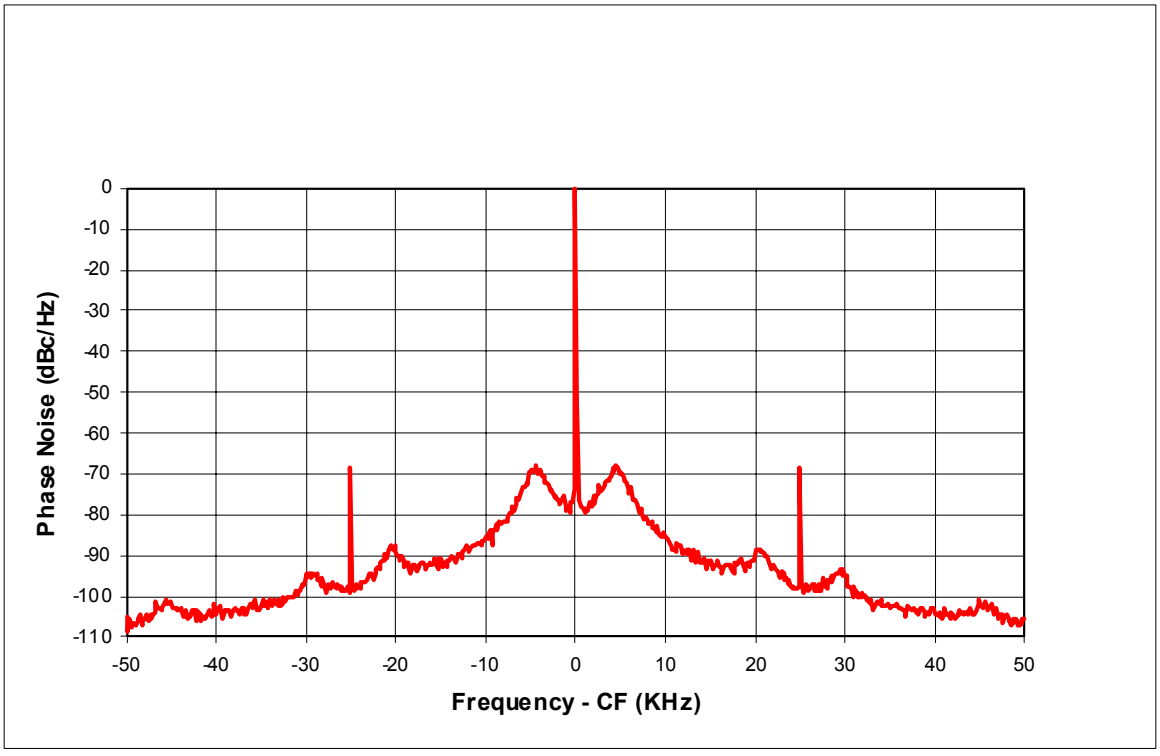


Figure 2. PE3291 PLL 1 Fractional Ratio Spurs



Excellent fractional spurious output suppression that is stable across temperature, voltage and frequency with no adjustments or tuning.

The PE3291 is generally capable of suppressing fractional spurious outputs to –65 dBc or less for fractional ratios of 32. For fractional ratios of 16, 8, 4 and 2 the fractional spur is farther from the carrier and will generally be further suppressed by the loop filter. The spurious suppression requires no tuning and is stable across temperature, supply voltage and output frequency.

The classic method of fractional spurious output compensation requires a compensating current to balance the errors in the phase detector. To suppress the fractional spurs by 20 dB requires a balance current that tracks the charge pump error to within 1%. In practice, it is difficult to maintain 1% regulation of a sub nano-ampere current source across temperature and voltage. Also, the calculated current is correct for only one frequency, a 1% frequency change will result in a 1% balance current error.

The Peregrine PE3291 uses an accumulate-and-average method to reduce the fractional spurious outputs. The outputs from the charge pump are stored on a 50 pF capacitor (100 pF on the IF side). The stored current on the capacitor is transferred to the loop filter by opening a pass gate each time the fractional accumulator returns to the base state. For a fractional ratio of 32, the pass gate will open after each 32 cycles of the phase detector and the main fractional spur will have an offset of 1/32 of the comparison frequency (which will usually be the channel spacing). If the value for F is 2, 6, 10, 14, 18, 22, 26 or 30 the resulting fractional ratio will be16 and the main spur will be at an offset of fr/16. For F = 4, 12, 20 or 28, fractional ratio will be 8. For F= 8 or 24, fractional ratio is 4. Fractional ratio is 2 for F=16.

Industry leading low power consumption

The PE3291 uses a typical power of 9.9 mW when operating at the maximum speed on loop 1 (RF to 1000 MHz, IF to 300 MHz). Power consumption drops to 7.5 mW with both PLLs set for low speed (RF to 700 MHz, IF to 300 MHz). The internal biasing is controlled by the programming software.

The PE3291 can further reduce power consumption if an external voltage is used to supply the prescalers. Full speed operation (RF to 900 MHz, IF to 550 MHz) can be achieved on 7.9 mW while reduced speed operation (RF to 450 MHz, IF to 300 MHz) can run on only 3.9 mW.

The ability to run at reduced power consumption with lower synthesized LO frequencies may lead to a preference for low side injection architectures.

Design considerations

When designing for best phase noise the preferred choice of fractional ratio is the highest practical value. This tends to lead to high comparison frequencies. As an example, a 10 kHz step size has a 320 kHz comparison frequency as the preferred choice. This may lead to restrictions in the choice of reference frequency. The 30, 15, 10, 7.5, 6 and 3 kHz series of channel spacings come from a 960 kHz comparison frequency (or integer division of 960 kHz). The 25, 12.5, 6.25 and 3.125 kHz channel spacings come from an 800 kHz comparison frequency. Reference frequencies which are a multiple of 4.8 MHz allow access to both series of comparison frequency (14.4 and 19.2 MHz are the most common).

The minimum value of N may become a limiting consideration for some of the larger channel spacings used in low data rate applications (25 kHz or 30 kHz). Values of N less than 1024 for PLL1 (256 for PLL2) may not be achievable. This is due both to the fractional-N architecture and to the 32/33 prescaler used in the RF main divider chain (16/17 in the IF chain). As an example, when using an 800 kHz comparison frequency with 25 kHz steps the lowest frequency before missing steps appear is 819.2 MHz. Between 818.4 MHz and 819.2 MHz none of the fractional values of N can be accessed.

Loop filter considerations

The loop filter components can be calculated using the standard PLL loop filter equations for either second-order or third-order passive loop filters driven by a charge pump. Peregrine has these available on its website at www.peregrine-semi.com (click on the Loop Filter Calc Button under the PE3291 product page). Note that the comparison frequency and the channel spacing are not the same in a fractional-N PLL. The proper number to use in the equations is the comparison frequency, as this determines how often the charge pump adds current to the averaging capacitor and thus sets the rate at which the charge pump drives the loop filter.

The channel spacing is determined by the comparison frequency divided by the fractional ratio. An 800 kHz comparison frequency and a fractional ratio of 32 give a step size of 25 kHz. The step size is the proper number to use in choosing the loop filter bandwidth, since it sets how often the integrating capacitor charge is output to the loop filter and how long the delay is between loop phase error detection and the corrective output to the loop filter. For best stability, the loop filter bandwidth should be a maximum of 10% of the step size. For a 25 kHz step size this would be a 2.5 kHz loop natural frequency.

Lock time

The PE3291has lock times comparable to other standard integer-N PLLs used with the same step size. When designing for best lock time, use the widest loop bandwidth practical. In general, a loop bandwidth that is 20% of the step size is the maximum practical value that maintains acceptable loop stability. F=1 is the condition that yields slowest lock time, and is also a worst case for fractional spurious output amplitude. Setting the increment value of the fractional accumulator to 1 implements the full fractional ratio of 32. Setting the fractional ratio to 16 (F=2, 6, 10, 14, 18, 22, 26 or 30) will double the stability by halving the time between the fractional spur suppression integrator cycles.

Figure 3. PE3291 PLL 1 Lock Time

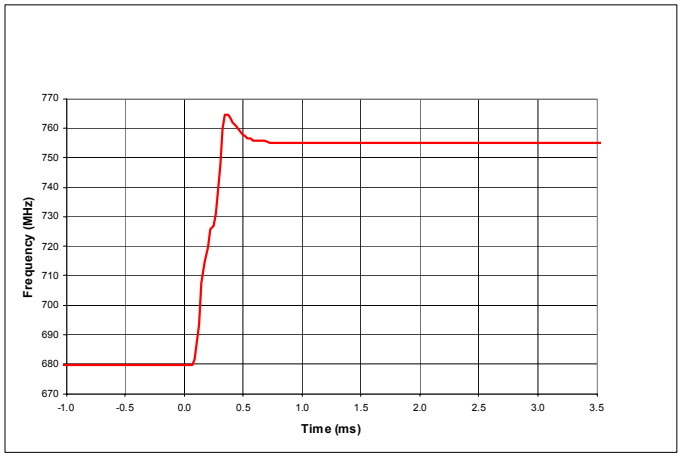
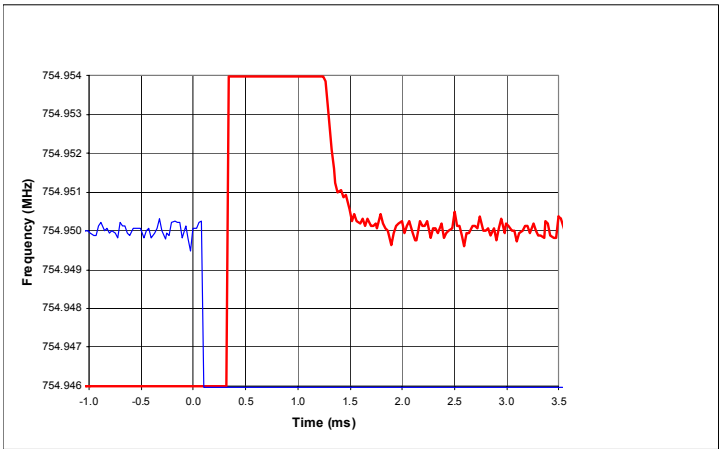


Figure 4. PE3291 PLL 1 Lock Time



VCO considerations

The PE3291 is a three-volt device. The VCO control voltage from the PLL is 0.5 to 2.5 volts. Five–volt VCOs may be used, however the upper limit of the tuning range will be less than specified for the VCO. Wide tune range VCOs may be used by employing an active loop filter to give the needed tuning voltage swings. In general, the narrowest practical tuning range to meet the output frequency requirements of the system should be used. The resulting lower VCO gain (KVCO) will result in lower conversion of charge pump spurious current output to spurious frequency output from the VCO. The lower tuning range VCO will also generally have a higher operating Q factor and contribute less phase noise to the frequency synthesizer output.

Minimizing power consumption

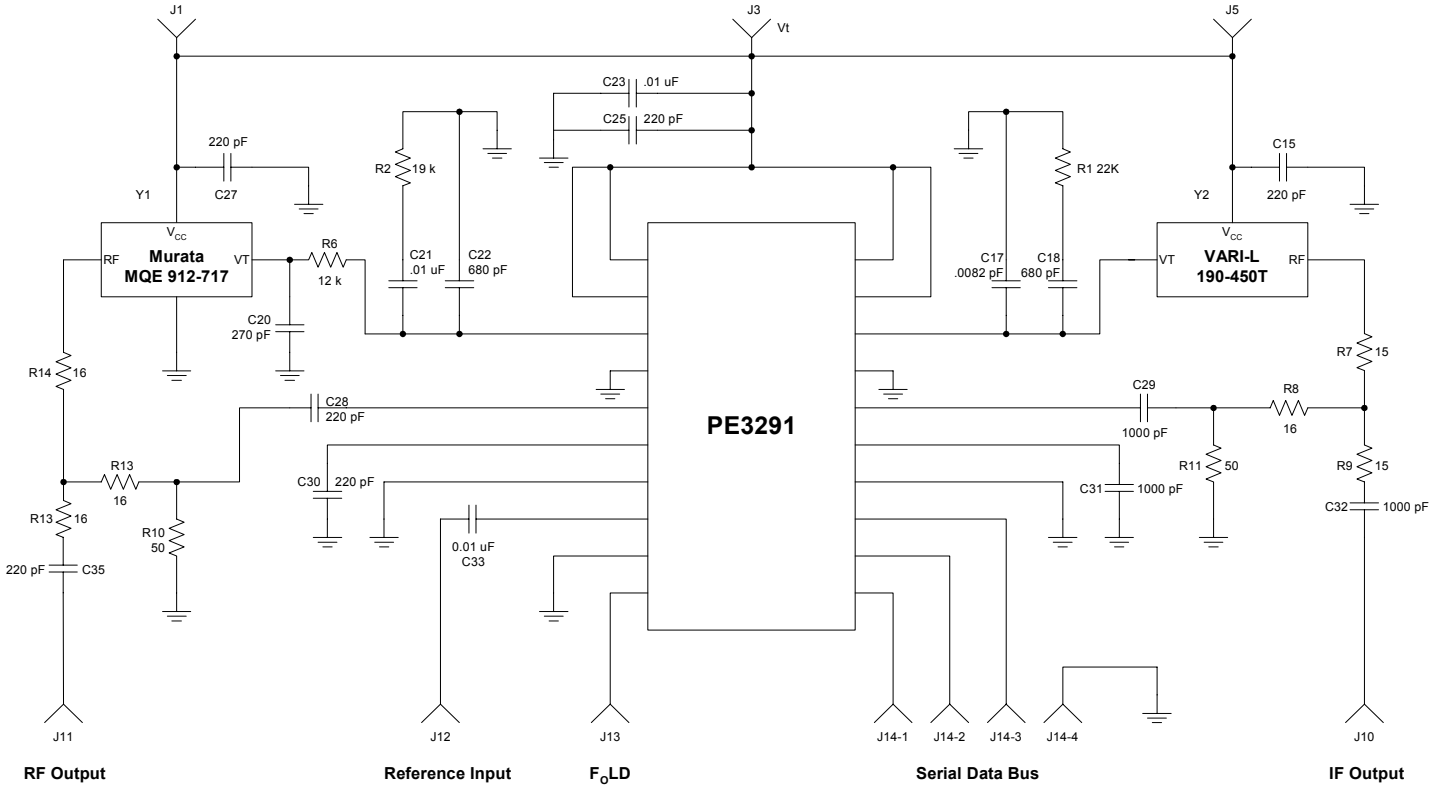
Programmable biasing and external access to the prescaler power supply points have been incorporated into the PE3291 for flexibility in reducing the total power consumption of the device while meeting the requirements of the system. When working from a single 3-volt supply, the current consumption can be reduced if the RF frequency is below 700 MHz or the IF frequency is below 300 MHz by using the software commands to set the PLLs to low power. When multiple voltages are available, further power reduction is possible by custom tuning the current usage to the required frequency, and reducing the voltage that supplies the prescaler current.

The datasheet example shows a 1000 MHz/300 MHz output using 9.9 mW (PLL1 high power, PLL2 low power). If the frequency requirement is reduced to 700 MHz/300 MHz the device will use 7.5 mW from a single 3.0-volt supply (low power/low power). Using a 3.0-volt and 1.8-volt split supply gives 900 MHz/550 MHz on 7.9 mW. A 3.0-volt/1.0-volt supply allows 450 MHz/300 MHz operation on 3.9 mW.

Programming the PE3291

The PE3291 is programmed via a 3-wire serial bus using three-volt CMOS logic levels. Five-volt microprocessors can be used as the program source if an appropriate resistive voltage divider is used as a level shifter. The Data, Clock and Enable pins are CMOS inputs. Peregrine recommends that a pull down resistor be used on these high impedance inputs if the driving microprocessor cannot provide a continuous pull down on the programming lines. The Enable line is particularly critical, as any glitches on this line will reload a data buffer.

Figure 5. Schematic Diagram



The example circuit of Figure 5 has the following specifications and performance:

- Y1 = Murata MQE912-717
- KVCO = 42.5 MHz/V
- Output Frequency = 720 MHz
- Comparison Frequency = 400 kHz
- Channel Spacing = 25 kHz (fractional ratio = 16)
- Loop Filter:
  - 4.5 kHz Loop natural frequency
  - Third-order loop filter
  - 2 dB third-order section
  - 55 degrees phase margin
- Phase Noise = -78 dBc/Hz at 1 kHz offset (Figure 1)
- Fractional Spur = -69 dBc at 25 kHz offset (Figure 2)
- Lock Time = less than 1.5 ms to within 1 kHz (Figures 3 and 4)

Sales Offices

United States

Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Japan

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches
Tel 33-1-47-41-91-73
Fax 33-1-47-41-91-73

Australia

Peregrine Semiconductor Australia
8 Herb Elliot Ave.
Homebush, NSW 2140
Australia
Tel: 011-61-2-9763-4111
Fax: 011-61-2-9746-1501

For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Application Note Identification

No patent rights or licenses to any circuits described in this application note are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Peregrine products are protected under one or more of the following U.S. patents: 6,090,648; 6,057,555; 5,973,382; 5,973,363; 5,930,638; 5,920,233; 5,895,957; 5,883,396; 5,864,162; 5,863,823; 5,861,336; 5,663,570; 5,610,790; 5,600,169; 5,596,205; 5,572,040; 5,492,857; 5,416,043. Other patents may be pending or applied for.