PEREGRINE SEMICONDUCTOR

AN5: Application Note

Using the PE329x Series Fractional-N PLL s

Features

- Industry-leading fractional spur compensation: no adjusting required, stable over temperature
- Ultra-Low Power via FlexiPower variable supply voltages
- Modulo-32 fractional-N main counters

Loop Filter

Second and Third-Order Loops

Choosing the optimum loop filter for a design encompasses many tradeoffs. A general rule of thumb for choosing the loop filter bandwidth is 10 percent of the step size. A second-order loop (C_3 R_3 C_6 and R_6 omitted from Figure 1) will provide the least number of components and the fastest lock times. Widening the loop filter will improve lock time, although stability will suffer and lock time will actually degrade if it is made too wide. If lock time is not an important parameter, a narrower second-order filter will minimize residual FM without requiring additional components.

Third-order loop filters (as shown in Figure 1) provide a good compromise between lock time and residual FM. Using a third-order loop with 20 dB of rejection at the step size will halve the Residual FM as compared to a similar second-order loop, with minimum effect on lock time.

Maximum Loop Filter Bandwidth

The PE329x series PLLs contain capacitors to ground, internal to the charge pump circuitry. PLL1 contains a 50 pF capacitor and PLL2 contains a 100 pF capacitor. These capacitors are relatively transparent for narrow-band loop filters. As the loop bandwidth increases, however, the internal capacitor becomes dominant and limits loop bandwidth. For most applications this is not a concern. For example, a PLL1 application that uses a step size of 80 kHz can operate with an 8 kHz loop bandwidth.

Digital Control Lines

Control Line Noise

Frequency jitter can occur during programming if a low impedance (such as a capacitor to ground) is placed on any control line pin (clock, data, and load enable). The use of a 51k ohm resistor in series with the control line will eliminate the problem with no effect on programming time.

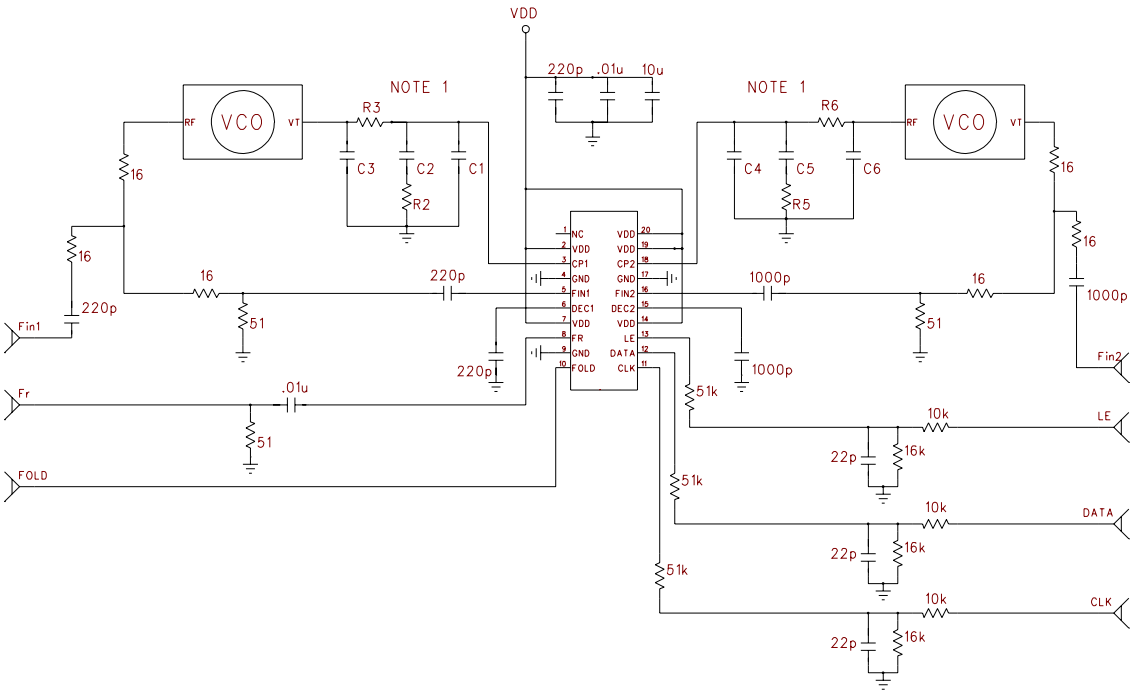
Enable Line Voltage

The PE329x series PLLs use a level-sensitive load enable. The digital controller must therefore provide an active low to the part at all times except when the data is to be loaded into the shift register. If the PLL controller does not hold the voltage low, a high value resistor to ground should be added to the enable line to ensure stable operation.

5 Volt Operation:

The PE329x series PLLs are not capable of accepting control voltages greater than 3.6 volts. Interfacing with 5 volt controllers requires the addition of resistive dividers to comply with the 3.6 volt maximum operating voltage.

Figure 1.



Note 1: For optimum fractional spur and lock-time performance C_2 and C_5 should be polyester (or poly propylene). In addition, the loop filter components must be free from contamination. Contamination will result in poor spur performance.

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Application Note Identification

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