Introduction

CDMA phone manufacturers are in continual battle to maximize radio performance while minimizing power consumption. The Phase Locked Loop portion of a radio's synthesizer plays a critical role in optimizing the phase noise, lock time, spurs, and power consumption requirements.

CDMA customers need to achieve lock times as fast as 2ms in order to meet the new IS95B specifications. Due to the built-in spur compensation mechanism, the Peregrine fractional-N architecture achieves this lock time while providing superior phase noise and spurious performance. This performance is achieved at the lowest power consumption available for a dual 1 GHz PLL, making the Peregrine device an excellent solution for CDMA handsets.

PE3291 Fractional-N PLL - Minimizing Phase Noise, Spurs, Lock Time and Idd for CDMA Applications

Features

- Ultra-Low Power via FlexiPower variable supply voltages
- Modulo-32 fractional-N main counters
- On-board fractional spur compensation: no tuning required, stable over temp.
- Improved phase noise compared to integer-N architectures

Comparison

In order to best illustrate our performance advantage, we have evaluated the most widely used PLL (National's LMX2332L) and compared it with our PE3291. The summary performance is provided in Table 1.

Two comparison boards were built identically using the same VCOs and reference oscillators. The only difference was a second-order loop filter was used with the PE3291, and a third-order loop filter was used with the LMX2332L. The third-order loop filter was needed to improve spurs phase noise and lock time. Measurements were made over temperature and are summarized in Table 1.

Table 1. Summary Performance

	Unit	Condition	Peregrine PE3291*	National LMX2332L**
Power Consumption	mW	3VDC	6.3	10
Phase Noise	dBc / Hz	100 Hz Offset 1 kHz Offset 10 kHz Offset	-68 -75 -100	-66 -65 -96
Lock Time	ms	< +/- 1 kHz	1.8	2.2
Spur Performance 30 kHz Offset	dBc	25° C 85° C	< -91 -89	-83 -64

* PE3291 on-board spur compensation eliminates need for third-order loop filter

** LMX2332 requires a third-order loop filter to meet -70 dBc spur requirement
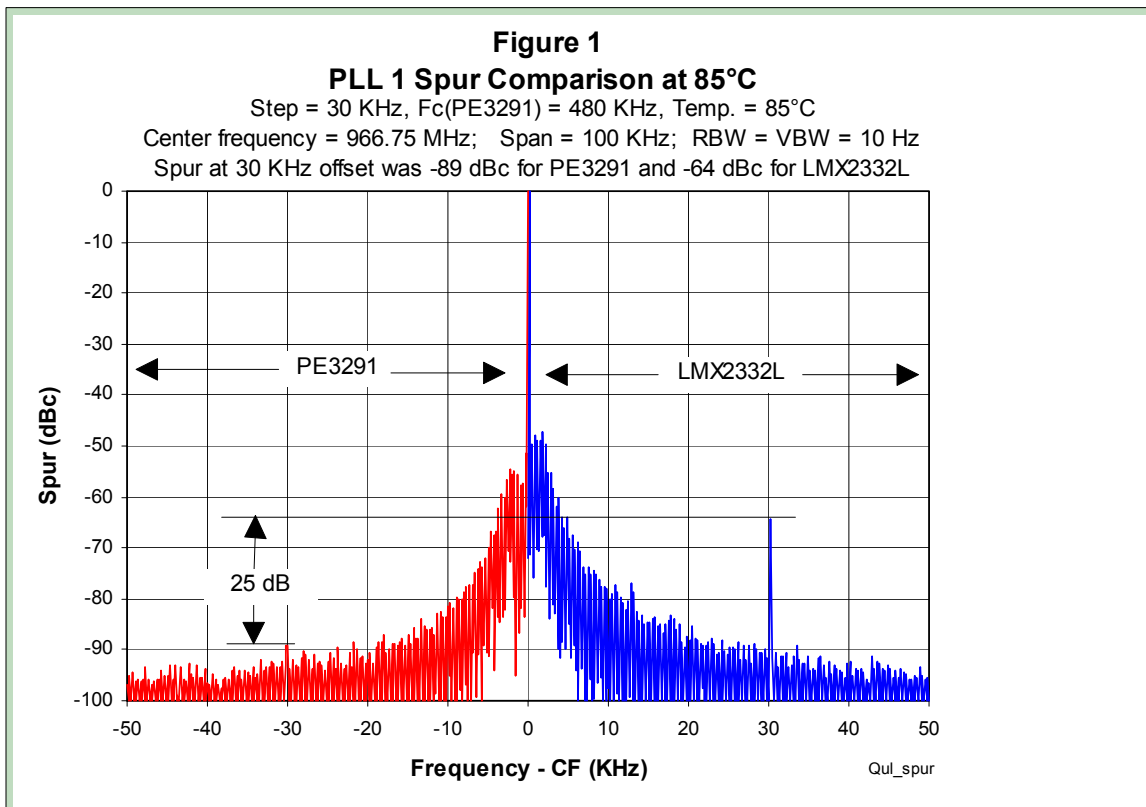
Spur Performance

The Peregrine Semiconductor PE3291 has a patented internal spur compensation network that almost eliminates fractional spurs. This network allows for a wider loop filter for improved lock time, thus eliminating the compromise between lock time and spur performance seen with other PLLs.

A direct comparison (second-order loop with a second-order loop) would show a 30 dB difference between spurs at a 30 kHz offset, +25 degrees C.

When a third-order loop filter is used to improve the LMX2332L spur performance, the PE3291 still provides 8 dB lower spur level at room temperature (Table 1).

High temperature performance is more dramatic. The PE3291 spur suppression degrades by only 2 dB at +85C. Even with the loop order difference, the Peregrine PE3291 provides 25 dB lower spur levels at +85 degrees C, as shown in Figure 1.

Figure 1
PLL 1 Spur Comparison at 85°C
Step = 30 KHz, Fc(PE3291) = 480 KHz, Temp. = 85°C
Center frequency = 966.75 MHz;   Span = 100 KHz;   RBW = VBW = 10 Hz
Spur at 30 KHz offset was -89 dBc for PE3291 and -64 dBc for LMX2332L

Power Consumption

The PE3291 sets a new standard in power consumption. The PE3291 requires a mere 1.4 mA (nominal) at 800MHz, approximately 50% that of the LMX2332L. Peregrine's UTSi CMOS technology allows significant power savings over BiCMOS technology for comparable speeds. The resultant power consumption of the dual PE3291 running at 800 MHz & 50 MHz is 6.3 mW at 3V.
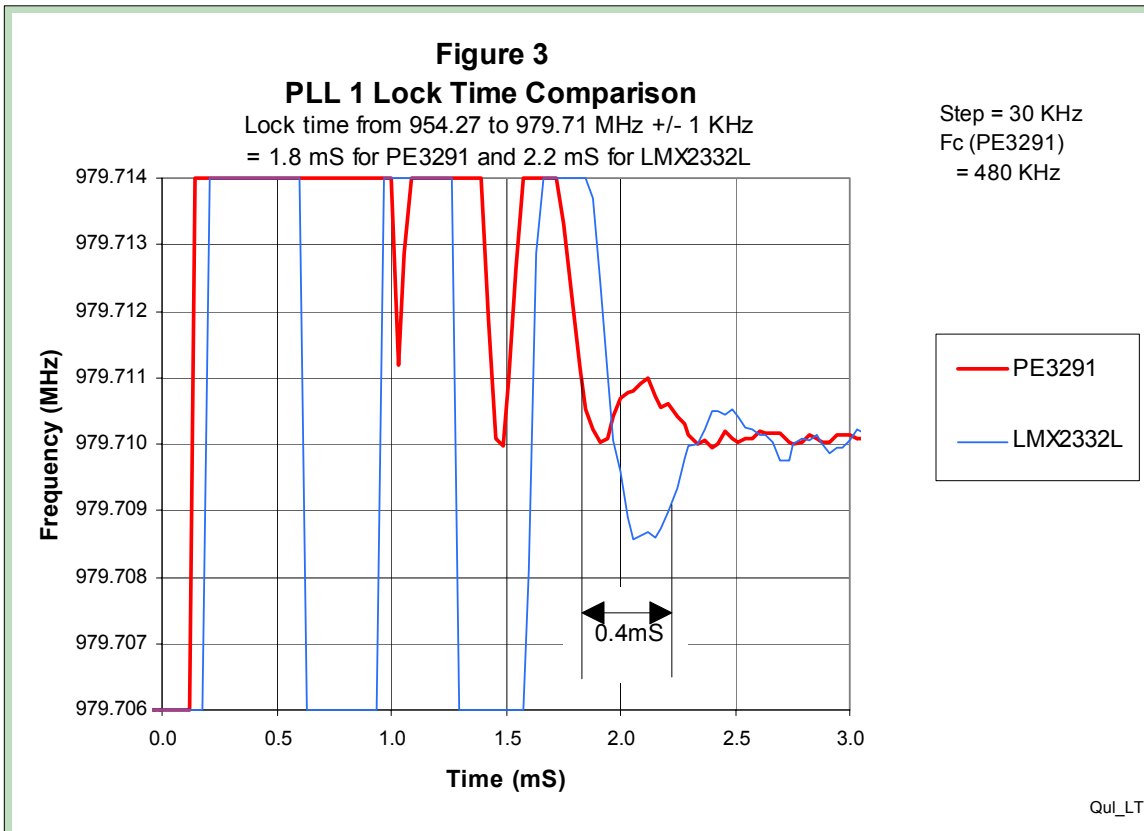
Phase Noise

The PE3291 provides unsurpassed phase noise performance. The use of fractionality allows a higher comparison frequency than integer-N parts. This benefit is easily seen in the comparison plot of phase noise (Figure 2 below). A 5 dB improvement is seen consistently throughout the pass band of the loop.

Figure 2
Phase Noise Comparison
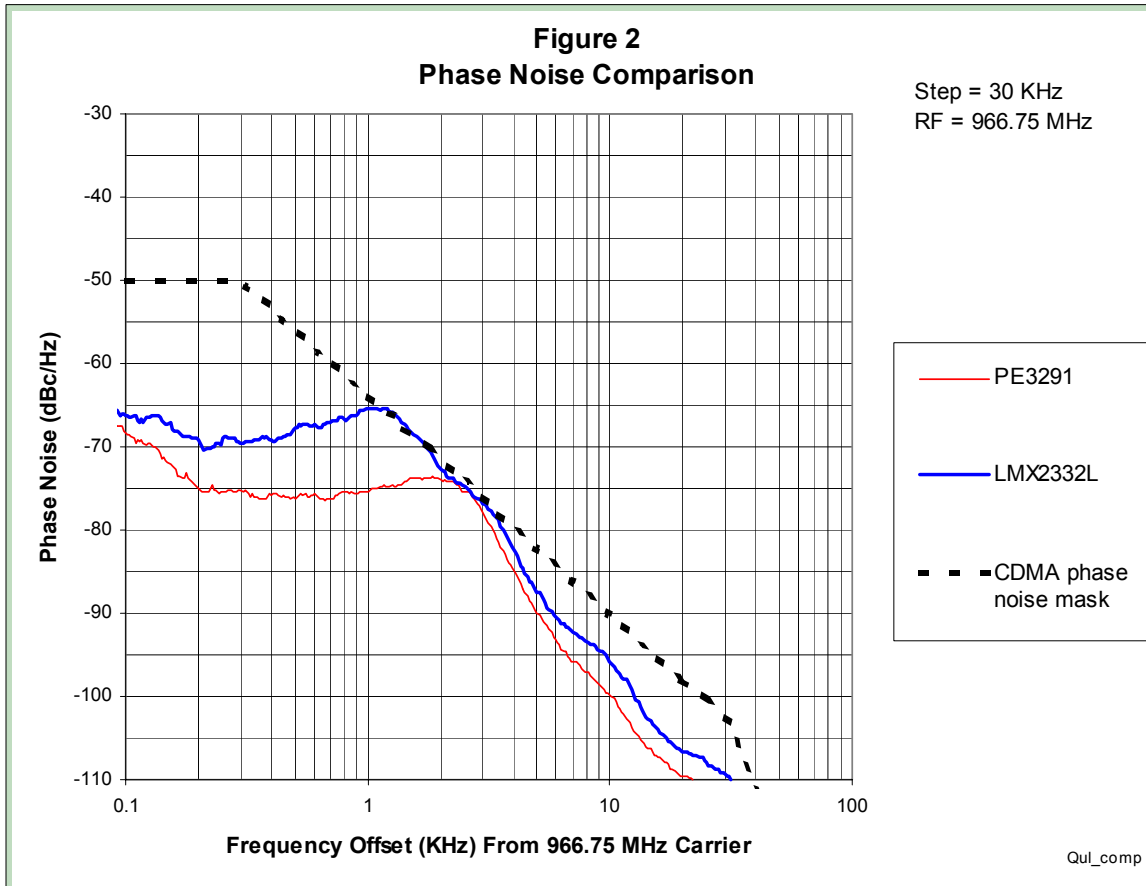
Lock Time

The wider loop bandwidth allowed by the PE3291's clean phase detector output allows for a 14 percent faster lock time, meeting the EIA95 CDMA 2ms lock time requirement. Figure 3 shows the lock time comparison.

Figure 3
PLL 1 Lock Time Comparison
Lock time from 954.27 to 979.71 MHz +/- 1 KHz
= 1.8 mS for PE3291 and 2.2 mS for LMX2332L

Step = 30 KHz
Fc (PE3291)
= 480 KHz

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Ease of Use

IS95B grade of performance is easily achieved with the PE3291. The on-chip fractional spur compensation allows for fast lock times. All this is achieved with a reduced parts count and a 33 percent reduction of power over the LMX2332L.

A schematic and parts list are provided in Figure 4 to aid in characterizing the part. Demo boards are available through your rep, or call direct (858) 455-0660 and ask for a free sample device.

Figure 4. Schematics and Parts List

PE3291
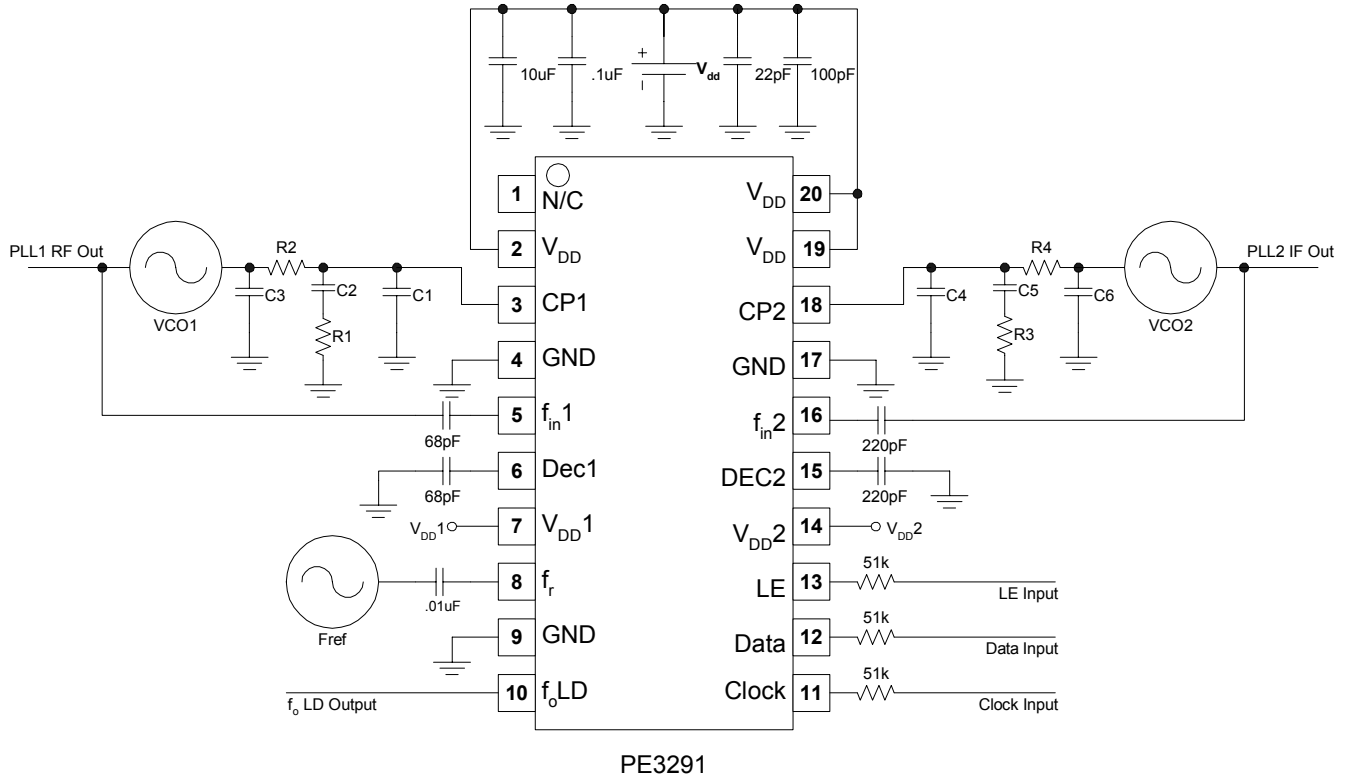
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Application Note Identification

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