PEREGRINE SEMICONDUCTOR

AN7: Application Note

Using the PE3293 Fractional-N PLL in Single-Band 1800 and Dual-Band CDMA Solutions

Features

- Industry-leading fractional spur compensation: no adjustment required, temperature stable
- Ultra-Low Power consumption: 4.0 mA typical, both loops operating
- Modulo-32 fractional-N main counters
- Supply voltage range 2.7 to 3.3 VDC

Introduction

The PE3293 is well suited for CDMA at PCS bands. The part was designed for low power consumption while maintaining excellent phase noise and spur performance. The PE3293 is easy to use and requires minimal external circuitry, as seen in Figure 1. Another advantage to the PE3293 is its high impedance VCO input pin that eliminates the need to use a power divider between the VCO, PLL, and RF circuitry.

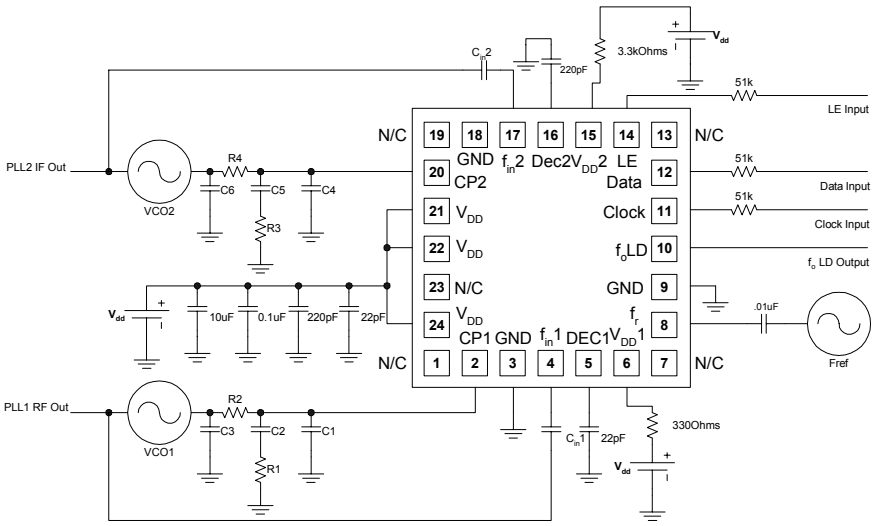
Second- and Third-order Loop Filter Design

Peregrine's patented internal fractional spur compensation works exceptionally well with single-band VCOs, requiring only a second-order loop filter. This configuratiion will provide spur rejection greater than -75 dBc and provide optimum phase noise.

Dual-band VCOs tend to have slightly lower spur performance, and the optimum design usually uses a third-order loop. This configuration will also provide -75 dBc spur performance with minimal effect to in-band phase noise.

Loop filter design for both second- and third-order loop filters is made easy with the use of an application available on our website at www.peregrine-semi.com (click on the Loop Filter Calc Button under the PE3293 product page).

Figure 1. PE3293 Schematic Drawing (BCC Package)



Note 1: For optimum fractional spur and lock-time performance C2 and C5 should be polyester (or poly propylene). In addition, the loop filter components must be free from contamination. Contamination will result in poor spur performance.

Note 2: Pins 1, 7, 13, 19 and 23 are no-connect pins. These may be connected to either V_{DD} or Ground.

Note 3: For best performance, place Cin1 as close to pin as possible and utilize proper transmission line layout techniques for RF runner from VCO output.

Table 1. Summary Performance

Loop Filter Order	2nd	3rd
VCO Frequency (MHz)	Single Band 1750	Dual Band 967 / 1750
Kvco (MHz / V)	27.9	40
LPF BW (kHz)	1	2.4
Application Step Size (kHz)	50	30 or 50
Design step (kHz)	10	10
Fc (kHz)	160	320
RF (MHz)	1750	1750
Loop Filter Values		
C1	1.5 nF	1.5 nF
C2	10 nF	22 nF
R1	43 k	15 k
C3	N/A	1.5 nF
R2	0	510
Loop BW (kHz)	1	1.1
Spur at step (dBc)	-79	-75
Phase Noise (dBc / Hz)		
@ 1 kHz offset	-60.2	-63.3
@ 10 kHz offset	-90.2	-92
@ 20 kHz offset	-100.7	-102.5
@ 50 kHz offset	-110.7	-110
@ 100 kHz offset	-116.3	-117
Peak Phase Noise	-60.2 dBm @ 1 kHz	-63 dBc @ 1.1 kHz
Current Consumption (mA) Both loops operating	3.1	3.1
Lock time to settle to within 1 kHz	2.3 mS for 100 kHz step and 4.2 ms for 60 MHz step	4.2 ms for 60 MHz shift @ 1800

Summary of Results

Phase noise, lock time, and spur performance are easily achieved using the schematic provided in Figure 1 with the appropriate loop filter. The example in Table 1 shows phase noise at 1 kHz offset less than 60 dBc / Hz and spur performance less than -70 dBc. Lock times for a 100 kHzstep are less than 2.3 ms. This performance is provided with a 10 kHz step size using only 3.1 mA at 3 V.

Peregrine Semiconductor invites you to try out a complimentary PE3293.

Demonstration boards are also available.

You can contact us through your local representative or directly at (858) 455-0660.

Sales Offices

United States

Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Japan

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches
Tel 33-1-47-41-91-73
Fax 33-1-47-41-91-73

Australia

Peregrine Semiconductor Australia
8 Herb Elliot Ave.
Homebush, NSW 2140
Australia
Tel: 011-61-2-9763-4111
Fax: 011-61-2-9746-1501

For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Application Note Identification

No patent rights or licenses to any circuits described in this application note are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Peregrine products are protected under one or more of the following U.S. patents: 6,090,648; 6,057,555; 5,973,382; 5,973,363; 5,930,638; 5,920,233; 5,895,957; 5,883,396; 5,864,162; 5,863,823; 5,861,336; 5,663,570; 5,610,790; 5,600,169; 5,596,205; 5,572,040; 5,492,857; 5,416,043. Other patents may be pending or applied for.