OC-12 622.08 MHz Reference Clock Design

Features

- Presents several easy-to-replicate design examples
- Extremely low phase noise
- Super low RMS jitter (0.12 ps in a frequency offset range of 10 kHz to 80 MHz)
- No interface or microprocessor – self starting

Summary

Peregrine Semiconductor Application Note AN16 demonstrates an extremely low-jitter, high frequency reference clock design by combining a high performance integer-N PLL with a low noise VCO/VCXO. This report shows specific design examples using the Peregrine PE3341 or PE3335 PLLs. The PE3341, with on-chip EEPROM, or the PE3335, with direct load interface, will self-start at a fixed frequency chosen by the user - ideal for reference clock applications. This note describes 622.08 MHz reference clock with integrated RMS jitter as low as 0.12 ps for a frequency offset from 10 kHz to 80 MHz.

1. Introduction

A typical clock supporting OC-12 applications running at 622.08-MHz requires low jitter and can also be used as a clean reference source for OC-192 and higher rates. Peregrine Semiconductor AN16, *Using Peregrine Phase-Locked Loop (PLL) Integrated Circuits in Reference and System Clock Applications*, provides the essential PLL theory and basic design trade-offs for these applications.
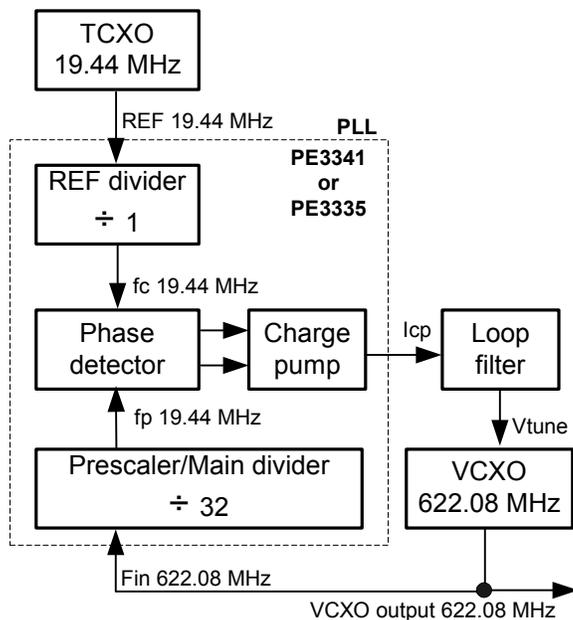
Figure 1. OC-12 Reference Clock Design.

As shown in Figure 1, the excellent stability of a low frequency crystal source at 19.44 MHz can be extended to the OC-12 clock frequency at 622.08 MHz by using a high performance PLL. This report presents several practical examples and compares the results.

2. Design Consideration and Setup

An RMS jitter specification with a frequency offset in the range of 10 kHz to 80 MHz is a standard metric for many reference clocks and is used for the results reported in this application note. The PLL loop bandwidth was also set for best jitter performance within this same frequency offset range.

A typical PLL has an integrated phase detector with either a charge pump (CP) or logic level (UP/DOWN) output. Reference clock applications usually favor a CP output version for two important reasons. First, the CP can drive a simple low cost, passive resistor-capacitor loop filter. Second, most Voltage Controlled Oscillators (VCOs) with the lowest phase noise performance have a narrow tuning range that is well suited to a CP with a 3-volt supply rail.

Another unique feature of Peregrine's PLLs, the EEPROM feature of the PE3341 or the direct

interface mode of the PE3335, enables the PLL to self-start without the need of a control interface or supporting microprocessor. Both have a charge pump (CP) phase detector output, are available in very small MLPQ packages, and provide other features ideal for both reference clocks and clock modules.

The reason specific parameters were selected (a reference frequency 19.44 MHz, REF divider of 1 and Prescaler/Main divider of 32 as shown in Fig. 1) is now described in detail.

Since any frequency multiplication/division increases system noise, the reference (REF) divider and the Prescaler/Main divider values, shown in Fig. 1, should be kept as small as possible. The REF divider of a Peregrine Integer-N PLL can divide from 1 to 64. Thus the minimum value of 1 is selected as the reference divider ratio. This will set the comparison frequency, F_c, to the same frequency, F_r, of the reference TCXO. Next, the Prescaler/Main divider number, N, and the reference TCXO frequency, F_r, must be selected. There are three restrictions in choosing N and F_r:

> 1). N must fall within the allowable range of the on-chip M and A counters. The available low-value N numbers are 20, 21, 22, 30, 31, 32, 33, 40, 41, 42, 43, 44, etc., and are continuous for $N \geq 90$ to N_{max} (5135 for PE3341 and PE3335).
> 2). $Fout = N \bullet F_c = N \bullet F_r$ = 622.08 MHz.
> 3). The maximum F_c frequency is 20 MHz although the external reference may go as high as 100 MHz.

The smallest N that satisfies all three restrictions is 32, resulting in a REF frequency of 19.44 MHz. A 19.44-MHz TCXO is readily available and often used in many telecom applications.

Many TCXOs were tested for this application. The optimum choice is a compromise of size, price, and performance. Of the TCXOs tested, the Vectron International OSC Series Ultra Miniature TCXO was chosen as the preferred device due to its low profile, low cost, 3 or 5 VDC supply operation, and many stability and trim options. The particular model used for the design examples presented is

the OSC-3B0-19.44 MHz. Phase noise of this model appears in the appendix.

The 622.08 MHz oscillator phase noise is a very important parameter in this application. Most of the 10 kHz to 80 MHz offset bandwidth naturally falls outside the PLL loop bandwidth (LBW). With the selection of a narrow LBW, the integrated noise is approximately the output oscillator noise floor alone. Several narrowband 622.08 MHz VCOs were evaluated: the RF Monolithics, Inc. VCSC OP4005B, the Vectron International VCSO VS-500A, and the MyFrequency, Inc. VCXO M7302-50V.

The OP4005B and VS-500A phase noise plots are shown in Figure 2, courtesy of RF Monolithics. The MFI M7302-50V was not included in Fig. 2 because the data was not available at time of publication for this new product. The operating voltage for all units was 3.3 Volts. The OP4005B and VS-500A have an additional complimentary output that was terminated with a 51-ohm load. As shown in Figure 3, a passive 3-way divider splits the VCXO output. One output supplies the test equipment while the other completes the PLL path through an additional 2 dB pad. AC coupling removes any DC bias concerns. The appendix contains additional details.
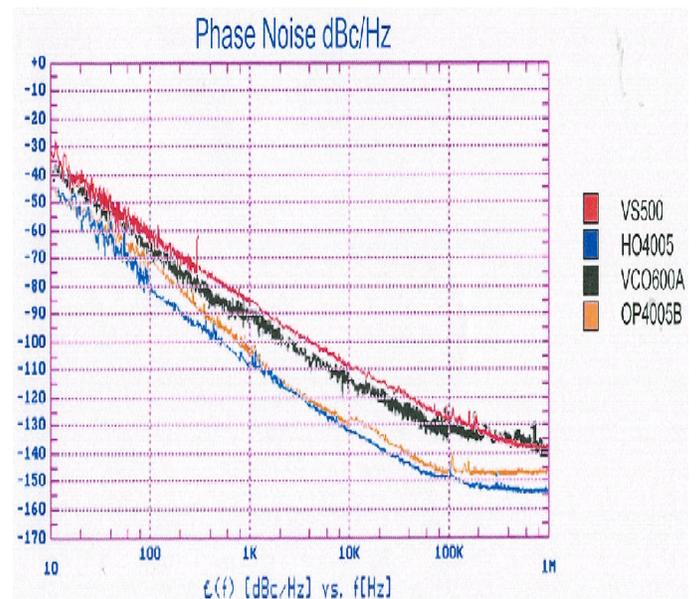
Figure 2. Noise floor of several VCXOs. (Courtesy of RF Monolithics, Inc.)
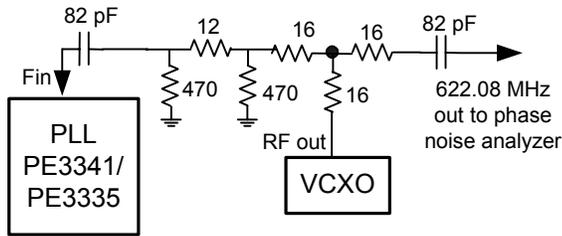
Figure 3. RF signal path.

The loop filter is a passive second order filter as shown in Figure 4. The LBWs used in the phase noise tests were 300 and 500 Hz with the component values given in Table 1.
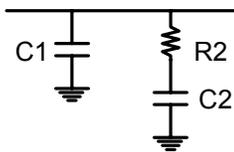
Figure 4. Passive second order loop filter.

Table 1. Loop filters components for Kvco = 120 kHz/V, Icp = 2 mA, N = 32 and phase margin = 67 degs.

LPF BW (Hz)	300	500
C1	0.39 uF	0.15 uF
C2	10 uF	3.47 uF
R2 (Ohm)	270	470

The phase noise from 10 Hz to its 1 MHz offset limit was measured with a RDL NTS-1000B Phase Noise Analyzer. An Agilent E4440A PSA Series Spectrum Analyzer performed the phase noise measurement from 1 MHz to 100 MHz, corrected to align the 1 MHz crossover.

3.   Effect of Loop Filter Bandwidth

Figure 5 shows the PE3341 closed loop phase noise with the RFM OP4005B at a LBW of 300 Hz and 500 Hz (Note: the frequency unit in the graph is kHz). The phase noise beyond a 2 kHz offset is essentially the same for both LBWs. This shows, as expected, that the VCO alone sets the phase noise well outside the LBW, i.e. > 2 kHz offset. A 500 Hz LBW removes virtually all PLL generated jitter for an RMS jitter measurement from 10 kHz to 80 MHz. For added margin, all subsequent reference clock designs and comparisons use a 300 Hz LBW.
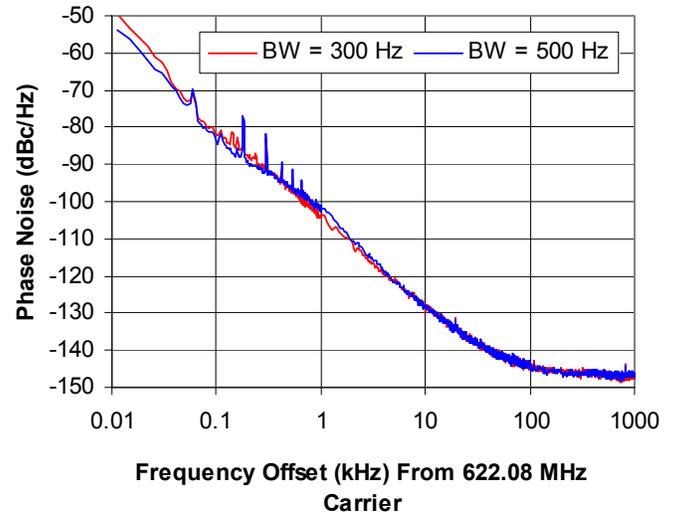
Figure 5. Phase noise of PE3341/RFM OP4005B OC-12 reference clocks with 300 and 500 Hz LBW

4.   Phase Noise of OC-12 Reference Clocks.

Four OC-12 reference clocks were fabricated using the PE3341 or PE3335 PLLs with the RFM OP400B, Vectron VS-500A or MFI M7302-50V VCOs. The PLL/VCO combinations used were; PE3341/OP400B, PE3335/OP400B, PE3335/VS-500A and PE3341/M7302. Figure 6 displays the phase noise performance of these four examples.
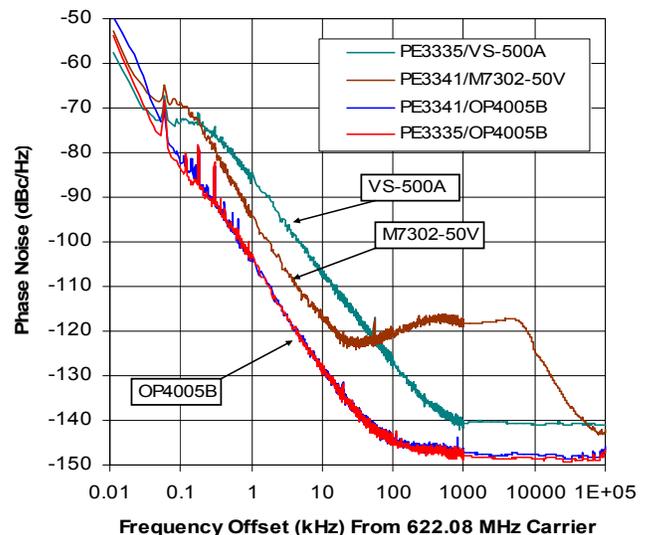
Figure 6.   Phase noise of OC-12 reference clocks: PE3341/OP400B, PE3335/OP400B, PE3335/VS-500A and PE3341/M7302.

As shown in Fig. 6, the PE3341/OP4005B and PE3335/OP4005B combinations perform best at all offsets. The excellent performance with either the PE3341 or PE3335 PLLs shows that both are well paired with the OP4005B. The clock design using the VS-500A performs better than the M7302-50V version at frequency offsets from 0.2 to about 55 kHz, but is worse for the remainder of frequency offsets. The closed loop phase noise of each PLL/VCO combination agrees well with the corresponding open loop VCO noise floors in Fig. 2. The correlation confirms that the PLL does not add undesired noise or spurious.

5. RMS Jitter from 10 kHz to 80 MHz

Table 2 gives the equivalent RMS jitter by integrating the Fig. 6 phase noise data over the 10 kHz to 80 MHz offset range. The RMS jitter for the RFM OP4005B with the PE3335 or PE3341 is 0.13 ps or less. The RMS jitter for the PE3335/VS-500A and the PE3341/M7302-50A units is still outstanding at 0.34 ps and 1.47 ps, respectively.

Table 2. Calculated jitter: 10 kHz to 80 MHz offset.

Reference Clock	RMS noise (Degrees)	RMS Jitter (UI)	RMS Jitter (ps)
PE3335/OP4005B	0.027	0.000074	0.12
PE3341/OP4005B	0.029	0.000081	0.13
PE3335/VS-500A	0.076	0.000210	0.34
PE3341/M7302-50A	0.330	0.000916	1.47

Note: RMS Jitter (UI) = RMS noise (degrees)/360°
RMS Jitter (Time) = RMS Jitter (UI) x Clock Period
Clock Period = 1.608 ns

6. Conclusion

The Peregrine Semiconductor PE3341 or the PE3335, combined with a low noise VCXO and a stable 19.44-MHz TCXO, provide a very low jitter OC-12 reference clock as demonstrated by the four examples in this report. RMS jitter, as low as 0.12 ps for 10 kHz to 80 MHz offsets, is readily achievable. The PE3341 EEPROM feature or the PE3335 direct interface mode allows simple, self-starting operation with no interface or support microprocessor needed – an especially attractive feature for standalone or module applications. Both PLLs are available in small leadless MLP packages; 7x7 mm for the PE3335 or 4x4 mm for the PE3341.

7. Acknowledgement

Many thanks to the following companies for providing their respective oscillators featured in this report:

RF Monolithics, Inc. (www.rfm.com)
Vectron International (www.vectron.com)
MyFrequency, Inc. (www.myfrequencyxtal.com)

8. Appendix

8.1. Phase Noise of Vectron OSC Series TCXOs

Data sheet phase noise at 10 MHz:

-80 dBc/Hz max. at 10 Hz offset
-125 dBc/Hz max. at 100 Hz offset
-145 dBc/Hz max. at 1 kHz offset
-148 dBc/Hz max. at 10 kHz offset
-150 dBc/Hz max. at 100 kHz offset

8.2. RFM VCSC OP4005B Connection
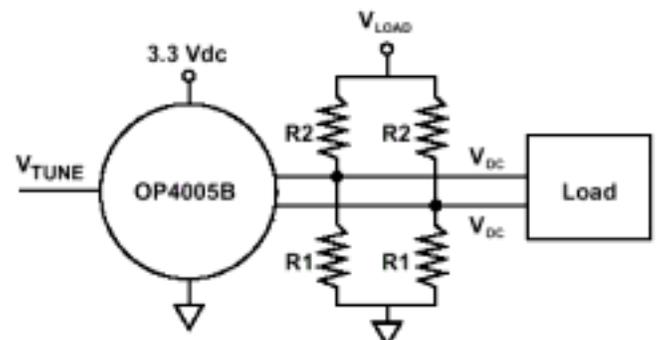
With AC coupling, R1, R2, and VLoad are not necessary. Only one of the complementary outputs was used in this test, the unused output was terminated with a blocking cap and a 51-ohm load.

8.3. Vectron VCSO VS-500A Connection

File No. 72/0030~00A │ **UTSi ® CMOS RFIC SOLUTIONS**
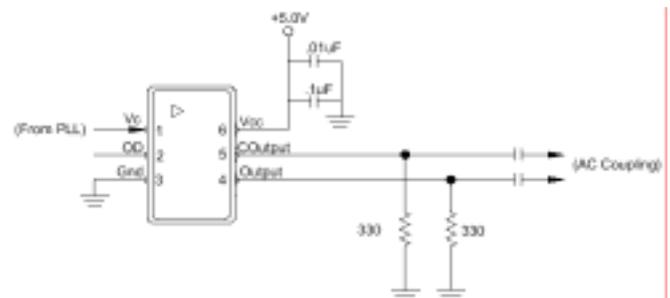
Note: To disable the output, ground the Output Disable, pin 2. To enable the output, leave pin 2 floating (open). Only one of the complementary outputs was used in this test. The unused output was terminated with a blocking cap and a 51-ohm load.

8.4. MyFrequency VCXO M7302-50V Connection
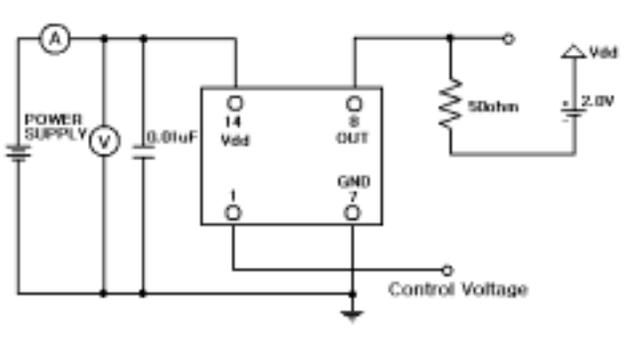
8.5. PE3341 Pin Connection for MLP 4x4 mm package

A partial schematic of the PE3341 in a leadless MLP package is shown below.
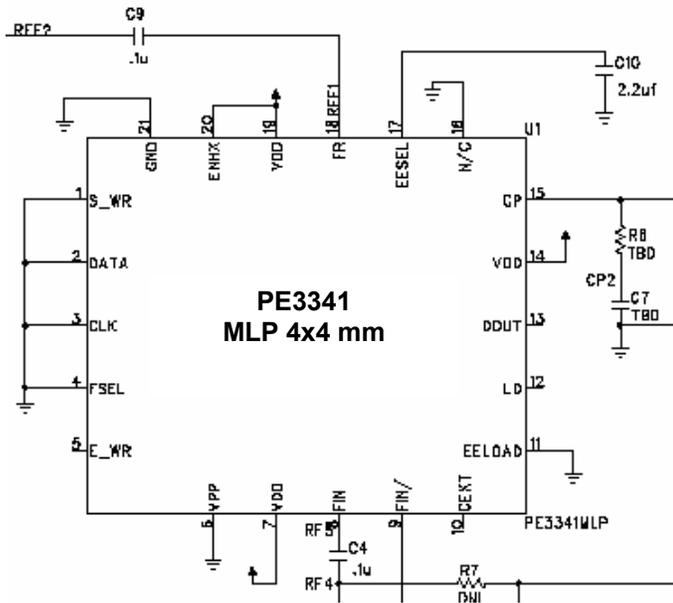
Connect ground and Vdd as shown.

Pins 5, 10, 12 and 13 floating (open).-Pin 15 charge pump output to the loop filter.

Pins 8 and 9 are Fin(+) and Fin(-), respectively.

AC couple (100 pF) the VCO output with a coupler, splitter, or attenuator as necessary. With a single-ended VCO the unused Fin pin should be

terminated with a blocking cap and a 51-ohm termination.

8.6. PE3341 Pin Connection for 20-lead TSSOP package

The TSSOP package pinout appears below.
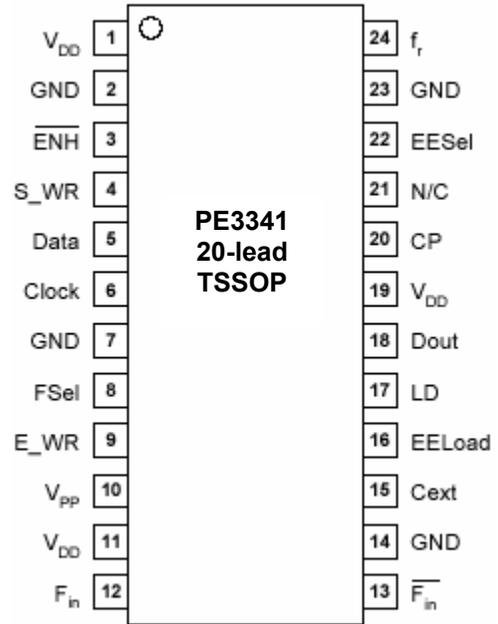
Pins 1, 3, 11 and 19 connect to Vdd (3V).

Pins 2, 4 - 8, 10, 14, 16, 21, and 23 are ground.

Pins 9, 15, 17 and 18 are floating (open).

Pin 22, connect a large cap, 2.2 uF, to ground.

Pin 24 is AC coupled (39 nF) to reference input.

Pin 20, charge pump output to the loop filter.

Pins 12 and 13 are Fin(+) and Fin(-), respectively

AC couple (100 pF) the VCO output with a coupler, splitter, or attenuator as necessary. With a single-ended VCO the unused Fin pin should be terminated with a blocking cap and a 51-ohm termination.

8.7. PE3335 Pin Connections for MLP package

PE3335
48-lead
MLPQ
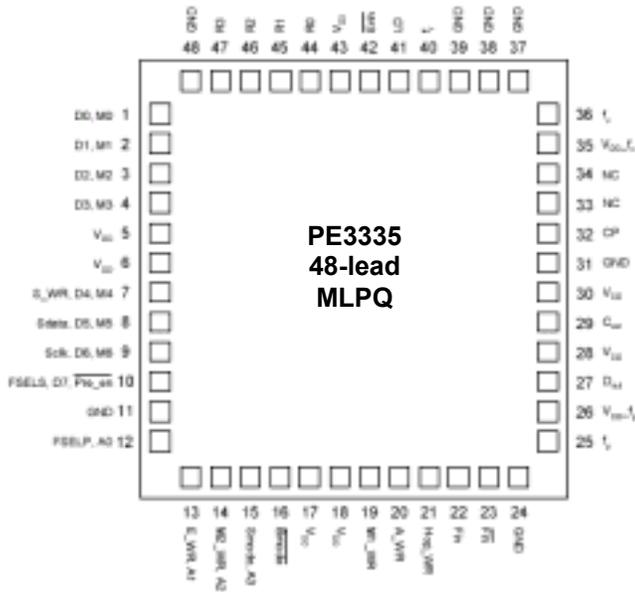
Pins 1, 3, 4, 7, 8, 9, 10, 11, 12, 14, 15, 19, 20, 21, 24, 26, 31, 33, 34, 35, 37, 38, 39, 44, 45, 46, 47 and 48 are ground.

Pins 2, 5, 6, 13, 16, 17, 18, 28, 30, 42 and 43 are connected to Vdd (3 V).

Pins 25, 27, 29, 36 and 41 float (open).

Pin 40 is AC coupled to the reference input.

Pin 32 charge pump output to the loop filter.

Pins 22 and 23 are Fin(+) and Fin(-), respectively.

AC couple (100 pF) the VCO output with a coupler, splitter, or attenuator as necessary. With a single-ended VCO the unused Fin pin should be terminated with a blocking cap and a 51-ohm termination.

PEREGRINE
SEMICONDUCTOR

Sales Offices

United States

Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Japan

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches
Tel 33-1-47-41-91-73
Fax 33-1-47-41-91-73

Australia

Peregrine Semiconductor Australia
8 Herb Elliot Ave.
Homebush, NSW 2140
Australia
Tel: 011-61-2-9763-4111
Fax: 011-61-2-9746-1501

For a list of representatives in your area, please refer to our Web site at: ***http://www.peregrine-semi.com***

Application Note Identification

No patent rights or licenses to any circuits described in this application note are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Peregrine products are protected under one or more of the following U.S. patents: 6,090,648; 6,057,555; 5,973,382; 5,973,363; 5,930,638; 5,920,233; 5,895,957; 5,883,396; 5,864,162; 5,863,823; 5,861,336; 5,663,570; 5,610,790; 5,600,169; 5,596,205; 5,572,040; 5,492,857; 5,416,043. Other patents may be pending or applied for.