



PE3240

2.2 GHz UltraCMOS™ Integer-N PLL for Low Phase Noise Applications

Product Description

Peregrine's PE3240 is a high performance integer-N PLL capable of frequency synthesis up to 2.2 GHz. The superior phase noise performance of the PE3240 is ideal for applications such as wireless local loop basestations, LMDS systems and other demanding terrestrial systems.

The PE3240 features a 10/11 dual modulus prescaler, counters and a phase comparator as shown in Figure 1. Counter values are programmable through a three wire serial interface.

The PE3240 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- 2.2 GHz operation
- $\div 10/11$ dual modulus prescaler
- Internal phase detector
- Serial programmable
- Low power—15 mA at 3 V
- Ultra-low phase noise
- Available in 20-lead TSSOP

Figure 1. Block Diagram

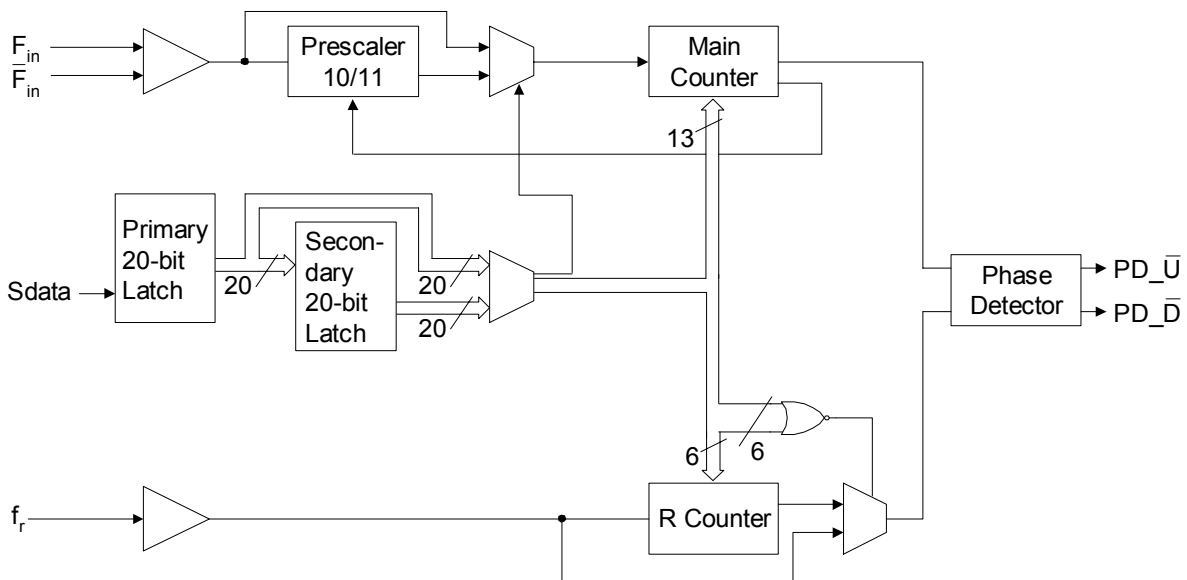
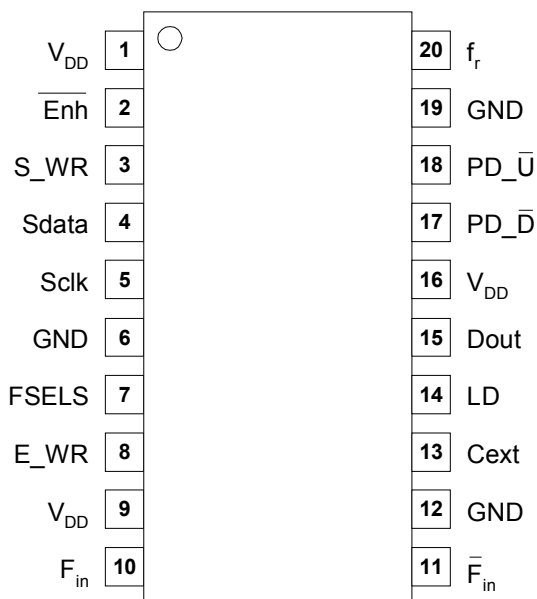


Figure 2. Pin Configuration (Top View)

Figure 3. Package Type

20-lead TSSOP


Table 1. Pin Descriptions

| Pin No. | Pin Name | Type | Description |
|---------|-------------------------|----------|--|
| 1 | V _{DD} | (Note 1) | Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing required. |
| 2 | $\overline{\text{Enh}}$ | Input | Enhancement mode. When asserted low ("0"), enhancement register bits are functional. Internal 70 k Ω pull-up resistor. |
| 3 | S_WR | Input | Serial load enable input. While S_WR is "low", Sdata can be serially clocked. Primary register data are transferred to the secondary register on S_WR rising edge. |
| 4 | Sdata | Input | Binary serial data input. Input data entered MSB first. |
| 5 | Sclk | Input | Serial clock input. Sdata is clocked serially into the 20-bit primary register (E_WR "low") or the 8-bit enhancement register (E_WR "high") on the rising edge of Sclk. |
| 6 | GND | | Ground. |
| 7 | FSELS | Input | Selects contents of primary register (FSELS=1) or secondary register (FSELS=0) for programming of internal counters. Internal 70 k Ω pull-down resistor. |
| 8 | E_WR | Input | Enhancement register write enable. While E_WR is "high", Sdata can be serially clocked into the enhancement register on the rising edge of Sclk. Internal 70 k Ω pull-down resistor. |
| 9 | V _{DD} | (Note 1) | Same as pin 1. |
| 10 | Fin | Input | Prescaler input from the VCO. Max frequency input is 2.2 GHz. |
| 11 | $\overline{\text{Fin}}$ | Input | Prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50 Ω resistor to the ground plane. |
| 12 | GND | | Ground. |
| 13 | Cext | Output | Logical "NAND" of PD_U and PD_D terminated through an on chip, 2 k Ω series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD. |
| 14 | LD | Output | Lock detect is an open drain logical inversion of CEXT. When the loop is in lock, LD is high impedance, otherwise LD is a logic low ("0"). |
| 15 | Dout | Output | Data out function, Dout, enabled in enhancement mode. |
| 16 | V _{DD} | (Note 1) | Same as pin 1. |

Table 1. Pin Descriptions (continued)

| Pin No. | Pin Name | Type | Description |
|---------|----------|--------|---|
| 17 | PD_D | Output | PD_D pulses down when f_p leads f_c . |
| 18 | PD_U | Output | PD_U pulses down when f_c leads f_p . |
| 19 | GND | | Ground. |
| 20 | f_r | Input | Reference frequency input. |

Note 1: V_{DD} pins 1, 9, and 16 are connected by diodes and must be supplied with the same positive voltage level.

Table 2. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|-----------|---------------------------|------|----------------|-------|
| V_{DD} | Supply voltage | -0.3 | 4.0 | V |
| V_I | Voltage on any input | -0.3 | $V_{DD} + 0.3$ | V |
| I_I | DC into any input | -10 | +10 | mA |
| I_O | DC into any output | -10 | +10 | mA |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 3. Operating Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|----------|-------------------------------------|------|------|-------|
| V_{DD} | Supply voltage | 2.85 | 3.15 | V |
| T_A | Operating ambient temperature range | -40 | 85 | °C |

Table 4. ESD Ratings

| Symbol | Parameter/Conditions | Level | Units |
|-----------|---------------------------------------|-------|-------|
| V_{ESD} | ESD voltage human body model (Note 1) | 1000 | V |

Note 1: Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

Table 5. DC Characteristics: $V_{DD} = 3.0\text{ V}$, $-40^\circ\text{ C} < T_A < 85^\circ\text{ C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|--|---|---------------------|-----|---------------------|---------------|
| I_{DD} | Operational supply current; Prescaler enabled | $V_{DD} = 2.85\text{ to }3.15\text{ V}$ | | 15 | 20 | mA |
| Digital Inputs: S_WR, Sdata, Sclk | | | | | | |
| V_{IH} | High level input voltage | $V_{DD} = 2.85\text{ to }3.15\text{ V}$ | $0.7 \times V_{DD}$ | | | V |
| V_{IL} | Low level input voltage | $V_{DD} = 2.85\text{ to }3.15\text{ V}$ | | | $0.3 \times V_{DD}$ | V |
| I_{IH} | High level input current | $V_{IH} = V_{DD} = 3.15\text{ V}$ | | | +1 | μA |
| I_{IL} | Low level input current | $V_{IL} = 0, V_{DD} = 3.15\text{ V}$ | -1 | | | μA |
| Digital inputs: $\overline{\text{Enh}}$ (contains a 70 k Ω pull-up resistor) | | | | | | |
| V_{IH} | High level input voltage | $V_{DD} = 2.85\text{ to }3.15\text{ V}$ | $0.7 \times V_{DD}$ | | | V |
| V_{IL} | Low level input voltage | $V_{DD} = 2.85\text{ to }3.15\text{ V}$ | | | $0.3 \times V_{DD}$ | V |
| I_{IH} | High level input current | $V_{IH} = V_{DD} = 3.15\text{ V}$ | | | +1 | μA |
| I_{IL} | Low level input current | $V_{IL} = 0, V_{DD} = 3.15\text{ V}$ | -100 | | | μA |
| Digital inputs: FSELS, E_WR (contains a 70 k Ω pull-down resistor) | | | | | | |
| V_{IH} | High level input voltage | $V_{DD} = 2.85\text{ to }3.15\text{ V}$ | $0.7 \times V_{DD}$ | | | V |
| V_{IL} | Low level input voltage | $V_{DD} = 2.85\text{ to }3.15\text{ V}$ | | | $0.3 \times V_{DD}$ | V |
| I_{IH} | High level input current | $V_{IH} = V_{DD} = 3.15\text{ V}$ | | | +100 | μA |
| I_{IL} | Low level input current | $V_{IL} = 0, V_{DD} = 3.15\text{ V}$ | -1 | | | μA |
| Reference Divider input: f_r | | | | | | |
| I_{IHR} | High level input current | $V_{IH} = V_{DD} = 3.15\text{ V}$ | | | +100 | μA |
| I_{ILR} | Low level input current | $V_{IL} = 0, V_{DD} = 3.15\text{ V}$ | -100 | | | μA |
| Counter and phase detector outputs: Dout, PD_D, PD_U | | | | | | |
| V_{OLD} | Output voltage LOW | $I_{out} = 6\text{ mA}$ | | | 0.4 | V |
| V_{OHD} | Output voltage HIGH | $I_{out} = -3\text{ mA}$ | $V_{DD} - 0.4$ | | | V |
| Lock detect outputs: (Cext, LD) | | | | | | |
| V_{OLC} | Output voltage LOW, Cext | $I_{out} = 0.1\text{ mA}$ | | | 0.4 | V |
| V_{OHC} | Output voltage HIGH, Cext | $I_{out} = -0.1\text{ mA}$ | $V_{DD} - 0.4$ | | | V |
| V_{OLLD} | Output voltage LOW, LD | $I_{out} = 1\text{ mA}$ | | | 0.4 | V |

Table 6. AC Characteristics: $V_{DD} = 3.0\text{ V}$, $-40^{\circ}\text{ C} < T_A < 85^{\circ}\text{ C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|--|----------------------|-----|------|--------|
| Control Interface and Latches (see Figures 6, 7) | | | | | |
| f_{CLK} | Serial data clock frequency | (Note 1) | | 10 | MHz |
| t_{CLKH} | Serial clock HIGH time | | 30 | | ns |
| t_{CLKL} | Serial clock LOW time | | 30 | | ns |
| t_{DSU} | Sdata set-up time to Sclk rising edge | | 10 | | ns |
| t_{DHLD} | Sdata hold time after Sclk rising edge | | 10 | | ns |
| t_{PW} | S_WR pulse width | | 30 | | ns |
| t_{CWR} | Sclk rising edge to S_WR rising edge | | 30 | | ns |
| t_{CE} | Sclk falling edge to E_WR transition | | 30 | | ns |
| t_{WRC} | S_WR falling edge to Sclk rising edge | | 30 | | ns |
| t_{EC} | E_WR transition to Sclk rising edge | | 30 | | ns |
| Main Divider (Including Prescaler) | | | | | |
| F_{in} | Operating frequency | | 200 | 2200 | MHz |
| P_{Fin} | Input level range | External AC coupling | -5 | 5 | dBm |
| Main Divider (Prescaler Bypassed) | | | | | |
| F_{in} | Operating frequency | | 20 | 220 | MHz |
| P_{Fin} | Input level range | External AC coupling | -5 | 5 | dBm |
| Reference Divider | | | | | |
| f_r | Operating frequency | (Note 3) | | 100 | MHz |
| P_{fr} | Reference input power (Note 2) | Single ended input | -2 | | dBm |
| Phase Detector | | | | | |
| f_c | Comparison frequency | (Note 3) | | 20 | MHz |
| SSB Phase Noise ($F_{\text{in}} = 1.3\text{ GHz}$, $f_r = 10\text{ MHz}$, $f_c = 1.25\text{ MHz}$, $\text{LBW} = 70\text{ kHz}$, $V_{\text{DD}} = 3.0\text{ V}$, $\text{Temp} = -40^{\circ}\text{ C}$) | | | | | |
| | | 100 Hz Offset | | -75 | dBc/Hz |
| | | 1 kHz Offset | | -85 | dBc/Hz |

Note 1: fclk is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify fclk specification.

Note 2: CMOS logic levels can be used to drive reference input if DC coupled. Voltage input needs to be a minimum of 0.5 Vp-p. For optimum phase noise performance, the reference input falling edge rate should be faster than 80mV/ns.

Note 3: Parameter is guaranteed through characterization only and is not tested.

Typical Performance Data ($V_{DD} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$)

Figure 4. Typical RF Input Sensitivity

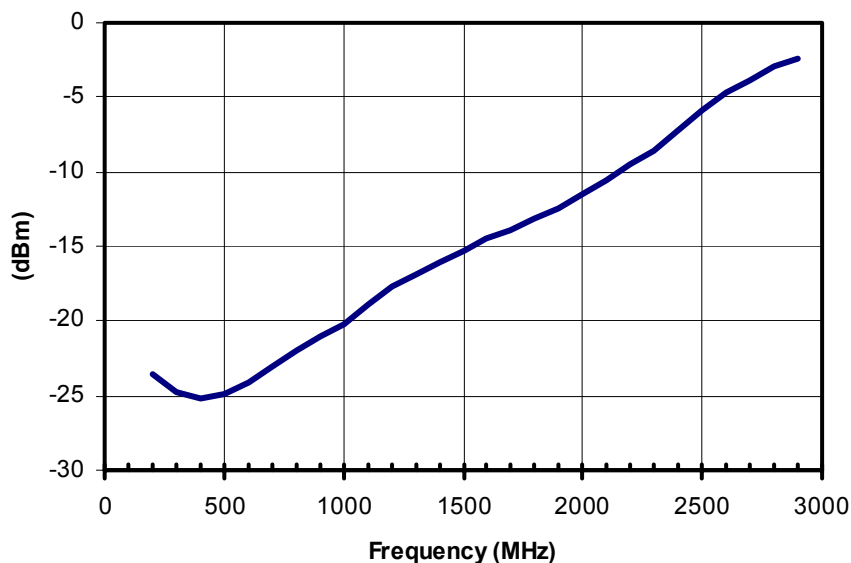
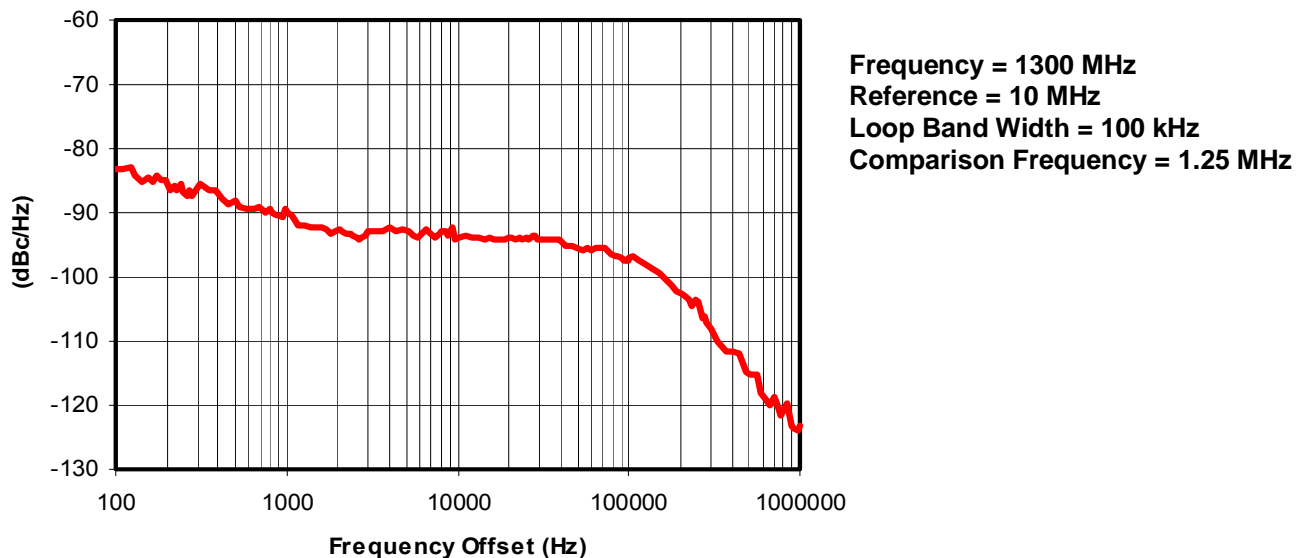


Figure 5. Typical Phase Noise Performance

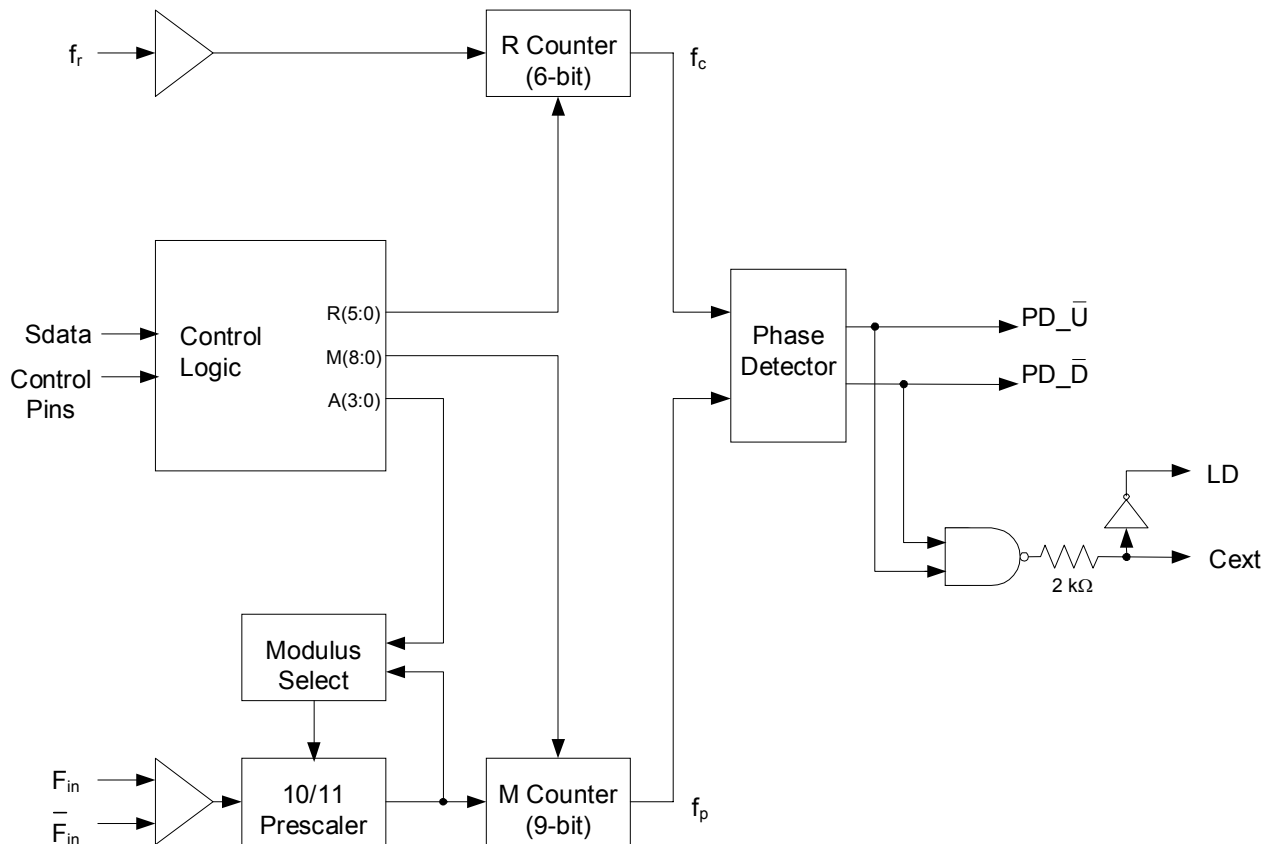


Functional Description

The PE3240 consists of a prescaler, counters, a phase detector and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic.

The phase-frequency detector generates up and down frequency control signals. Data is written into the internal registers via the three wire serial bus. There are also various operational and test modes and a lock detect output.

Figure 6. Functional Block Diagram



Main Counter Chain

Normal Operating Mode

Setting the Pre_en control bit “low” enables the $\div 10/11$ prescaler. The main counter chain then divides the RF input frequency (F_{in}) by an integer derived from the values in the “M” and “A” counters.

In this mode, the output from the main counter chain (f_p) is related to the VCO frequency (F_{in}) by the following equation:

$$f_p = F_{in} / [10 \times (M + 1) + A] \quad (1)$$

where $A \leq M + 1$, $1 \leq M \leq 511$

When the loop is locked, F_{in} is related to the reference frequency (f_r) by the following equation:

$$F_{in} = [10 \times (M + 1) + A] \times (f_r / (R+1)) \quad (2)$$

where $A \leq M + 1$, $1 \leq M \leq 511$

A consequence of the upper limit on A is that F_{in} must be greater than or equal to $90 \times (f_r / (R+1))$ to obtain contiguous channels. The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M.

Programming the M counter with the minimum allowed value of “1” will result in a minimum M counter divide ratio of “2”.

Prescaler Bypass Mode

Setting the frequency control register bit Pre_en “high” allows F_{in} to bypass the $\div 10/11$ prescaler. In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly. The following equation relates F_{in} to the reference frequency f_r :

$$F_{in} = (M + 1) \times (f_r / (R+1)) \quad (3)$$

where $1 \leq M \leq 511$

Reference Counter

The reference counter chain divides the reference frequency f_r down to the phase detector comparison frequency f_c .

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = f_r / (R + 1) \quad (4)$$

where $0 \leq R \leq 63$

Note that programming R with “0” will pass the reference frequency (f_r) directly to the phase detector.

Register Programming

Serial Interface Mode

While the E_WR input is “low” and the S_WR input is “low”, serial input data (Sdata input), B_0 to B_{19} , are clocked serially into the primary register on the rising edge of Sclk, MSB (B_0) first. The contents from the primary register are transferred into the secondary register on the rising edge of either S_WR according to the timing diagrams shown in Figure 7. Data are transferred to the counters as shown in Table 7 on page 9.

The double buffering provided by the primary and secondary registers allows for “ping-pong” counter control using the FSELS input. When FSELS is “high”, the primary register contents set the counter inputs. When FSELS is “low”, the secondary register contents are utilized.

While the E_WR input is “high” and the S_WR input is “low”, serial input data (Sdata input), B_0 to B_7 , are clocked serially into the enhancement register on the rising edge of Sclk, MSB (B_0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of E_WR according to the timing diagram shown in Figure 7. After the falling edge of E_WR, the data provide control bits as shown in Table 8 on page 9 will have their bit functionality enabled by asserting the Enh input “low”.

Table 7. Primary Register Programming

| Interface Mode | $\overline{\text{Enh}}$ | R ₅ | R ₄ | M ₈ | M ₇ | $\overline{\text{Pre_en}}$ | M ₆ | M ₅ | M ₄ | M ₃ | M ₂ | M ₁ | M ₀ | R ₃ | R ₂ | R ₁ | R ₀ | A ₃ | A ₂ | A ₁ | A ₀ |
|----------------|-------------------------|----------------|----------------|----------------|----------------|-----------------------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Serial* | 1 | B ₀ | B ₁ | B ₂ | B ₃ | B ₄ | B ₅ | B ₆ | B ₇ | B ₈ | B ₉ | B ₁₀ | B ₁₁ | B ₁₂ | B ₁₃ | B ₁₄ | B ₁₅ | B ₁₆ | B ₁₇ | B ₁₈ | B ₁₉ |

*Serial data clocked serially on Sclk rising edge while E_WR “low” and captured in secondary register on S_WR rising edge.



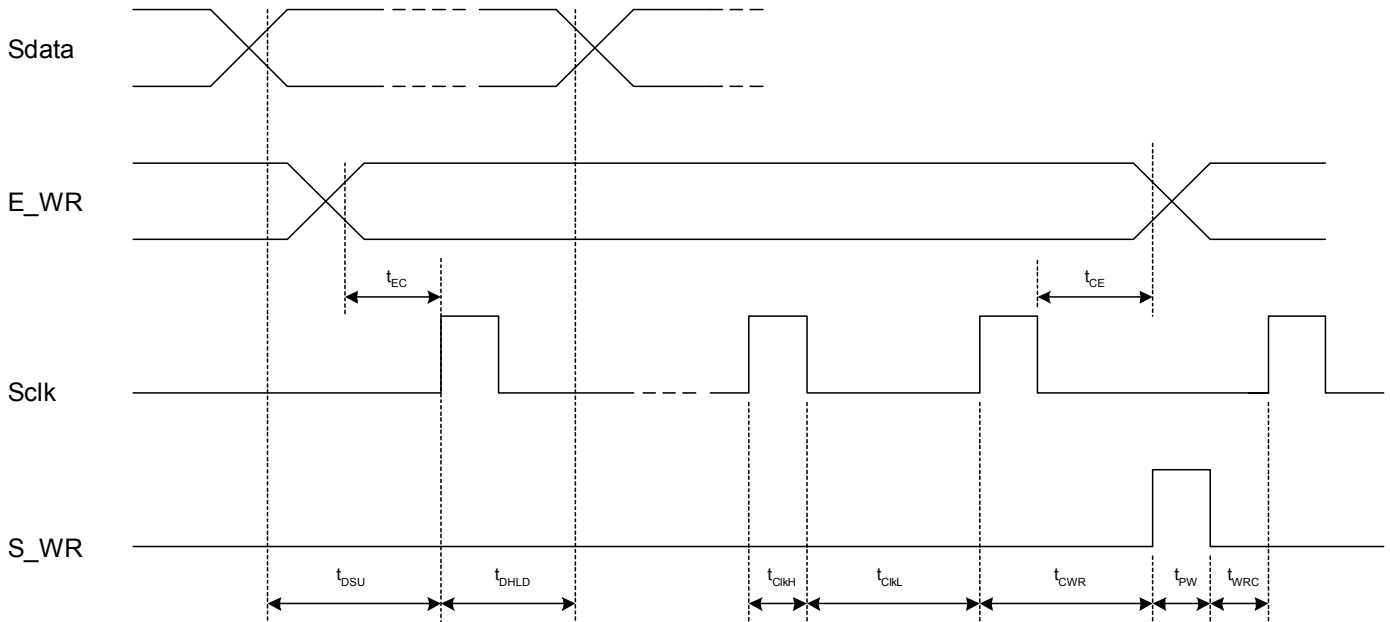
Table 8. Enhancement Register Programming

| Interface Mode | $\overline{\text{Enh}}$ | Reserved | Reserved | f _p Output | Power down | Counter load | MSEL output | f _c output | Reserved |
|----------------|-------------------------|----------------|----------------|-----------------------|----------------|----------------|----------------|-----------------------|----------------|
| Serial* | 0 | B ₀ | B ₁ | B ₂ | B ₃ | B ₄ | B ₅ | B ₆ | B ₇ |

*Serial data clocked serially on Sclk rising edge while E_WR “high” and captured in the double buffer on E_WR falling edge.



Figure 7. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 9. Enhancement Register Bit Functionality

| Bit Function | | Description |
|--------------|--------------|--|
| Bit 0 | Reserved** | |
| Bit 1 | Reserved** | |
| Bit 2 | f_p output | Drives the M counter output onto the Dout output. |
| Bit 3 | Power down | Power down of all functions except programming interface. |
| Bit 4 | Counter load | Immediate and continuous load of counter programming. |
| Bit 5 | MSEL output | Drives the internal dual modulus prescaler modulus select (MSEL) onto the Dout output. |
| Bit 6 | f_c output | Drives the reference counter output onto the Dout output |
| Bit 7 | Reserved** | |

** Program to 0

Phase Detector

The phase detector is triggered by rising edges from the main Counter (f_p) and the reference counter (f_c). It has two outputs, namely PD_U, and PD_D. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_D pulses “low”. If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_U pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c .

The phase detector gain is equal to $2.70 \text{ V} / 2 \pi$, which numerically yields $0.43 \text{ V} / \text{Radian}$.

PD_U and PD_D drive an active loop filter which controls the VCO tune voltage. PD_U pulses result in an increase in VCO frequency and PD_D results in a decrease in VCO frequency, for a positive K_v VCO.

A lock detect output, LD is also provided, via the pin Cext. Cext is the logical “NAND” of PD_U and PD_D waveforms, which is driven through a series 2 kohm resistor. Connecting Cext to an external shunt capacitor provides low pass filtering of this signal. Cext also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of PD_U and PD_D

Figure 9. Package Drawing

20-lead TSSOP

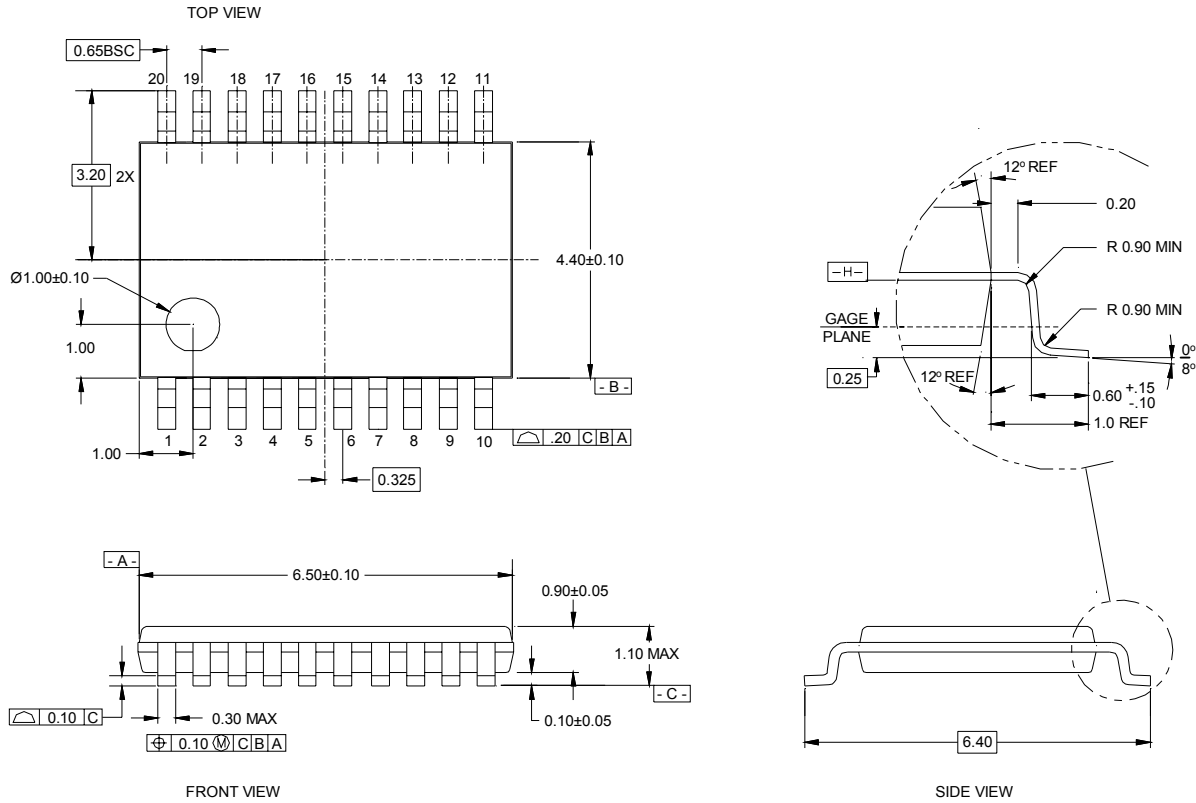


Table 10. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|------------|--------------|-------------------------|------------------|------------------|
| 3240-11 | PE3240 | PE3240-20TSSOP-74A | 20-lead TSSOP | 74 units / Tube |
| 3240-12 | PE3240 | PE3240-20TSSOP-2000C | 20-lead TSSOP | 2000 units / T&R |
| 3240-00 | PE3240EK | PE3240-20TSSOP-EVAL KIT | Evaluation Board | 1 / Box |

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Data Sheet Identification

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The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

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Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

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