



SPDT High Power UltraCMOS™ RF Switch DC - 6000 MHz, +50 dBm IIP3

Markets

- WiMAX
- Wireless Infrastructure
- High Performance RF Applications

Figure 1. Functional Diagram

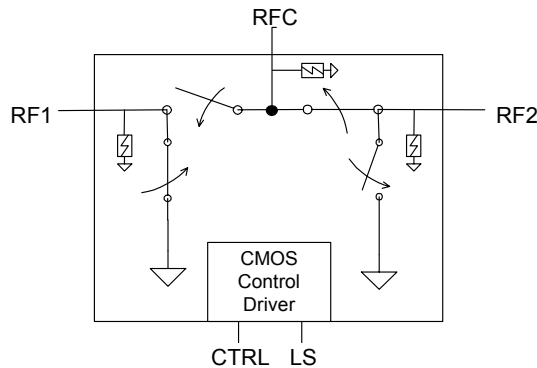
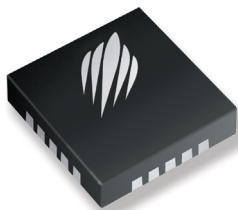


Figure 2. Package Type
 20-lead 4x4 mm QFN



Features

- High linearity: +50 dBm IIP3 from DC - 6000 MHz
- Low insertion loss: 0.65 dB at 3500 MHz, 0.90 dB at 6000 MHz
- High isolation of 27 dB at 3500 MHz, 21 dB at 6000 MHz
- High power 1 dB compression point of +34 dBm
- Single-pin 2.75 V CMOS logic control
- Logic select pin to change definition of logic control
- 4x4 mm QFN package

Product Description

The PE42555 is a HaRP™-enhanced High Power RF Switch designed to support the requirements of the Wireless Infrastructure and high performance RF applications market. It maintains excellent RF performance and linearity from DC through 6000 MHz. The PE42555 integrates on-board CMOS control logic driven by a single-pin, low voltage CMOS control input. It also has a logic select pin which enables changing the logic definition of the control pin. Additional features include a novel user defined logic table, enabled by the on-board CMOS circuitry. The PE42555 also exhibits outstanding isolation that approaches 21 dB at 6000 MHz and is offered in a small 4x4 mm QFN package.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Table 1. Electrical Specifications @ +25 °C, V_{DD} = 2.75 V (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Min	Typical	Max	Units
Operation Frequency ¹		DC		6000	MHz
Insertion Loss	9 KHz 3500 MHz 6000 MHz		0.55 0.65 0.90	0.65 0.75	dB dB dB
Isolation – RF1 to RF2	3500 MHz 6000 MHz	25	27 21		dB dB
Return Loss	3500 MHz 6000 MHz		15 16		dB dB
Switching Time	50% CTRL to 0.1 dB final value		7		μs
Input 1 dB Compression	6000 MHz	32	34		dBm
Input IP3	6000 MHz		+50		dBm

Note 1: Device linearity will begin to degrade below 10 MHz.

Table 2. Operating Specifications

Parameter	Min	Typ	Max	Units
V _{DD} Positive Power Supply Voltage	2.5	2.75	3.0	V
V _{DD} Negative Power Supply Voltage	-2.5	-2.75	-3.0	V
I _{DD} Power Supply Current (V _{DD} = 3V, V _{CTRL} = 3V)		20		μA
Control Voltage High	0.7xV _{DD}			V
Control Voltage Low			0.3xV _{DD}	V
RF Power In: 9 kHz • 600 kHz 600 kHz • 3 MHz 3 Mhz • 6 GHz			13 20 31	dBm dBm dBm

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V _{DD}	Power supply voltage	-0.3	4.0	V
V _I	Voltage on any input except for CTRL and LS inputs	-0.3	V _{DD} +0.3	V
V _{CTRL}	Voltage on CTRL input		4.0	V
V _{LS}	Voltage on LS input		4.0	V
T _{ST}	Storage temperature range	-65	150	°C
T _{OP}	Operating temperature range	-40	85	°C
P _{IN}	Input Power: 9 kHz • 600 kHz 600 kHz • 3 MHz 3 Mhz • 6 GHz		16 23 34	dBm dBm dBm
V _{ESD}	ESD voltage (Human Body Model)		500	V

Part performance is not guaranteed under these conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

Table 4. Pin Descriptions

Pin No.	Pin Name	Description
13	RF2	RF2 port. ²
1, 2, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15, 19	GND	Ground Connection. Traces should be physically short and connected to the ground plane. This pin is connected to the exposed solder pad that also must be soldered to the ground plane for best performance.
3	RF1	RF1 port. ²
16	CTRL	CMOS level: See Table 5.
8	RFC	Common RF port for switch. ²
17	LS	Logic Select - Used to determine the definition for the CTRL pin (see Table 5)
18	V _{SS}	Negative power supply. Apply nominal -2.75 V supply.
20	V _{DD}	Nominal 2.75 V supply connection

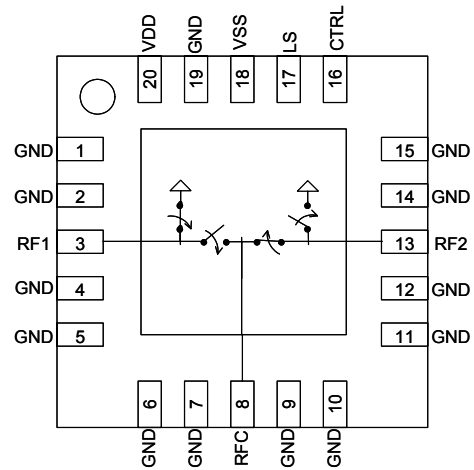
Note 2: All RF pins must be held at 0 VDC or the DC must be blocked with an external series capacitor .

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

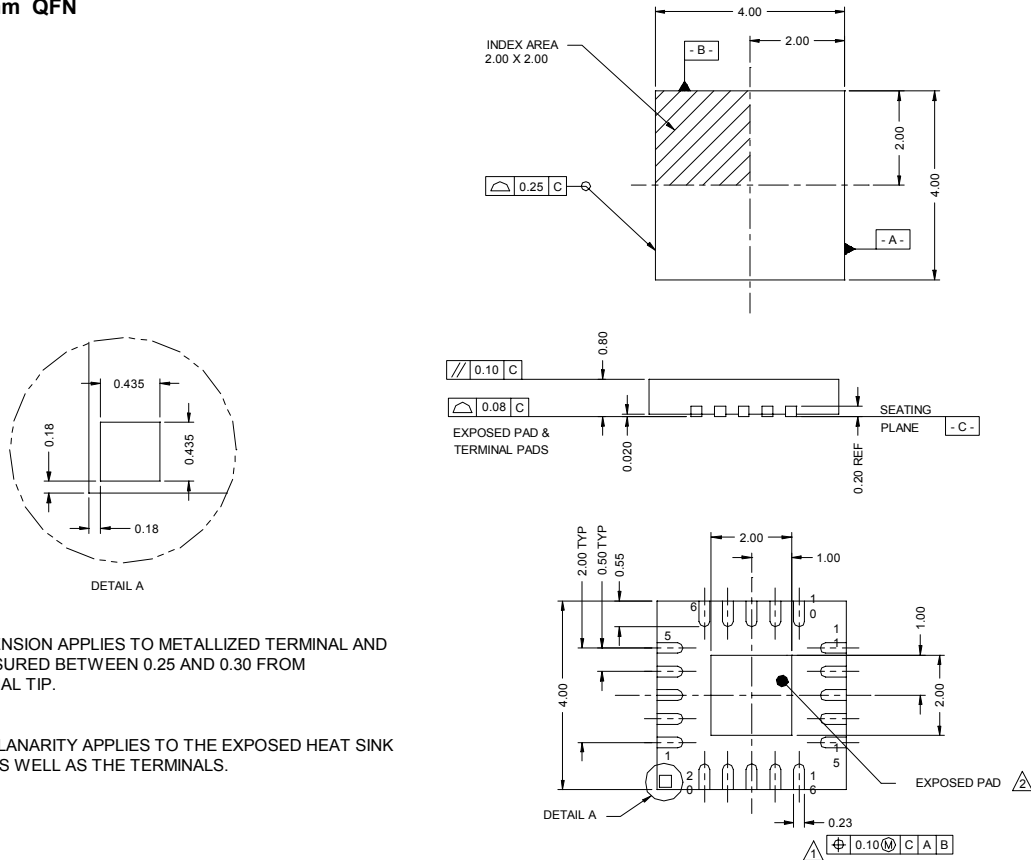
Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Figure 3. Pin Configuration (Top View)**Table 5. Control Logic Truth Table**

LS	CTRL	RFC-RF1	RFC-RF2
0	0	off	on
0	1	on	off
1	0	on	off
1	1	off	on

Figure 4. Package Drawing (mm)
20-lead 4x4 mm QFN



1. DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 FROM TERMINAL TIP.
2. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 5. Tape and Reel Drawing

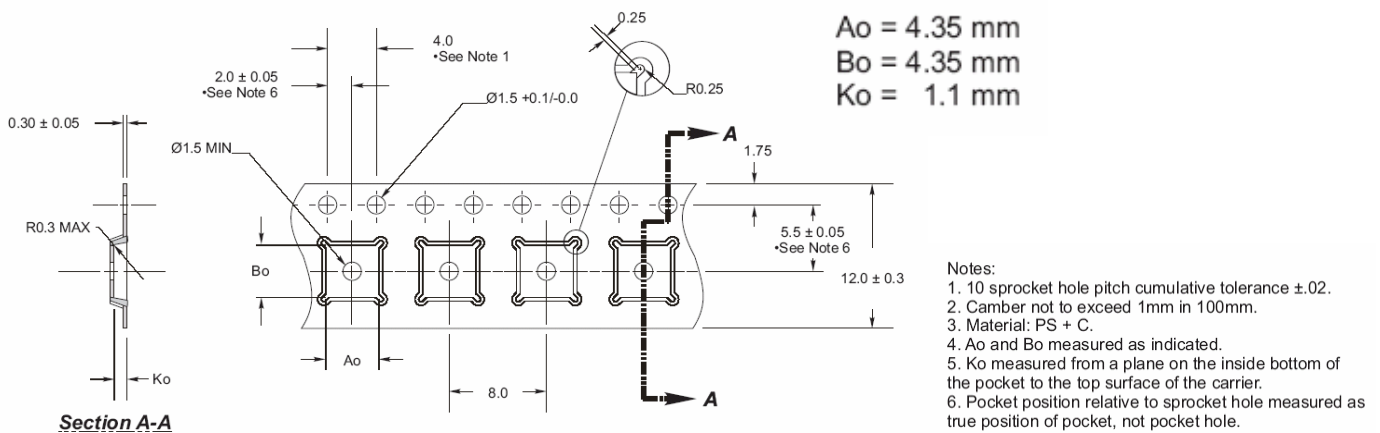


Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
42555-00	PE42555-EK	PE42555-20QFN 4x4 mm-EK	Evaluation Kit	1 / Box
42555-51	42555	PE42555G-20QFN 4x4 mm-75A	Green 20-lead 4x4 mm QFN	Parts in Tubes or Cut Tape
42555-52	42555	PE42555G-20QFN 4x4 mm-3000C	Green 20-lead 4x4 mm QFN	3000 units / T&R

Sales Offices

The Americas

Peregrine Semiconductor Corporation

9450 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

Space and Defense Products

Americas:

Tel: 858-731-9453

Europe, Asia Pacific:

180 Rue Jean de Guiramand
13852 Aix-En-Provence Cedex 3, France
Tel: +33-4-4239-3361
Fax: +33-4-4239-7227

North Asia Pacific

Peregrine Semiconductor K.K.

Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

Peregrine Semiconductor, Korea

#B-2402, Kolon Tripolis, #210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-480 S. Korea
Tel: +82-31-728-4300
Fax: +82-31-728-4305

South Asia Pacific

Peregrine Semiconductor, China

Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

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西安劳动南路 88 号电子商城二楼 D23 号

TEL: 029-81022619 13072977981 FAX:029-88789382