



PE3503 EVALUATION KIT USER'S MANUAL

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1. Introduction

The PE3503 is a high performance, low power monolithic divider manufactured using Peregrine's UTSi CMOS process. It features a fixed divide ratio of 8 and can operate with input signals of up to 3.5 GHz. The PE3503 operates on a nominal 3 volts supply and draws only about 14mA of current. The wideband frequency of operation of the PE3503 makes it an ideal part used in a DBS down converter system. Figure 1 illustrates how the PE3503 may be implemented in such a system.

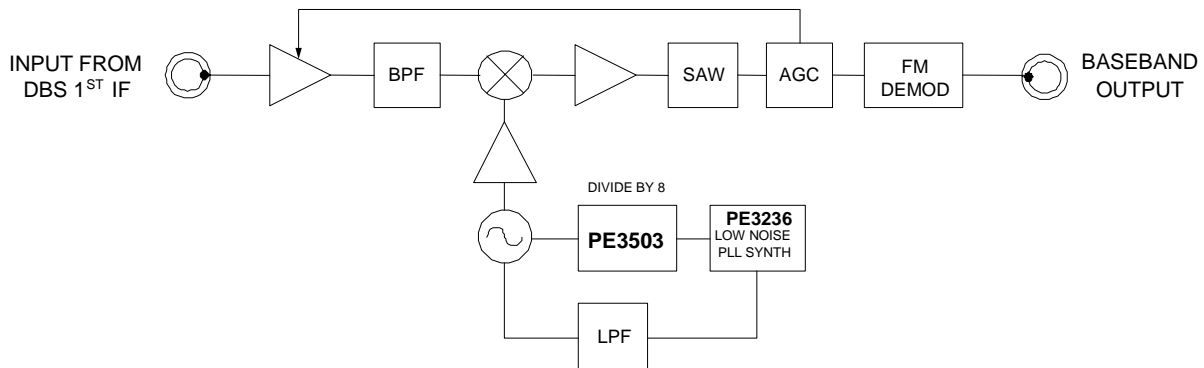


Figure 1. PE3503 System Application

2. Evaluation Board Description

The PE3503 evaluation board is depicted below in Figure 2. The input is driven into the RF In port while the divided output is taken at Out 1. Both input and output contain footprints for AC coupling capacitors (C3 and C1 respectively). The power supply connection is provided near the top of the evaluation board (J2) with the lower pin as the supply and the upper pin as ground. In addition C2, C5, and C10 are placeholders for power supply decoupling capacitors. Placeholders C4, C6, and C8 are needed for required bypass capacitors. **Note: C4 and C6 are located on the underside of the evaluation board.**

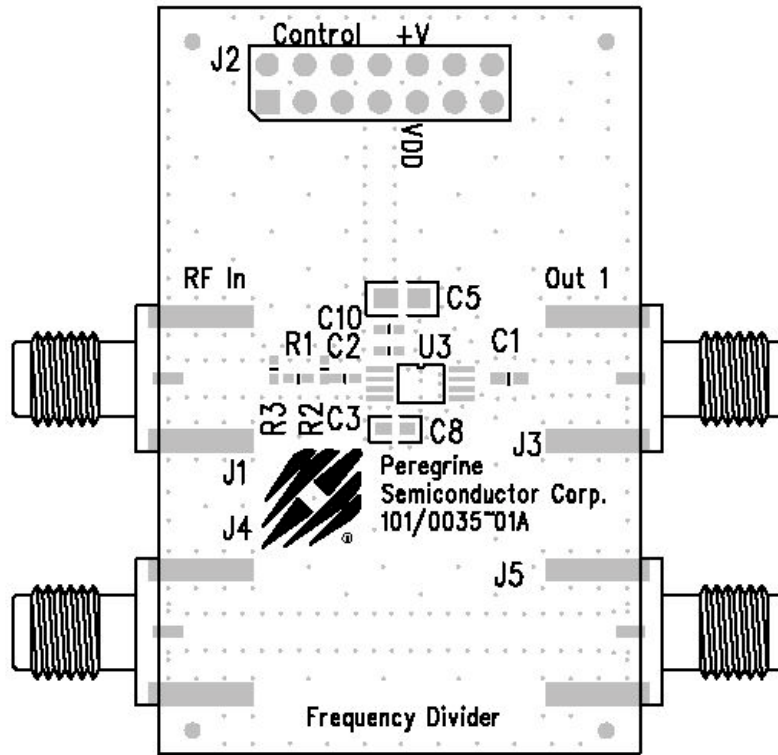


Figure 2. PE3503 Evaluation Board

3. Evaluation Board Test Setup

The PE3503 can be tested on the evaluation board using the test setup shown below in Figure 3. In the test setup, it is essential that the power supply is properly decoupled and bypass capacitors are used for pin 3. In addition, the input and output need to be AC coupled.

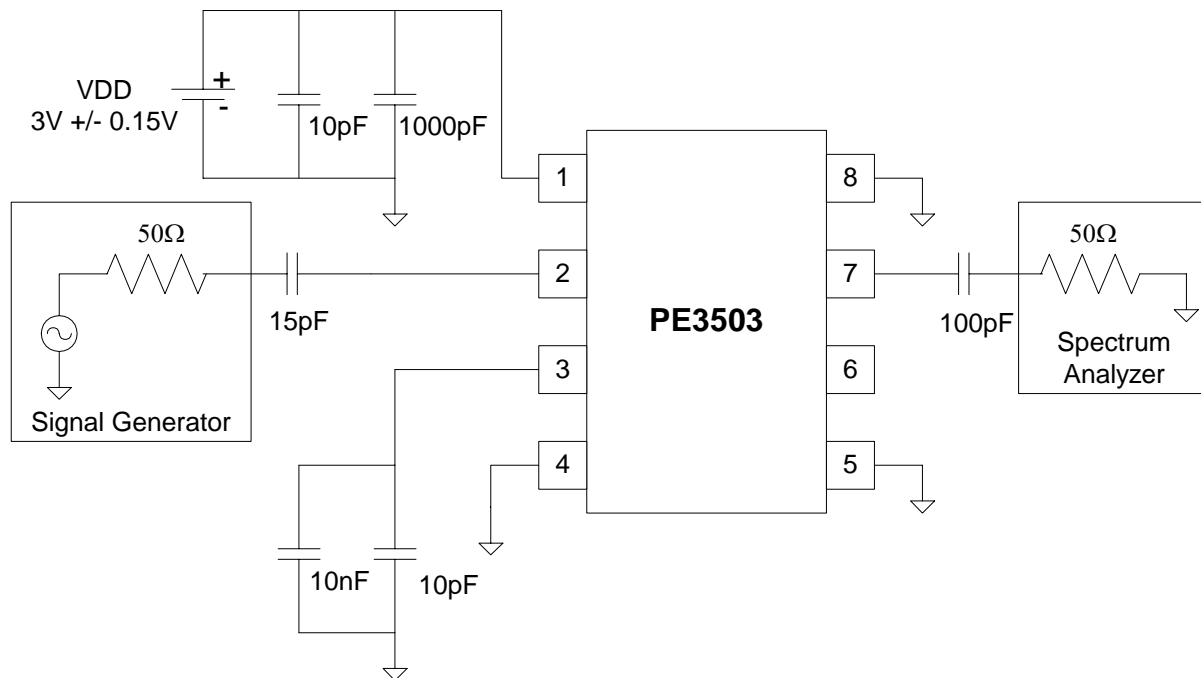


Figure 3. PE3503 Test Setup

4. Testing

Test measurements were made using the test setup depicted above in Figure 3. With a nominal supply of 3 volts, the input signal generator was swept from 2000 MHz to 3500 MHz with the input power set at -9dBm . The output power was measured with a power meter.

5. Revision History

DCN#	Revision	Date:	Originator:	Description of Change:
01227	00A	04/19/01	D. Jones	Initial Release

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