PRELIMINARY

I²C to PARALLEL CONVERTER

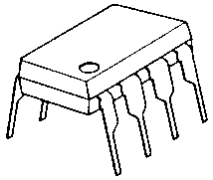
■ GENERAL DESCRIPTION

The **NJU3730** is a serial-to-parallel converter IC, which converts I²C serial data into 3 bits parallel data.

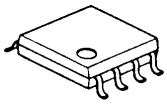
The **NJU3730** incorporates selectable three kinds of I²C-slave-address, which are used to distinguish one of three **NJU3730**s. Thus, maximum three of the NJU3730 can be connected onto the same I²C-bus and each NJU3730 operates as a controller for non-I²C device or extensive ports.

The **NJU3730** is suitable for I²C-BUS applications such as TV, AV amplifier, mini Stereo component, speaker system and others.

■ PACKAGE OUTLINE



NJU3730D

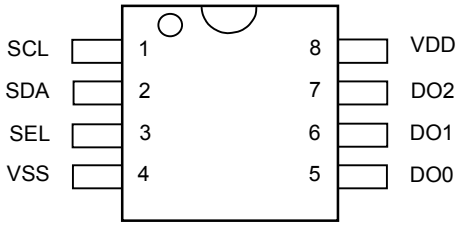


NJU3730M

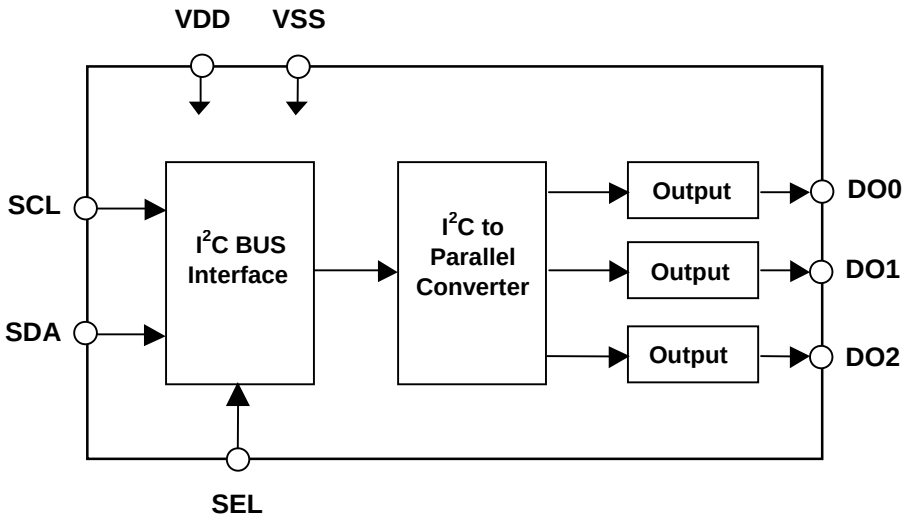
■ FEATURES

- Converts I²C data to parallel data
- 3 bits parallel output port
- Selectable 3 slave addresses
- Operating Voltage 4.5 to 5.5V
- C-MOS Technology
- Package Outline DIP8, DMP8

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



*Purchase of I²C components of New Japan Radio Co., Ltd or one of its sublicensed Associated Companies conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ TERMINAL DESCRIPTION

NO.	SYMBOL	I/O	FUNCTION
1	SCL	I	I^2C-bus Serial Clock Input Terminal
2	SDA	I/O	I^2C-bus Serial Data Input/Output Terminal
3	SEL	I	Slave-address Select Terminal
4	VSS	-	GND: VSS=0V
5	DO0	O	Output Terminal 0
6	DO1	O	Output Terminal 1
7	DO2	O	Output Terminal 2
8	VDD	-	Power Supply: VDD=+5V

■ FUNCTIONAL DESCRIPTION

(1) Data Transmission

NJU3730 is controlled by I^2C-bus using the SCL and the SDA terminals. NJU3730 is a receive-only slave, and doesn't correspond to the general call address ("0000 0000").

The data transfer is available, when the following timing is executed. When the data transferred exactly, NJU3730 outputs "L" level signal from the SDA terminal as acknowledge signal just after each 8 bits.

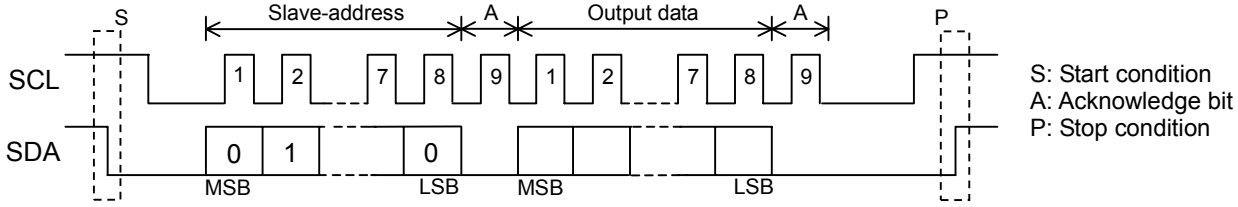


Fig.1 Data Transfer Timing

(1-1) Start Condition

A falling edge of the SDA terminal while the SCL terminal is "H" level is defined as the Start condition. After the Start condition, NJU3730 starts reading the data.

(1-2) Slave-address

The first byte defines the slave-address. When NJU3730 acknowledges a coincidence its own address with the address information, it outputs the Acknowledge at 9^{th} bit timing.

(1-3) Output Data

The second byte defines the output data. NJU3730 outputs the Acknowledge at 9^{th} bit timing.

(1-4) Stop Condition

A rising edge of the SDA terminal while the SCL terminal is "H" level is defined as the Stop condition. After the Stop condition, NJU3730 finishes reading the data.

(2) Slave-address

The slave-address is selected by the condition of the SEL terminal.

SEL	Slave-address
Low Level	0100 0000
Open	0100 0010
High Level	0100 0100

(3) Output Terminal (DO0-2) Settings

Output level of the DO0 to DO2 terminals is selected by the condition of the LSB 3 bits of the output data.

DO2	DO1	DO0	Output Data	Initial Value
L	L	L	XXXX X000	✓
L	L	H	XXXX X001	
L	H	L	XXXX X010	
L	H	H	XXXX X011	
H	L	L	XXXX X100	
H	L	H	XXXX X101	
H	H	L	XXXX X110	
H	H	H	XXXX X111	

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_I	-0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	500 (DIP) 300 (DMP)	mW
Operating Temperature	Topr	-40 to +85	°C
Storage Temperature	Tstg	-40 to +125	°C

Note 1) All voltage values are specified as VSS=0V.

Note 2) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.

Note 3) Decoupling capacitors should be connected between VDD-VSS due to the stabilized operation.

■ ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{DD}=5.0V, V_{SS}=0.0V, unless otherwise noted)

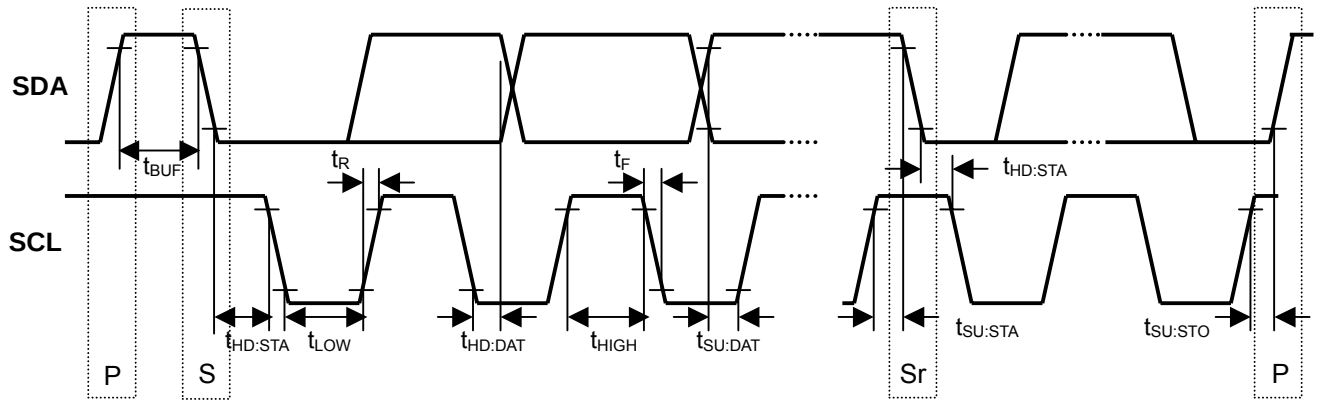
● DC Characteristics

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD}		4.5	5.0	5.5	V
Operating Current	I_{DD}	No signal, without pull up resistor	-	250	300	μA
Low level Input Voltage	V_{IL}		0	-	$0.2V_{DD}$	V
High level Input Voltage	V_{IH}		$0.7V_{DD}$	-	V_{DD}	V
Low level Output Voltage	V_{OL}	I_{OL}=1mA	0	-	0.4	V
High level Output Voltage	V_{OH}	I_{OH}=-1mA	V_{DD}-0.4	-	V_{DD}	V

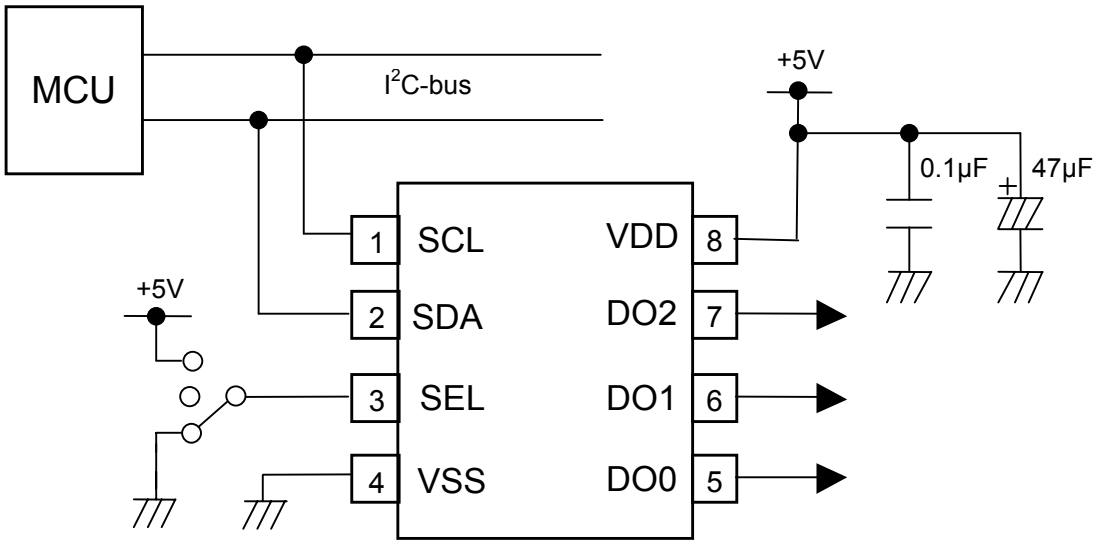
● AC Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Clock Frequency	f_{SCL}	-	-	100	kHz
Data Change Minimum Waiting Time	t_{BUF}	4.7	-	-	μs
Data Transfer Start Minimum Waiting Time	$t_{HD:STA}$	4.0	-	-	μs
Low Level Clock Pulse Width	t_{LOW}	4.7	-	-	μs
High Level Clock Pulse Width	t_{HIGH}	4.0	-	-	μs
Minimum Start Preparation Waiting Time	$t_{SU:STA}$	4.7	-	-	μs
Minimum Data Hold Time	$t_{HD:DAT}$	5.0	-	-	μs
Minimum Data Preparation Time	$t_{SU:DAT}$	250	-	-	ns
Rise Time	t_R	-	-	1.0	μs
Fall Time	t_F	-	-	300	ns
Minimum Stop Preparation Waiting Time	$t_{SU:STO}$	4.0	-	-	μs

Note 4) I^2C-bus Load Condition: Pull up resistance 4kΩ (Connected to +5V),
Load capacitance 200pF (Connected to GND).



■ APPLICATION CIRCUIT



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