# DOLBY PRO LOGIC SURROUND DECODER

■ GENERAL DESCRIPTION

The NJM2177A is a higher level integration and high quality audio performance monolithic IC designed for use in Dolby Pro Logic Surround System. The NJM2177A provides all the necessary function for a complete Pro Logic processor except time delay; Automatic input balance, noise sepuencer, adaptibve matrix, center mode control, and modified B-type noise reduction all on chip.

In addition to Dolby Pro Logic function including Dolby 3-stereo, this device provides two channel bypass mode and two special outputs used for other surround conbeniently.
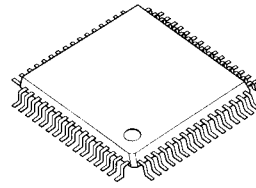
(note) Dolby and the double-D symbol are trademarks of Dolby Laboratories Licensing Corporation. San Francisco, CA94103-4813, USA.

This device available only to licensees of Dolby Lab.

Licensing and application information may be obtained from Dolby Lab.

■ PACKAGE OUTLINE

NJM2177AFG1

■ FEATURES

● Operating Voltage	9 to 13V
● Dolby operating level	300mVrms
● Lower Operating Current	34mA typ.
● Internal mode control switches	
● Package	**TQFP64**

■ FUNCTIONS

● Auto input balance and buffer
● Noise sequencer; a Noise generator, a sequencer controlled by external two bits
● Adaptive Matrix
● Center mode control; ON/OFF, Normal/Phantom/Wideband
● Modified Dolby B Type Noise Reduction and OP amp. for 7kHz low-pass filter
● Operating mode control; 4ch(L,C,R), 3ch(L,C,R), 2ch(no processing)
● $L+R$ and $L-R$ output

■ ACTIVE SURROUND DECODER BLOCK DIAGRAM
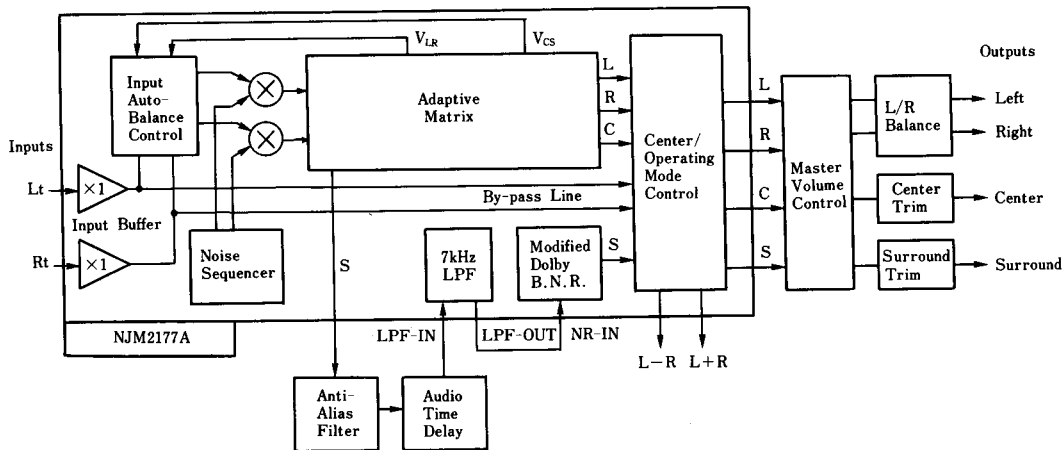
■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V$^+$=12V, 0dB　Reference is 300mV/1kHz at C-OUT. Unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Overall						
Operating Voltage Range	V$_{OP}$		9.0	—	13.0	V
Operating Current	I$_{CC}$	No signal	—	34.0	40.0	mA
Reference Voltage	V$_{ref}$	No signal	—	4.0	—	V
Control SW input voltage						
2ch Mode	V$_C$-2ch	MODE-CNT PIN	0.0	—	0.8	V
3ch	V$_C$-3ch	MODE-CNT PIN	—	Open	—	
4ch	V$_C$-4ch	MODE-CNT PIN	3.8	—	7.0	V
Center on	V$_C$-con	CENTER-CNT PIN	2.4	—	7.0	V
Center off	V$_C$-coff	CENTER-CNT PIN	0.0	—	0.8	V
Noise Seq. on	V$_C$-nson	NOISE-CNT-E PIN	0.0	—	0.8	V
Noise Seq. off	V$_C$-nsoff	NOISE-CNT-E PIN	3.2	—	7.0	V
Noise Seq. channel select H	V$_C$-nssH	NOISE-CNT-A and NOISE-CNT-B PIN	3.2	—	7.0	V
Noise Seq. channel select L	V$_C$-nssL	NOISE-CNT-A and NOISE-CNT-B PIN	0.0	—	0.8	V
Modified B Noise Reduction (0dBd Reference is input leve at NR-IN when adjust to 300mV/100Hz at S-OUT)						
Voltage Gain	GV-BNR	V$_{in}$= 0dBd, f=100Hz	—	9.0	—	dB
Decode Responce 1	D$_{ec1}$	V$_{in}$=0dBd, f=1.0kHz	−1.6	−0.1	1.4	dB
2	D$_{ec2}$	V$_{in}$=−15dBd, f=1.4kHz	−3.0	−1.5	0.0	dB
3	D$_{ec3}$	V$_{in}$=−20dB, f=1.4kHz	−4.9	−3.4	−1.9	dB
4	D$_{ec4}$	V$_{in}$=40dBd, f=5.0kHz	−6.8	−5.3	−3.8	dB
T.H.D	THD-NR	V$_{in}$=0dBd, f=1.0kHz	—	0.07	—	%
Headroom	HR-NR	V$^+$=9V AT T.H.D.=1%	15.0	17.0	—	dB
SN Ratio	SN-NR	Rg=0, weighted CCIR/ARM	76	82	—	dB
Noise sequencer						
OUTPUT Noise level	V$_{no}$		−15	−12.5	−10	dB
Output Noise Level Accuracy relative to Cch Lch Rch S'ch	ΔV$_{no}$		−0.5	0.0	0.5	dB
Adaptive Matrix						
Output Level Accuracy relative to Cch L,R,S'ch out	ΔVol		−0.5	0.0	0.5	dB
Matrix Rejection relative L,R,C,S'ch out	Mr		25.0	40.0	—	dB
T.H.D L,R,C,S'ch out	THD-AM		—	0.02	—	%
Headroom L,R,C,S'ch out	HR-AM	V$^+$=9V at T.H.D=1%	15.0	15.7	—	dB
Signal to Noise Ratio L,R,C,S' ch out	SN-AM	Rg=0, weighted CCIR/ARM	78	83	—	dB
Auto Balance						
Capture Range	CPR		—	±5	—	dB
Error collection	CER		—	±4	—	dB
T.H.D Lt, Rt OUT	THD-AB		—	0.03	—	%
S/N Lt, Rt OUT	SN-AB	Rg=0, weighted CCIR/ARM	78	83	—	dB
Headroom Lt,Rt OUT	HR-AB	V$^+$=9V at T.H.D=1%	15.0	17.0	—	dB
L+R & L-R OUTPUT						
Output Level Accuracy relative to Cch L+R, L−R ch	ΔVol-OP		—	0.0	—	dB
T.H.D	THD-OP		—	0.02	—	%
S/N	SN-OP	Rg=0, weighted CCIR/ARM	—	92	—	dB
Headroom	HR-OP	Vcc=9V at T.H.D=1%	—	17.0	—	dB

NJM2177A

■ **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	$-20 \sim +75$	°C
Storage Temperature Range	T_{stg}	$-40 \sim +125$	°C

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