PRELIMINARY

STEREO BTL OUTPUTS SWITCHING DRIVER FOR Class D AMPLIFIER

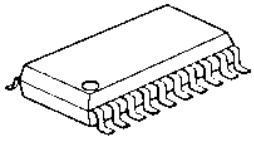
■ GENERAL DESCRIPTION

The **NJU8714** is a stereo BTL outputs switching driver for class D amplifier. It receives PWM/PDM signals from DSP outputs, and drives headphones or speakers by BTL outputs.

Output drivers are composed of Series-Connected N-channel FETs, and output voltage levels can be controlled by variable power supply with keeping all of input signal information.

The NJU8714 incorporates BTL outputs amplifiers, which eliminate AC coupling capacitors. Also, it provides "SEL" terminal which selects "Synchronous" or "Asynchronous". "Asynchronous" can be reduced the operating current. Therefore, it is suitable for portable audio set and others.

■ PACKAGE OUTLINE

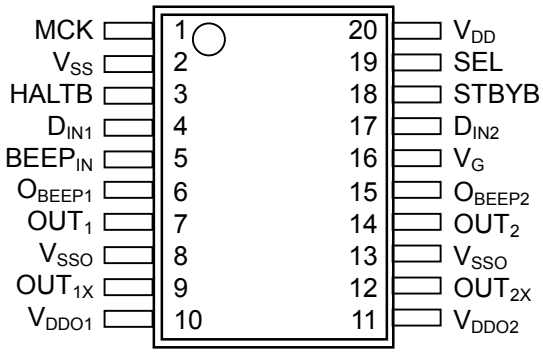


NJU8714VB2

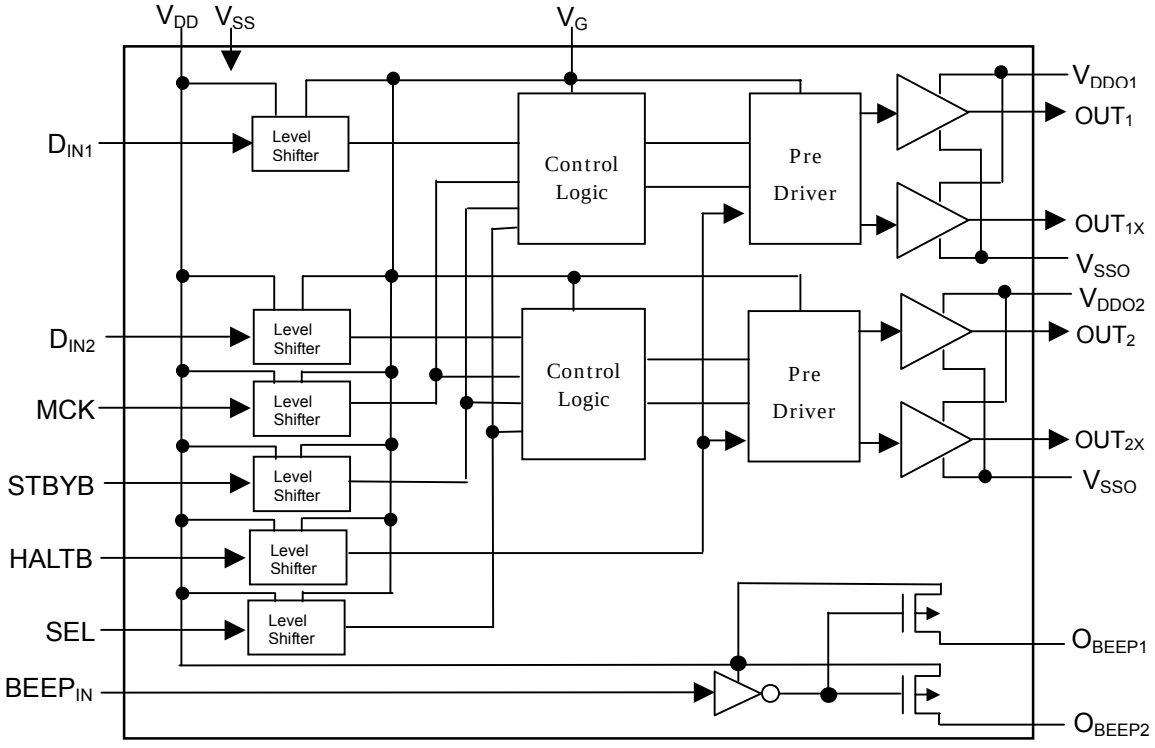
■ FEATURES

- 2-channel 1bit Audio Signal Input
- Stereo BTL Outputs
- Output Power : Typ.150mW@8Ω
- BEEP Function
- Standby Function
- Output Driver Control Function
- Operating Voltage V_{DD}: 1.7V to 2.7V
  V_{DDO}: 0V to 2.0V
  V_G: 4.5V to 5.25V
- CMOS Technology
- Package Outline :SSOP20-B2

■ PIN CONFIGURATION



■ BLOCK DIAGRAM

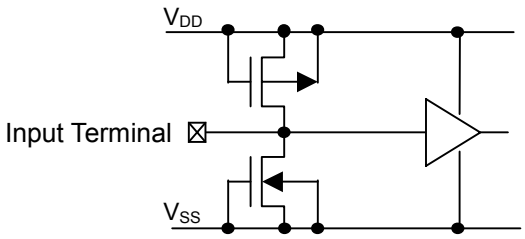


■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	FUNCTION
1	MCK	I	Master Clock Input Terminal
2	V_{SS}	-	Power GND: V_{SS}=0V (Note.1)
3	HALTB	I	Output Driver Control Terminal
4	D_{IN1}	I	1bit Data Input Terminal 1
5	$BEEP_{IN}$	I	BEEP Signal Input Terminal
6	O_{BEEP1}	O	BEEP Output terminal 1
7	OUT_1	O	Positive Output Terminal 1
8,13	V_{SSO}	-	Output GND terminal: V_{SS}=0V (Note. 1)
9	OUT_{1X}	O	Negative Output 1
10	V_{DDO1}	-	Output Power supply 1(Note. 2)
11	V_{DDO2}	-	Output Power supply 2(Note. 2)
12	OUT_{2X}	O	Negative Output 2
14	OUT_2	O	Positive Output Terminal 2
15	O_{BEEP2}	O	BEEP Output terminal 2
16	V_G	-	Pre-driver Power supply
17	D_{IN2}	I	1bit Data Input Terminal 2
18	STBYB	I	Standby control terminal (L:Standby)
19	SEL	I	Input Signal Synchronization With “MCK” (H: Synchronous., L: Asynchronous.)
20	V_{DD}	-	Power Supply: V_{DD}=2.5V

(Note. 1) Pin No.2(V_{SS}), 8(V_{SSO}) and 13(V_{SSO}) should be connected at the nearest point to the IC.
(Note. 2) Pin No.10(V_{DDO1}) and 11(V_{DDO2}) should be connected at the nearest point to the IC.

■ INPUT TERMINAL STRUCTURE



MCK, HALTB, D_{IN1}, D_{IN2}, $BEEP_{IN}$, STBYB, SEL

■ FUNCTIONAL DESCRIPTION

(1) Signal Output

The $OUT_{1/1X}$ and $OUT_{2/2X}$ generate respectively L-channel and R-channel output signals, which will be converted to analog signals via external 2nd-order or higher LC filter. A switching regulator with a high response against a voltage fluctuation is the best selection for the V_{DDO1} and V_{DDO2}, which are the power supply for output drivers. To obtain better T.H.D. performance, the stabilization of the power is required.

(2) Master Clock (MCK)

Input 1-bit audio signals such as PWM or PDM to the D_{IN1} and D_{IN2} pins. By setting the SEL pin to "H", master clock (MCK) synchronizes the audio signal inputs (D_{IN1} and D_{IN2}). In case of "SEL" = "L", input signals go into the amplifier circuits by own timing. Therefore, it requires careful design of PCB patterns from DSP to **NJU8714**.
The setup time and the hold time should be kept in the AC characteristics because D_{IN1} and D_{IN2} are fetched with the rising edge of MCK. MCK requires jitter-free or jitter as small as possible because the jitter downs S/N ratio.

(3) Power Supply

V_{DD} : Power supply for input part.
V_G : Power supply for control logic and pre-driver which drives the transistor gates of output drivers. It requires much higher power supply voltage than V_{DDO1} and V_{DDO2} for better T.H.D..
V_{DDO1}, V_{DDO2} : Power supply for output drivers.

(4) Output Control

Output circuit is selected by the conditions of STBYB, HALTB, SEL, D_{IN1}, D_{IN2} and MCK.

STBYB	HALTB	SEL	D_{IN1}, D_{IN2}	MCK	OUT_1	OUT_2	OUT_{1X}	OUT_{2X}
L	L	*	*	*	V_{SSO}	V_{SSO}	V_{SSO}	V_{SSO}
H		*	*	*				
L	H	*	*	*	Hi-z	Hi-z	Hi-z	Hi-z
H	H	L	L	*	V_{SSO}	V_{SSO}	V_{DDO1}	V_{DDO2}
			H		V_{DDO1}	V_{DDO2}	V_{SSO}	V_{SSO}
		H	L	⊓	V_{SSO}	V_{SSO}	V_{DDO1}	V_{DDO2}
			H		V_{DDO1}	V_{DDO2}	V_{SSO}	V_{SSO}

*Don't care
BEEP circuit is operated regardless of STBYB and HALTB.

(5) Input Signal Synchronization Function

D_{IN1} and D_{IN2} are synchronized with master clock by setting SEL pin to "H".
By setting SEL pin to "L", D_{IN1} and D_{IN2} are asynchronous with master clock.

(6) Output Driver Control Function

By setting HALTB pin to "L", high side output drivers become OFF and Low side output drivers become ON, then both of $OUT_{1/1X}$ and $OUT_{2/2X}$ output V_{SSO} level signals. This function works regardless of STBYB pin setting.

(7) Standby Control Function

By setting STBYB pin to "L", the NJU8714 becomes standby condition. During standby condition, by setting HALTB to "L", $OUT_{1/1X}$ and $OUT_{2/2X}$ become V_{SSO}, and by setting HALTB pin to "H", $OUT_{1/1X}$ and $OUT_{2/2X}$ become Hi-z.

To save the power supply current at standby, MCK requires "L" level.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 to +2.75	V
	V_G	V_{DD} to +5.5	
	V_{DDO}	-0.3 to +5.5	
Input Voltage	Vin	-0.3 to V_{DD}+0.3	V
Operating Temperature	Ta	-40 to +85	°C
Storage Temperature	Tstg	-40 to +125	°C
Power Dissipation	P_D	450*	mW

* : Mounted on two-layer board of based on the JEDEC.

Note.1) All voltage values are specified as V_{SS}=0V.

Note.2) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.

Note.3) The relations of $V_{DDO} < V_G$ must be maintained during operations.

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}=2.5V, V_G=5.0V, V_{DDO1}= V_{DDO2}=1.7V, V_{SS}=V_{SSO}=0V, STBYB=HALTB=SEL=2.5V, Load Impedance=32Ω, f_S=44.1kHz, unless otherwise noted)

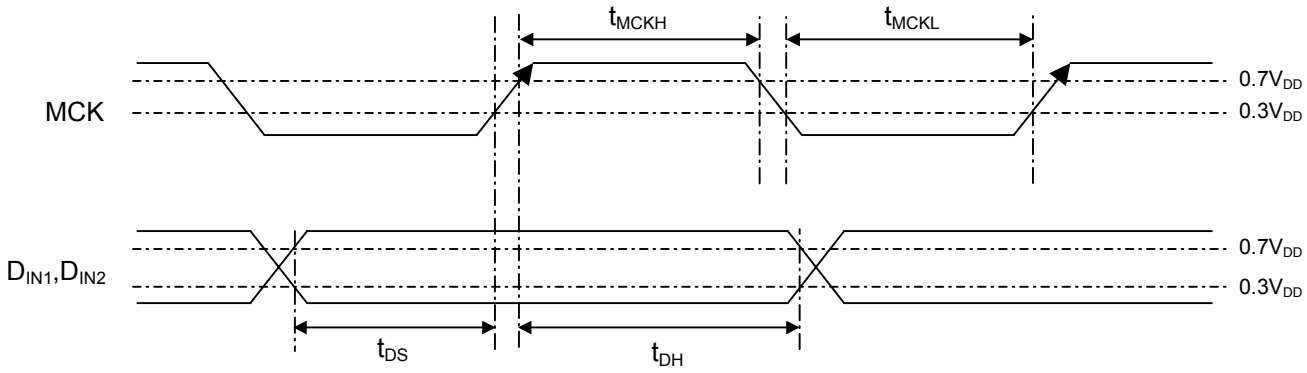
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} Supply Voltage	V_{DD}	-	1.7	2.5	2.7	V
$V_{DDO1,2}$ Input Voltage	V_{DDO}	-	0	-	2.0	
V_G Supply Voltage	V_G	-	4.5	5.0	5.25	
Output Driver High side Resistance	R_{HPH}	OUT_1, OUT_{1X}, OUT_2, OUT_{2X} = $V_{DDO1,2}$ – 0.1V V_G=5.0V	-	1.2	2	Ω
Output Driver Low side Resistance	R_{HPL}	OUT_1, OUT_{1X}, OUT_2, OUT_{2X} = 0.1V V_G= 5.0V	-	1.2	2	Ω
Beep High side Resistance	R_{BEEPH}	O_{BEEP1}, O_{BEEP2}= V_{DD}– 0.1V	-	9.0	15	Ω
Power Supply Current At Standby	I_{ST}	Stopping MCK, D_{IN1}, D_{IN2}, $BEEP_{IN}$ STBYB= 0V	-	-	1.0	uA
Power Supply Current At Operating (Mute signal input)	I_{DD}	No-load operating, MCK= 256f_S, D_{IN1}, D_{IN2}= 32f_S, V_{DDO1}= V_{DDO2}= 0.18V	-	0.05	0.1	mA
	I_{DDO}		-	0.25	0.5	
	I_G			1.0	2.0	
Input Voltage	V_{IH}	MCK, D_{IN1}, D_{IN2}, $BEEP_{IN}$, HALTB, STBYB, SEL	0.7V_{DD}	-	V_{DD}	V
	V_{IL}		0	-	0.3V_{DD}	V
Input Leakage Current	I_{LK}		-	-	±1.0	uA

Note 1) High side resistance and low side resistance depend on V_G and V_{DDO}. Therefore, V_G and V_{DDO} should be adjusted on the application system.

Note 2) Output power using 8Ω speaker is 150mW(TYP:THD+N=10%) at the following condition.
→V_{DD}=2.5V, V_G=5.0V, V_{DDO1}= V_{DDO2}=3.0V

■ TIMING CHARACTERISTICS

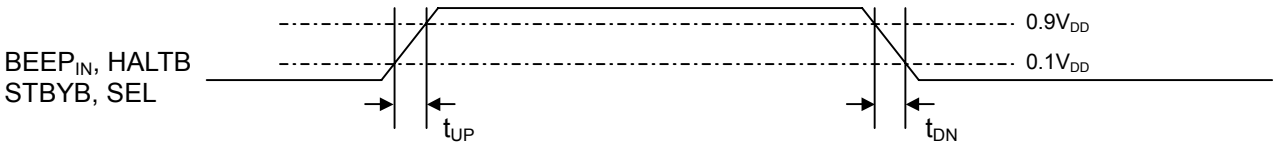
- Audio Signal Input



(Ta=25°C, V_{DD}=2.5V, V_{DDO1}=V_{DDO2}=1.7V, V_{SS}=V_{SSO}=0V,
STBYB=HALTB=SEL=2.5V, fs=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
MCK Frequency	f_{MCKI}		8	-	35	MHz
MCK Pulse Width (H)	t_{MCKH}		9	-	-	ns
MCK Pulse Width (L)	t_{MCKL}		9	-	-	ns
D_{IN1},D_{IN2} Setup Time	t_{DS}		5	-	-	ns
D_{IN1},D_{IN2} Hold Time	t_{DH}		5	-	-	ns
BEEP Frequency	f_b		0.1		20	kHz

- Output Control Signal Input

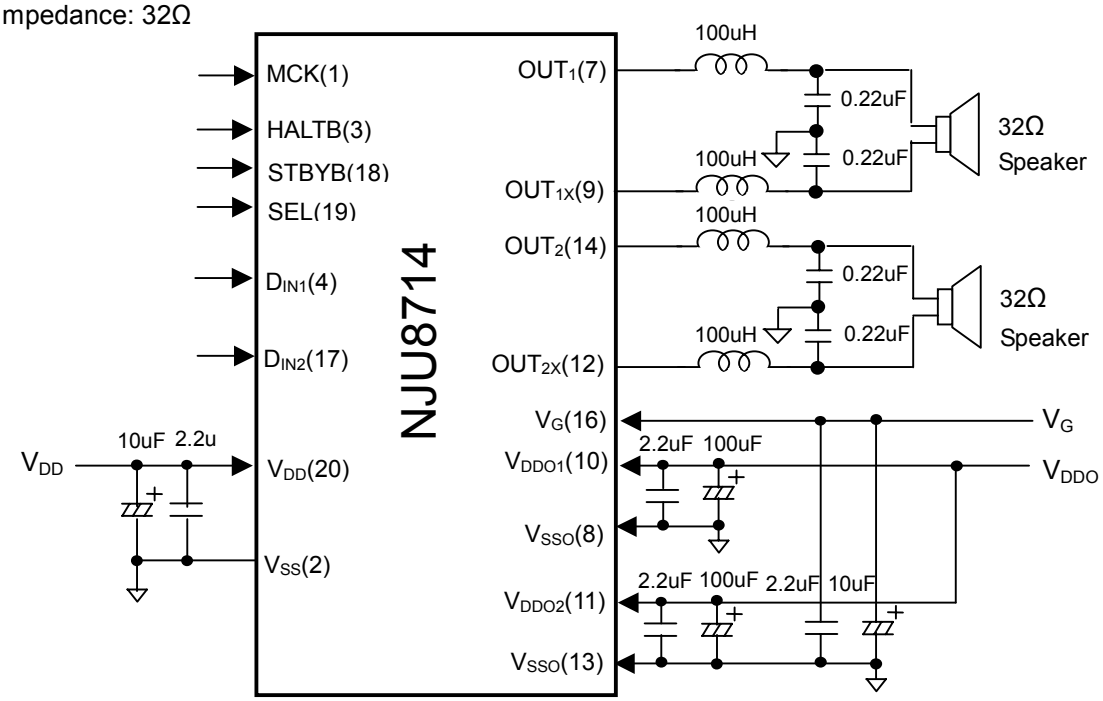


(Ta=25°C, V_{DD}=2.5V, V_{DDO1}=V_{DDO2}=1.7V, V_{SS}=V_{SSO}=0V,
STBYB=HALTB=SEL=2.5V, fs=44.1kHz, unless otherwise noted)

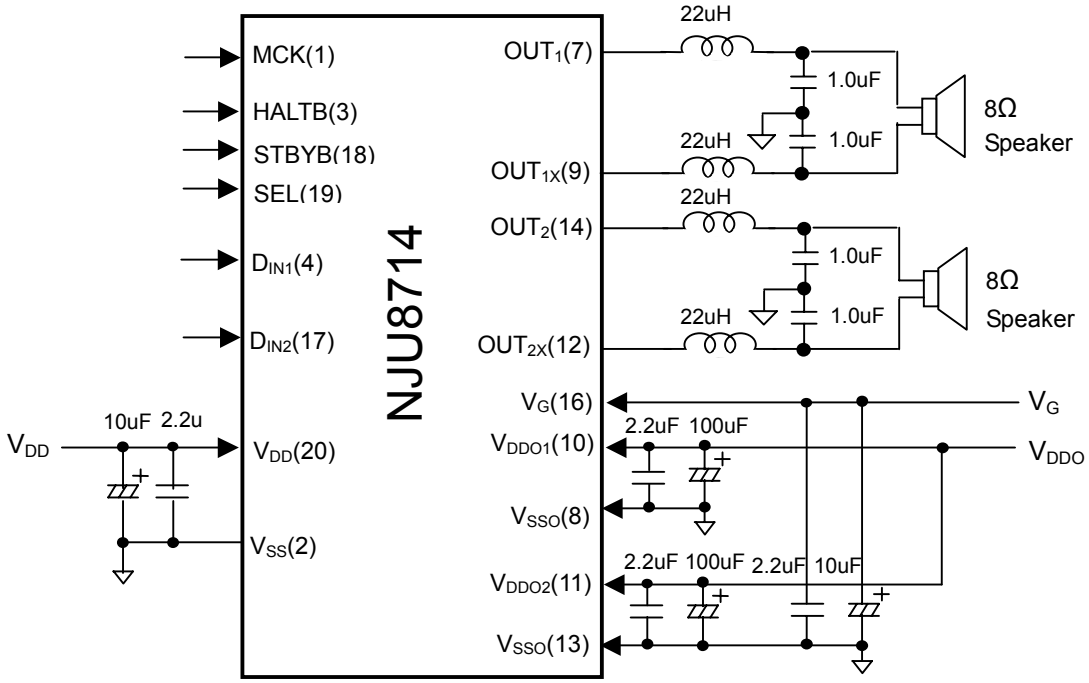
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Rise Time	t_{UP}		-	-	50	ns
Fall Time	t_{DN}		-	-	50	ns

■ APPLICATION CIRCUIT

-Load Impedance: 32Ω



-Load Impedance: 8Ω



Note 3) De-coupling capacitors must be connected between each power supply pin and GND pin.
Note 4) The power supply for V_{DDO} requires fast driving response performance such as a switching regulator for T.H.D..
Note 5) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please consider and check the circuit carefully to fit your application.

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