12-CHARACTER 1-LINE DOT MATRIX LCD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The NJU6467 is a Dot Matrix LCD controller driver for 12-character 1-line with icon display in single chip.

It contains CR oscillator, serial interface circuits, instruction decoder controller , character generator ROM/RAM, high voltage operation common and segment drivers.

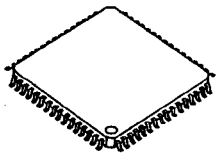
The CR oscillator incorporates C and R, therefore no external components for oscillation are required.

The serial interface circuits which operate by 1MHz, can be connected directly to serial port of the microprocessor.

The character generator consists of 7,680 bits ROM and 32 x 5 bits RAM.

The 17-common (16 for character, 1 for icon) and 30-segment drives up to 12-character 1-line , and the icon common driver display up to 24 icons.

■ PACKAGE OUTLINE

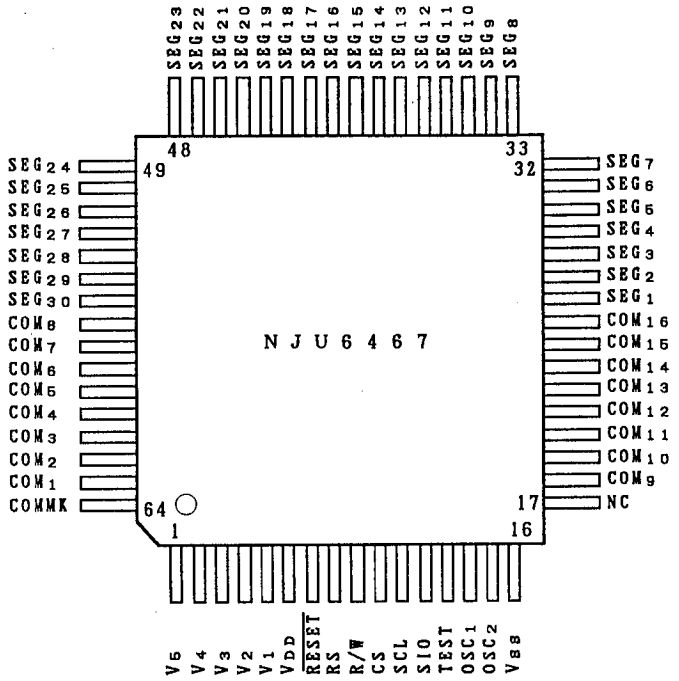


NJU6467F

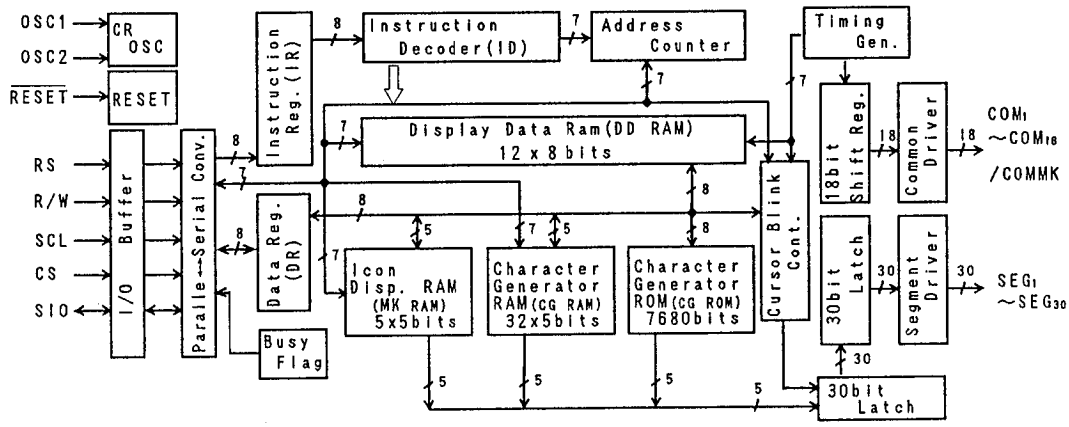
■ FEATURES

- 12-character 1-line Dot Matrix LCD Controller Driver
- Maximum 24 icon Display (Using COMMK)
- Serial Interface with Microprocessor
- Display Data RAM - 12 x 8 bits : Maximum 12-character 1-line Display
- Character Generator ROM - 7,680 bits : 192 Characters for 5 x 7 Dots
- Character Generator RAM - 32 x 5 bits : 4 Patterns(5 x 7 Dots)
- Icon Display RAM - 5 x 5 bits : 24 Icons
- High Voltage LCD Driver : 17-common / 30-segment
- Duty Ratio : 1/18 Duty
- Useful Instruction Set : Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift
- Power On Initialize / Hardware Reset Function
- Oscillation Circuit On-chip
- Low Power Consumption -- (50μA MAX.)
- Operating Voltage — 2.4 to 3.6 V (Except LCD Driving Voltage)
- Package Outline — QFP 64 / TQFP 64
- C-MOS Technology

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

PAD NO.	SYMBOL	F U N C T I O N
6	V_{DD}	Power Source (+ 3V)
16	V_{SS}	Power Source (0V)
1～5	V_5～V_1	LCD Driving Voltage Output
14 15	OSC_1 OSC_2	Oscillation Frequency Adjust Terminals. Normally open. (Oscillation C and R are incorporated, f_{OSC}=45kHz) For external clock operation, the clock should be input on OSC_1.
8	RS	Register Selection Signal Input (Pull-up Resistance On-chip) "0" : Instruction Register (Writing) Busy Flag, Address Counter (Reading) "1" : Data Register (Writing / Reading)
9	R/W	Read/Write Selection Signal Input (Pull-up Resistance On-chip) "0" : Write , "1" : Read
11	SCL	Shift Clock Input of Serial date transfer.
10	CS	Chip Select Signal Input of Serial date transfer.
12	SIO	Serial Data I/O of Serial date transfer.
56～63 18～25	COM_8～COM_1 COM_9～COM_{16}	LCD Common Driving Signal output terminals.
64	COMMK	Icon Display Common Driving Signal output terminals.
26～55	SEG_1～SEG_{30}	LCD Segment Driving Signal output terminals.
7	$\overline{RESET}$	Reset Terminal. When the "L" level input over than 1.2ms to this terminal, the system will be reset (f_{OSC}=45kHz).
13	TEST	Maker testing terminal. Normally Open.
17	NC	Non connect.

■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1−1) Register

The NJU6467 incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register(DR). The Register(IR) stores instruction codes such as "Clear Display" and "Return Home", and address data for Display Data RAM(DD RAM), Character Generator RAM(CG RAM) and Icon Display RAM(MK RAM).

The MPU can write the instruction code and address data to the Register(IR), but it cannot read out from the Register(IR).

The Register(DR) is a temporary stored register, the data stored in the Register(DR) is written into the DD RAM, CG RAM or MK RAM and read out from the DD RAM, CG RAM or MK RAM.

The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM, CG RAM or MK RAM by internal operation.

When the address data for the DD RAM, CG RAM or MK RAM is written into the Register(IR), the addressed data in the DD RAM, CG RAM or MK RAM is transferred to the Register(DR). By the MPU read out the data in the Register(DR), the data transmitting process is performed completely.

After reading the data in the Register(DR) by the MPU, the next address data in the DD RAM, CG RAM or MK RAM is transferred automatically to the Register(DR) to provide for the next MPU reading.

These two registers are selected by the selection signal RS as shown below.

Table 1. shows register operation controlled by RS and R/W signals.

5

Table 1. Register Operation

RS	R/W	Selected Register	Operation
0	0	IR	Write
0	1		Read busy flag(DB_7) and address counter(DB_0～DB_6)
1	0	DR	Write (Register(DR) to DD RAM, CG RAM or MK RAM)
1	1		Read (DD RAM, CG RAM or MK RAM to Register(DR))

(1−2) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag (BF) is "1", and any instruction reading is inhibited.

The busy flag (BF) is output at DB_7 when RS="0" and R/W="1" as shown in Table 1.

The next instruction should be written after the busy flag(BF) goes to "0".

(1−3) Address Counter (AC)

The address counter(AC) addressing the DD RAM, CG RAM and MK RAM.

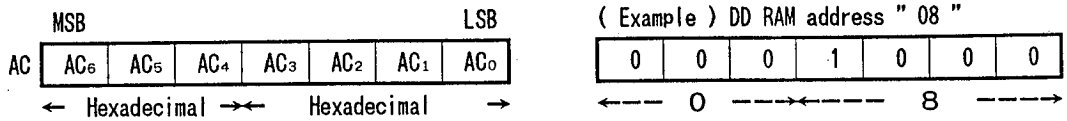
When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to Counter(AC). The selection of either the DD RAM, CG RAM or MK RAM is also determined by this instruction.

After writing (or reading) the display data to (or from) the DD RAM, CG RAM or MK RAM, the Counter (AC) increments (or decrements) automatically.

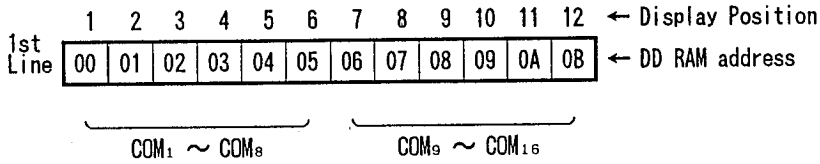
The address data in the Counter(AC) is output from DB_6～DB_0 when RS="0" and R/W="1" as shown in Table 1.

(1−4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 12 x 8 bits stores up to 12-character display data represented in 8-bit code.
The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.



The relation between DD RAM address and display position on the LCD is shown below.



When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

1	2	3	4	5	6	7	8	9	10	11	12
01	02	03	04	05	06	07	08	09	0A	0B	00

(Right Shift Display)

1	2	3	4	5	6	7	8	9	10	11	12
0B	00	01	02	03	04	05	06	07	08	09	0A

(1−5) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character codes.
The storage capacity is up to 192 kinds of 5 x 7 dots character pattern.
The correspondence between character code and standard character pattern of NJU6467 is shown in Table 2.
User-defined character patterns (Custom Font) are also available by mask option.

Table 2. CG ROM Character Pattern (ROM version -01)

Lower 4-bit (Hexadecimal) \ Upper 4-bit (Hexadecimal)	0	2	3	4	5	6	7	A	B	C	D	E	F
0	CG RAM (01)												
1	(02)												
2	(03)												
3	(04)												
4	(01)												
5	(02)												
6	(03)												
7	(04)												
8	(01)												
9	(02)												
A	(03)												
B	(04)												
C	(01)												
D	(02)												
E	(03)												
F	(04)												

Character code $(1X)_H$,$(8X)_H$,$(9X)_H$ don't exist.

(1－6) Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 5 x 7 dots written by the user program to display user's original character pattern and icon data. The CG RAM can store 4 kind of character in 5 x 7 dots mode or 2 kind of character in 5 x 7 dots mode and icon data.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ - $(03)_H$ should be written to the DD RAM as shown in Table 2.

Table 3. show the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(5 x 7 dots).

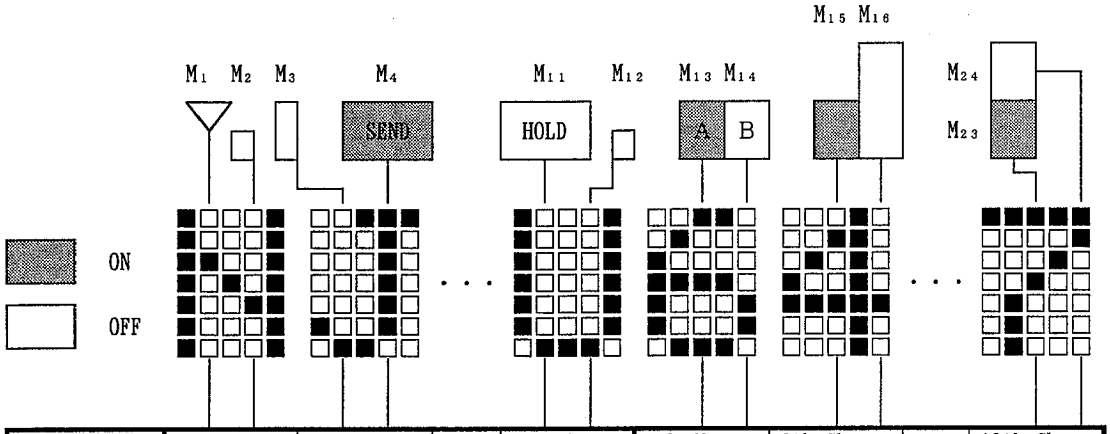
Character Code (DD RAM Data) 7 6 5 4 3 2 1 0 (Upperbit Lowerbit)	CG RAM Address 5 4 3 2 1 0 (Upper Lower)	Character Pattern (CG RAM Data) 7 6 5 4 3 2 1 0 (Upperbit Lowerbit)	
0 0 0 0 * 0 0 0	0 0 0 : 0 0 0	* * *	Character Pattern Example (1)
	0 0 1	↑	
	0 1 0	↓	
	0 1 1		
	1 0 0		
	1 0 1		
	1 1 0		
	1 1 1	* * *	←Cursor Position
0 0 0 0 * 0 0 1	0 0 1 : 0 0 0	* * *	Character Pattern Example (2)
	0 0 1	↑	
	0 1 0	↓	
	0 1 1		
	1 0 0		
	1 0 1		
	1 1 0		
	1 1 1	* * *	←Cursor Position
	0 0 0	* * *	
	0 0 1	↑	
⋮	⋮	⋮	* : Don't Care
0 0 0 0 * 1 1 1	1 1 1 : 0 1 1	↓	
	1 0 0		
	1 0 1		
	1 1 0		
	1 1 1	* * *	

Notes : 1. Character code bit 0, 1 correspond to the CG RAM address 3, 4(2bits:4 patterns).

2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and it is addressed by character code bits 0 and 1. Therefore, the address $(00)_H$, $(04)_H$, $(08)_H$ and $(0C)_H$ select the same character pattern as shown in Table 2.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1－7) Icon Display RAM (MK RAM)

The NJU6467 can display not only 5 x 7 bits character pattern but also maximum 24 icons.
The icon can be displayed by writing bit "1" to each data bit 0 to 4 in the address from $(60)_H$ to $(64)_H$ of MK RAM.
The icon display data is not affected except MK RAM writing and display ON/OFF instruction.
The relation between MK RAM address and icon display position on the LCD is fixed even if the display shift is executed. The relation is shown below:



Character		1st Chara	2nd Chara	· ·	6th Chara	7th Chara	8th Chara	· ·	12th Chara
SEG/display		1 2 3 4 5	6 7 8 9 10	· ·	2627282930	1 2 3 4 5	6 7 8 9 10	· ·	2627282930
MK RAM	data	0 0	0 1	· ·	0 0	1 0	1 0	· ·	1 0
	Add.	60_4 60_3	60_2 60_1		62_4 62_3	62_2 62_1	62_0 63_4		64_2 64_1

NOTE: The 60_4 corresponds bit 4 of $(60)_H$ in MK RAM.

Segment terminal number corresponding to the icon display position

	Segment Terminal No.
Above the 1st to 6th Character	2 4 7 9 12 14 17 19 22 24 27 29
Above the 7st to 12th Character	3 5 8 10 13 15 18 20 23 25 28 30

MK RAM address and data corresponding to the icon display position

MK RAM address	bits for icon display position							
	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
60_H	*	*	*	M_1	M_2	M_3	M_4	M_5
61_H	*	*	*	M_6	M_7	M_8	M_9	M_{10}
62_H	*	*	*	M_{11}	M_{12}	M_{13}	M_{14}	M_{15}
63_H	*	*	*	M_{16}	M_{17}	M_{18}	M_{19}	M_{20}
64_H	*	*	*	M_{21}	M_{22}	M_{23}	M_{24}	*

NOTE: When the icon display function using, the system should be initialized by the software initialization because of the MK RAM does not initialize except the software initialization.

(1−8) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, MK RAM and other internal circuits operation.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1−9) LCD Driver

LCD driver consist of 17-common driver and 30-segment driver.

When the line number is selected by a program, the required common drivers output the common driving waveform and the other common drivers output non-selection waveform automatically.

The 30 bits of character pattern data are shifted in the shift-register and latched when the 30 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1−10) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and the cursor position character blinks.

The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).

When the address counter is $(08)_H$, a cursor position is shown as follows:

	AC_4	AC_3	AC_2	AC_1	AC_0
(AC)	0	1	0	0	0

	1	2	3	4	5	6	7	8	9	10	11	12	← Display position
1-line Display	00	01	02	03	04	05	06	07	08	09	0A	0B	DD RAM address (Hexadecimal)

↑ Cursor position

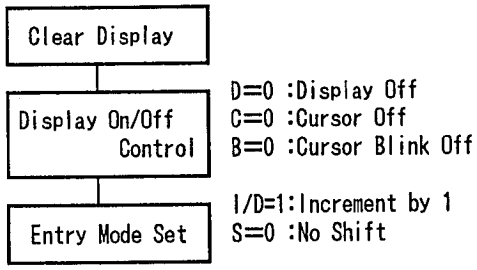
Note: The cursor or blinks also appear when the address counter (AC) selects the CG RAM. But the displayed cursor and blink are meaningless. If the AC storing the CG RAM address data, the cursor and blink are displayed in the meaningless position.

(2) Power on Initialization by internal circuits

(2−1) Initialization By Internal Reset Circuits

The NJU6467 is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 10 ms after V_{DD} rises to 2.4V.

Initialization flow is shown below:



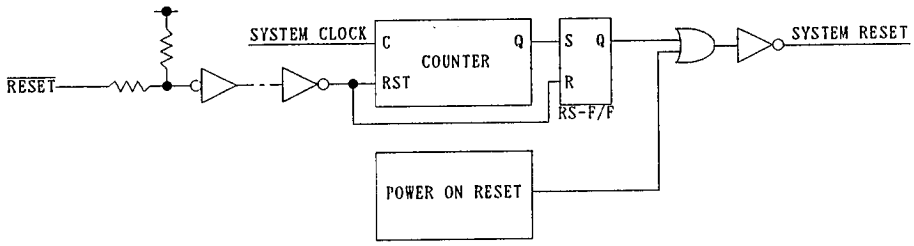
NOTE
If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operated and initialization will not performed.
In this case the initialization by MPU software is required.

(2−2) Initialization By Hardware

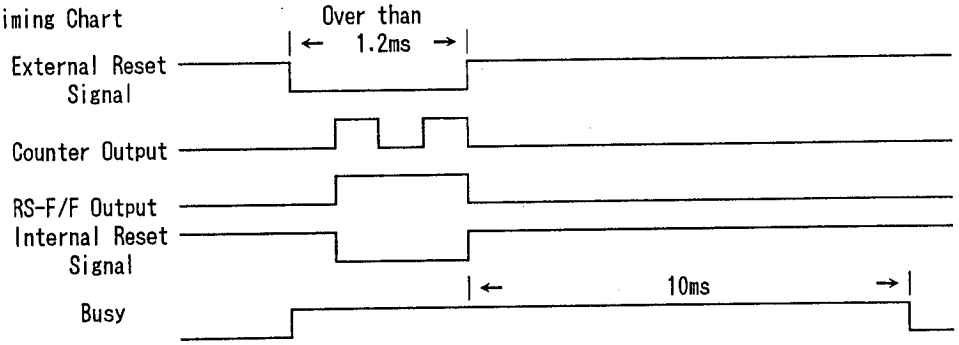
The NJU6467 incorporates $\overline{\text{RESET}}$ terminal to initialize the all system. When the "L" level input over than 1.2ms to the $\overline{\text{RESET}}$ terminal, reset sequence is executed. In this time, busy signal output during 10ms after $\overline{\text{RESET}}$ terminal goes to "H".

5

• Reset Circuit



• Timing Chart



(3) Instructions

The NJU6467 incorporates two registers, an Instruction Register (IR) and a Data Register(DR). These two registers store control information temporarily to allow interface between NJU6467 and MPU or peripheral ICs operating different cycles. The operation of NJU6467 is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data I/O signals (DB_0 to DB_7 by SIO terminal).

Table 4. Table of Instructions

INSTRUCTIONS	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DESCRIPTION	EXEC TIME
Maker Testing	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	-
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address 0 in AC.	2.89ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in AC and returns display being shifted to original position. DD RAM contents remain unchanged	223us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decrement S=1:Accompanies display shift	223us
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	223us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left	312us
Non Operation	0	0	0	0	1	*	*	*	*	*	Non operation.	-
	0	0	0	1	*	*	*	*	*	*		-
Set RAM Address	0	0	1	←—			Address			—→	Sets DD RAM, CG RAM and MK RAM address.	223us
Read Busy Flag & Address	0	1	BF	←—			AC			—→	Reads busy flag and AC contents. BF=1 : Internally operating BF=0 : Can accept instruction	0us
Write Data to CG & DD RAM	1	0	←— Write Data (DD RAM) —→								Writes data into DD, CG or MK RAMs	223us
	1	0	*	*	*	← Write Data (CG RAM) →						
	1	0	*	*	*	← Write Data (MK RAM) →						
Read Data from CG or DD RAM	1	1	←— Read Data (DD RAM) —→								Reads data from DD, CG or MK RAMs	312us
	1	1	*	*	*	← Read Data (CG RAM) →						
	1	1	*	*	*	← Read Data (MK RAM) →						
Explanation of Abbreviation	DD RAM : Display data RAM , CG RAM : Character generator RAM MK RAM : Icon Display RAM AC : Address counter used for both of DD, CG and MK RAMs											

* = Don't care

(3−1) Description of each instructions

(a) Maker Testing

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

All "0" code writing twice is using for device testing mode (only for maker). Therefore, please do not normally use this instruction.

(b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB_0. When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address 0 is set into the address counter and entry mode is set increment. If the cursor or blink are displayed, they are returned to the left end of the LCD. The S of entry mode does not change, the contents of CG RAM and MK RAM do not change either.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

5

(c) Return Home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	0	0	0	0	1	*	* = Don't care

Return home instruction is executed when the code "1" is written into DB_1. When this instruction is executed, the DD RAM address 0 is set into the address counter. Display is returned its original position if shifted, the cursor or blink are returned to the left end of the LCD, if the cursor or blink are on the display.
The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	Function
1	Address increment: The address of the DD RAM, CG RAM or MK RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD RAM, CG RAM or MK RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift. The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shifting.

(e) Display On/Off Control

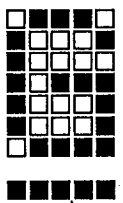
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

The Display On/Off control instruction which controls the whole display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB_0(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

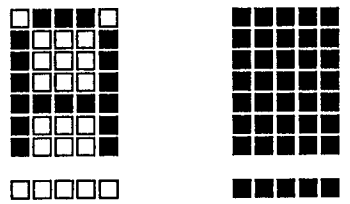
C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	Function
1	The cursor position character is blinking. Blinking rate is 540ms at f_{OSC}=45kHz for 12-character 1-line. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7 dots

(1) Cursor display example



Alternating display

(2) Blink display example

(f) Cursor/Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* = Don't care

Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display.

The contents of address counter(AC) does not change by operation of the display shift only.

This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3(S/C) and DB_2(R/L) as shown below.

S/C	R/L	Function
0	0	Shifts the cursor position to the left ((AC) is decremented by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

(g) Set RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	ADDRESS						

←Higher order bit Lower order bit→

Set RAM address instruction is set the address data written to DD RAM, CG RAM and MK RAM to the address counter (AC). After this instruction execution, the writing/reading is performed into/from the RAM written.

RAM Address

DD RAM	1st Line	:	from	$(00)_H$	to	$(0B)_H$
CG RAM	4 characters	:	from	$(40)_H$	to	$(5F)_H$
MK RAM	24 icons	:	from	$(60)_H$	to	$(64)_H$

(h) Read Busy Flag & Address

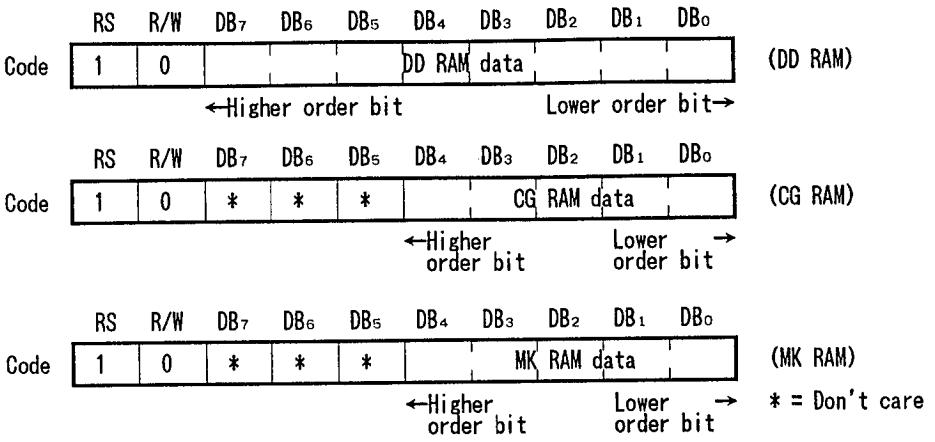
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A

←Higher order bit Lower order bit→

This instruction reads out the internal status of the NJU6467. When this instruction is executed, the busy flag (BF) which indicate internal operation is read out from DB_7 and the address of the CG RAM, DD RAM and MK RAM is read out from DB_6 to DB_0 (the address for the CG RAM, DD RAM or MK RAM is determined by the previous instruction).

(BF)="1" indicates that internal operation is in progress. The next instruction is inhibited when (BF)="1". Check the (BF) status before the next write operation.

(i) Write Data to DD RAM, CG RAM or MK RAM

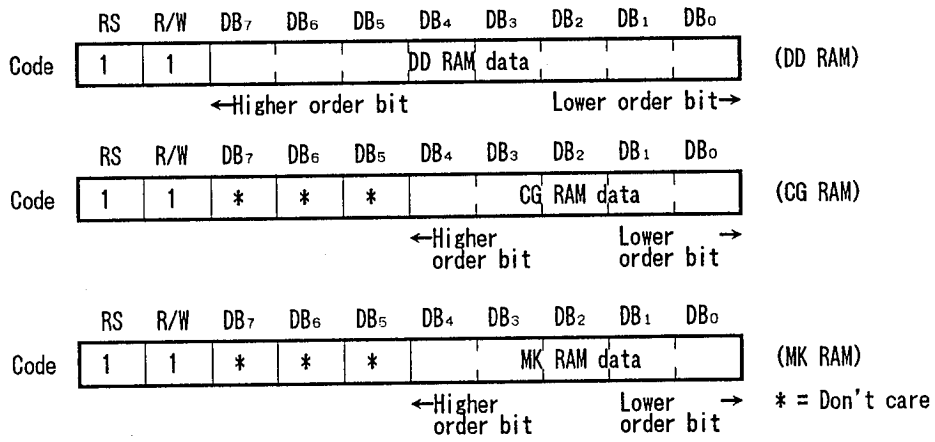


By the execution of this instruction, the RAM data of CG RAM, DD RAM or MK RAM is written into the CG RAM, DD RAM or MK RAM.

The selection of the RAM is determined by previous instruction (the RAM written must be selected before). After this instruction execution, the address increment (+1) or decrement (-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

5

(j) Read Data to DD RAM, CG RAM or MK RAM



The CG RAM, DD RAM or MK RAM is determined by previous instruction.

Before executing this instruction, either the CG RAM address set, DD RAM address or MK RAM set must be executed, otherwise the first read out data are invalidated.

When this instruction is serially executed, the next address data is normally read from the second read.

The address set instruction is not required if the cursor shift instruction is executed just beforehand (only DD RAM reading). The cursor shift instruction has same function as the DD RAM address set.

After reading the RAM, the address increment or decrement is executed automatically according to the entry mode. But display shift does not occur regardless of the entry mode.

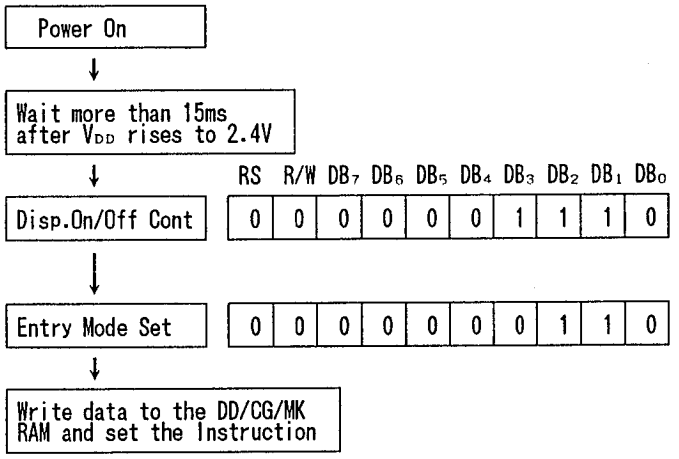
Note: The address counter(AC) is automatically incremented or decremented by 1 after write instruction to either of the DD RAM, CG RAM or MK RAM. Even if the read instruction is executed after this instruction, the addressed data can not be read out correctly. For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

(3−2) Initialization using the internal reset circuits

Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.

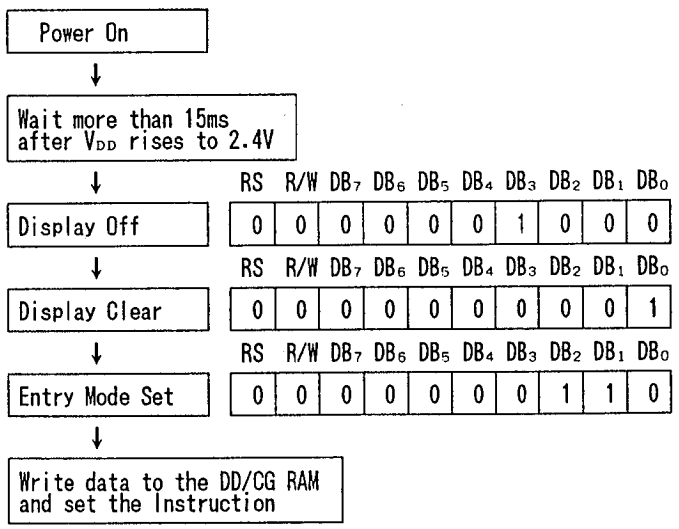
The DD RAM of the NJU6467 can store up to 12 characters, as explained before, therefore the advertising moving display is available when combined with the display shift operation.

Since the display shift operation changes only display position and the DD RAM contents remain unchanged, display data which are entered first can be output when the return home operation is performed.



(3−3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6467 must be initialized by the following routine.



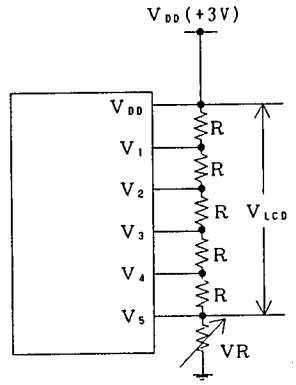
(4) LCD DISPLAY

(4−1) Power Supply for LCD Driving

In order to generate LCD driving waveform, the NJU6467 required external bleeder resistance. The bleeder resistance must be changed according to the duty ratio as shown below.

LCD Driving Voltage vs Duty Ratio

Power supply	Duty Ratio	1/16
	Bias	1/5
V_1		V_{DD} to $1/5V_{LCD}$
V_2		V_{DD} to $2/5V_{LCD}$
V_3		V_{DD} to $3/5V_{LCD}$
V_4		V_{DD} to $4/5V_{LCD}$
V_5		V_{DD} to V_{LCD}



(a) 1/5 Bias (1/18 Duty)

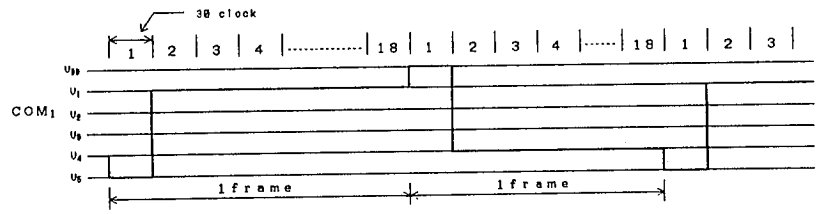
(4−2) Relation between oscillation frequency and LCD frame frequency.

As the NJU6467 incorporate oscillation capacitor and resistance for CR oscillation, 45kHz oscillation is available without any external components.

The LCD frame frequency example mentioned below is based on 45kHz oscillation.

(1 clock = 22.2us)

1/18 duty



1 frame = 22.2(us) x 30 x 18 = 12.0(ms)

Frame frequency = 1/12.0(ms) = 83.3(Hz)

(5) Serial Interface with MPU

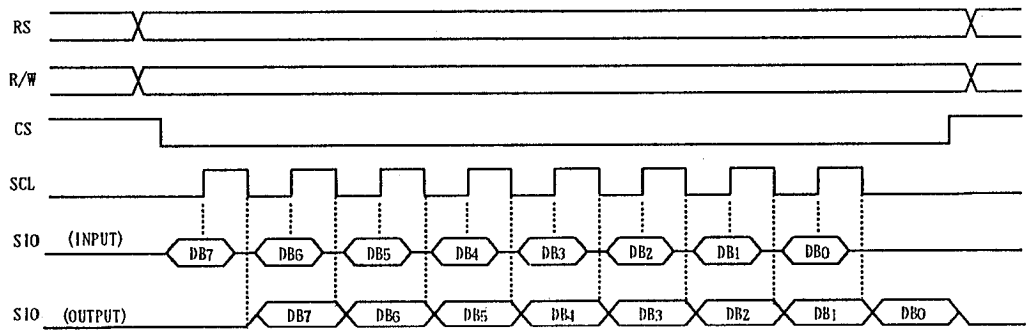
Serial interface circuit is activated when the chip select terminal (CS) goes to "L"level. The data input/output is MSB first like as the order of DB_7, DB_6 ···· DB_0.

The input data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The shift register converted to parallel data at the CS rise edge input. In case of entering over than 8-bit data, valid data is last 8-bit data.

The output data is exited from the shift register synchronized at the fall edge of the serial clock SCL.

The time chart for the serial interface is shown below.

Note : The level ("L" or "H") of RS and R/W terminals should be set before CS terminal goes to "L" level.



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	- 0.3 ～ + 7.0	V
Supply Voltage (2)	V_5	V_{DD}-13.5 ～ V_{DD}+0.3	V
Input Voltage	V_{IN}	- 0.3 ～ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ～ + 80	℃
Storage Temperature	Tstg	- 55 ～ + 125	℃

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) Decoupling capacitor should be connected between V_{DD} and V_{SS} , V_{DD} and V_5 due to the stabilized operation for the LSI.

Note 3) All voltage values are specified as V_{SS} = 0V

Note 4) The relation : $V_{DD} \geqq V_{SS}$, $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$, V_{SS}=0V must be maintained.
Turn on V_{DD} and V_5 at same time or turn on V_{DD} first then turn on V_5 must be required.
If the turn on sequence does not meet above conditions, latch up will occur.

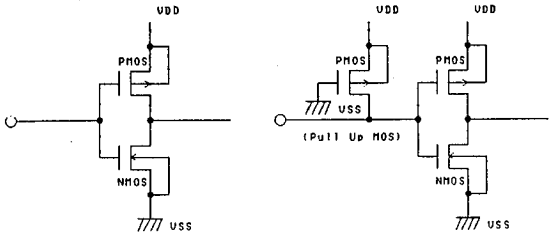
■ELECTRICAL CHARACTERISTICS

(V_{DD}=3V±20%, V_{SS}=0V, Ta=-20～+75℃)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage (1)	V_{DD}		2.4		3.6	V	
Operating Voltage (2)	V_5		V_{DD}-3.0		V_{DD}-13.5	V	
Input Voltage	V_{IH}		0.8V_{DD}		V_{DD}	V	5
	V_{IL}				0.2V_{DD}		
Output Voltage	V_{OH}	$-I_{OH}$=0.205mA	2.0			V	6
	V_{OL}	I_{OL}=1.6mA			0.5		
Driver On-resist.(COM)	R_{COM}	±I_d=10uA(All com.term.)			20	kΩ	9
Driver On-resist.(SEG)	R_{SEG}	±I_d=10uA(All seg.term.)			30		
Input Leakage Current	I_{LI}	V_{IN}=0 ～ V_{DD}	- 1		1	uA	7
Pull-up Resistance Current	$-I_P$	V_{DD}=3V	10	25	50	uA	
Operating Current	I_{DD}	V_{DD}=3V, f_{OSC}=Internal freq			50	uA	8
Oscillation Frequency	f_{OSC}	V_{DD}=3V, Ta=25℃	25	45	70	kHz	
Output Current	I_5	V_{DD}=V_{C1}=3V			50	uA	

Note 5) Input/Output structure except LCD driver are shown below:

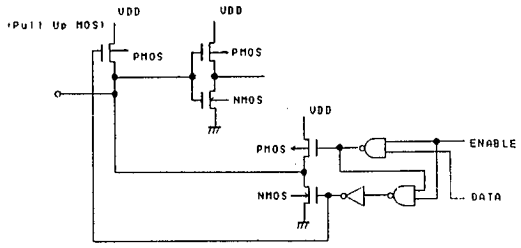
Input Terminal Structure



CS,SCL Terminals (No Pull-Up MOS)

RS,R/W,RESET Terminals (Pull-Up MOS)

Input/Output Terminal Structure



SIO Terminal

Note 6) Apply to the Output and Input/Output Terminal.

Note 7) Except pull-up MOS current and output driver current.

Note 8) Except Input/output current.
If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

Note 9) The relation : V_5=-10.5V, V_4=-7.8V, V_3=-5.1V, V_2=-2.4V, V_1=0.3V, V_{DD}=3.0

5

・Serial Interface Sequence

(V_{DD}=3V±20%, V_{SS}=0V, Ta=-20～+75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock Cycle Time		t_{CYCE}	1.3		fig.1	μs
Serial Clock Width	"High" level	t_{SCH}	0.3			μs
	"LOW" level	t_{SCL}	1.0			μs
Serial Clock rise and fall Time		t_{SCR}, t_{SCF}		20		ns
Chip Select Pulse Width		PW_{CS}	500			ns
Chip Select Setup Time		t_{CSU}	40			ns
Chip Select Hold Time		t_{CH}	60			ns
Chip Select rise and fall Time		t_{CSR}, t_{CSF}		20		ns
Setup Time	RS, R/W - CS	t_{AS}	60			ns
Address Hold Time		t_{AH}	20			ns
Serial Input Data Setup Time		t_{SISU}	60			ns
Serial Input Data Hold Time		t_{SIH}	40			ns
Serial Output Data Delay Time		t_{SOD}		950		ns
Serial Output Date Hold Time		t_{SOH}	0			ns

・SIO Load Condition : CL=100pF

Serial Interface Timing Characteristics

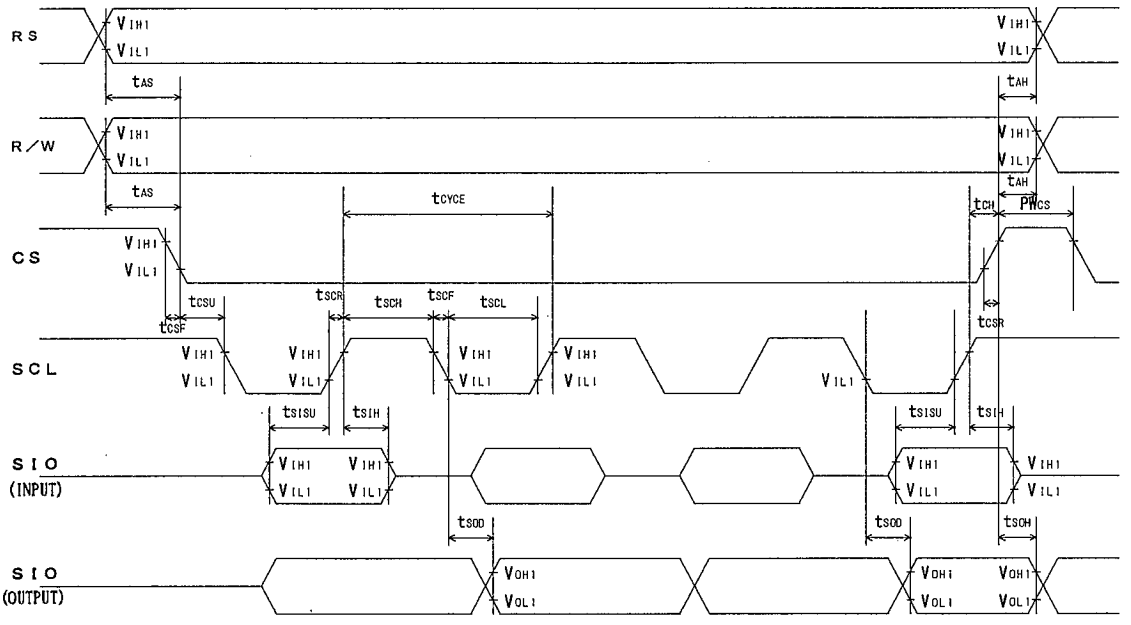
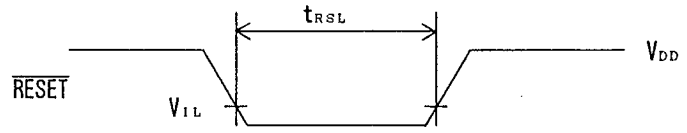


fig.1 The timing characteristics of the serial bus write/read operating sequence.

• The Input Condition when using the Hardware Reset Circuit

Input Timing

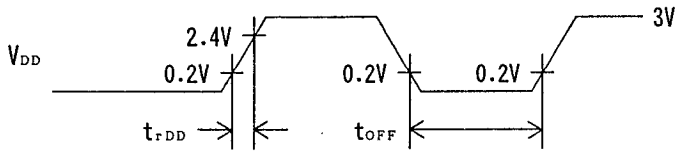


PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Reset Input "L" Level Width	t_{RSL}	f_{OSC}=45kHz	1.2	-	ms

• Power Supply Condition when using the internal initialization circuit(Ta=-20～+75℃)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Power Supply Rise Time	t_{rDD}		0.1	5	ms
Power Supply OFF Time	t_{OFF}		1		

Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction.
(Refer to initialization by the instruction)

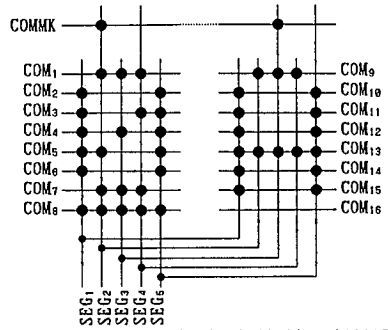


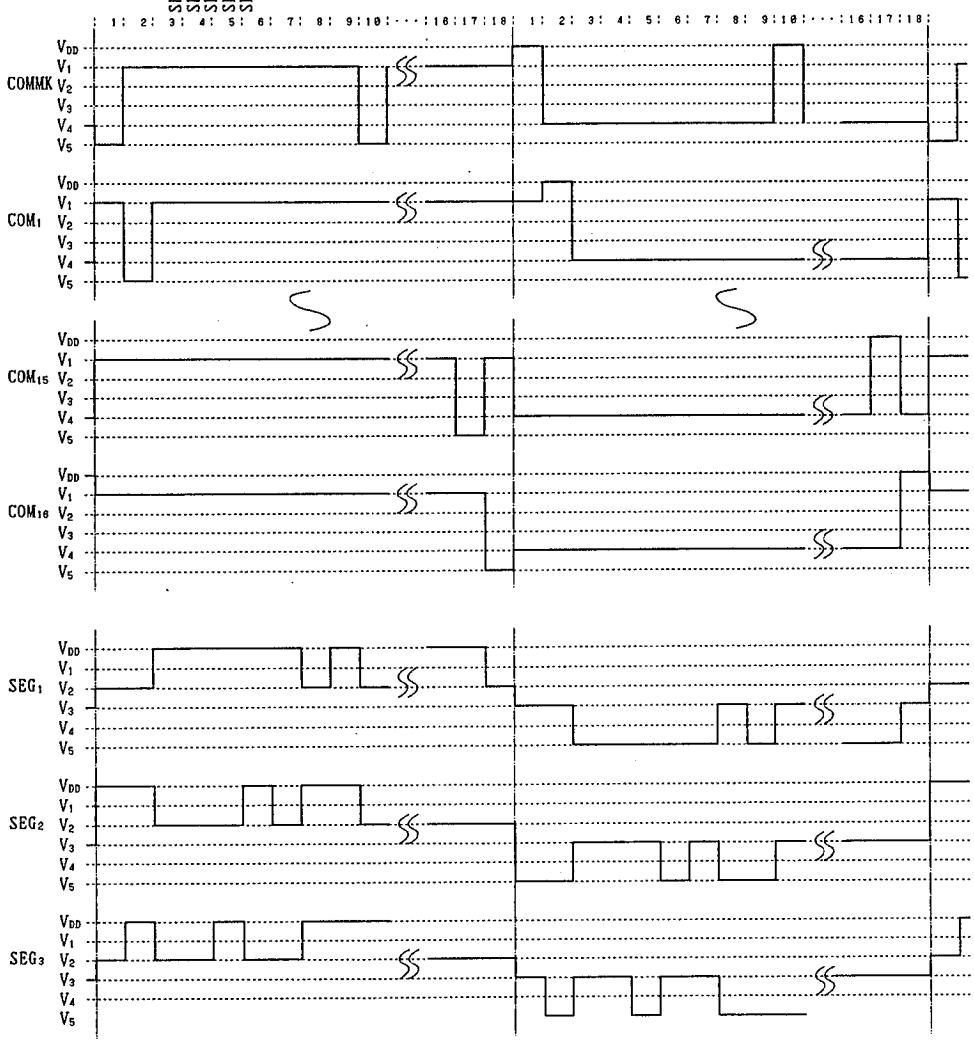
$0.1ms \leqq t_{rDD} \leqq 5ms$ $\quad t_{OFF} \geqq 1ms$

t_{OFF} specifies the power off time in a short period off or cyclical on/off.

■ LCD DRIVING WAVE FORM

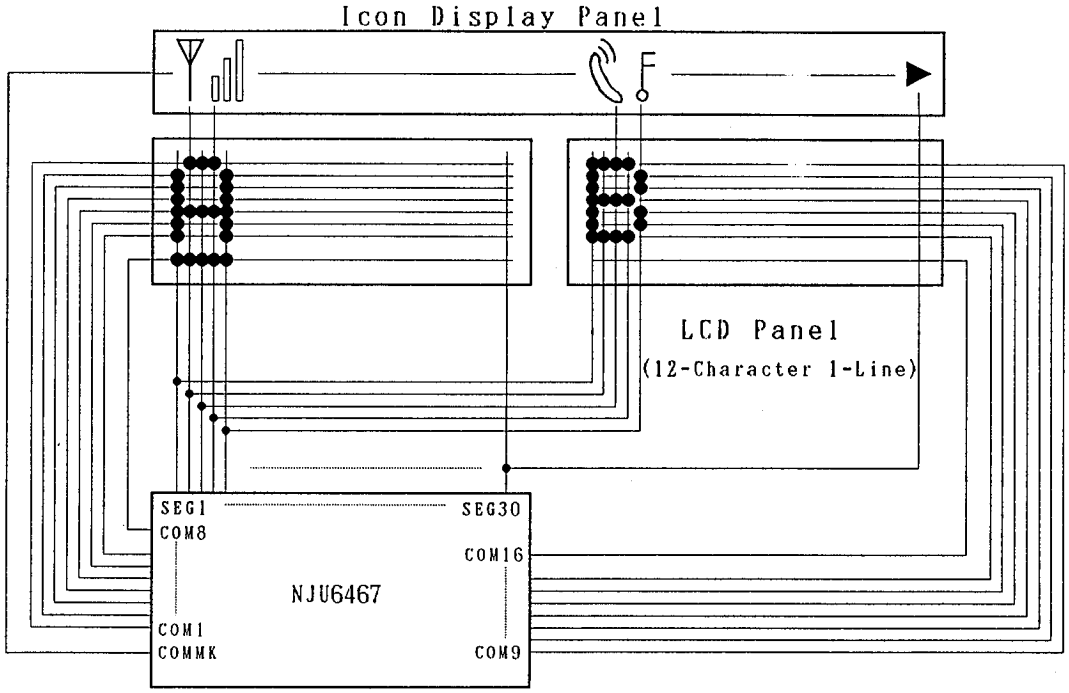
1/18 Duty Driving





■ APPLICATION CIRCUITS

12-Character 1-Line With Icon Display Example



MEMO