88-common x 132-segment
BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The **NJU6677** is a 88-common x 132-segment bit map LCD driver to display graphics or characters.
It contains 15,840 bits display data RAM, microprocessor interface circuits, instruction decoder, and common and segment drivers.
An image data from CPU through the serial or 8-bit parallel interface are stored into the 15,840 bits internal display data RAM and are displayed on the LCD panel through the commons and segments drivers.
The **NJU6677** displays 88 x 132 dots graphics or 8-character 5-line by 16 x 16 dots character.
The **NJU6677** contains a built-in OSC circuit for reducing external components. And it features Partial Display Function containing selectable active display block(s) (two blocks max.) and optimizing the duty cycle ratio. This function dramatically reduces the operating current, setting the optimum boosted voltage combined with a programmable voltage booster circuit and an electrical variable resister. As result, it reduces the operating current.
The operating voltage from 2.5V to 3.3V and low operating current are suitable for small size battery operation items.

■ PACKAGE OUTLINE

NJU6677CJ

■ FEATURES
- Direct Correspondence of Display Data RAM to LCD Pixel
- Display Data RAM - 15,840 bits ;(1.36 times over than display size)
- LCD drivers - 88-common and 132-segment
- Direct connection to 8-bit Microprocessor interface for both of 68 and 80 type MPU
- Serial Interface
- Partial Display Function   Two limited active display blocks setting. Duty ratio set automatically.
- Easy Vertical Scroll by setting the start line address of over size display data RAM
- Programmable Bias selection ; 1/4,1/5,1/6,1/7,1/8,1/9,1/10 bias
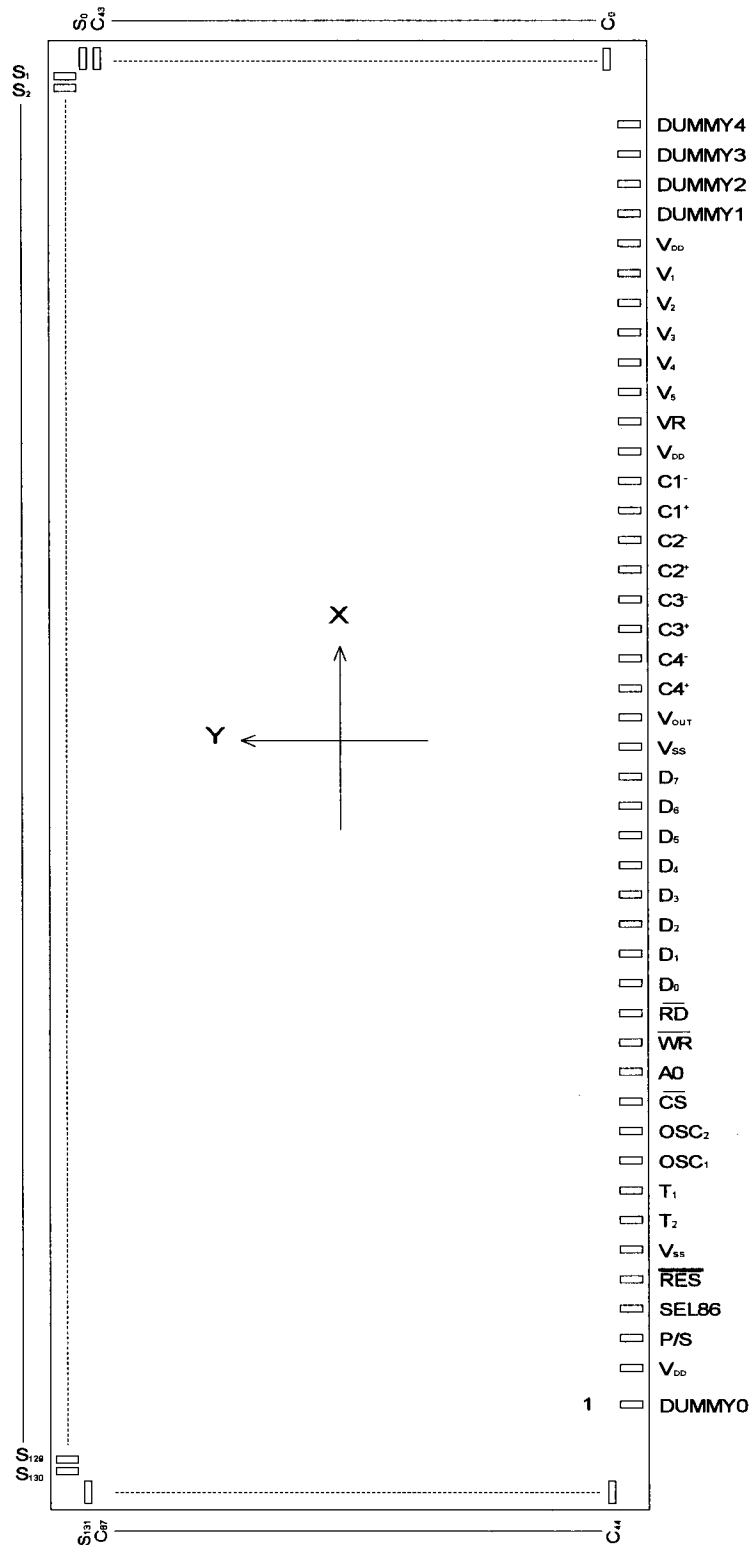- Common Driver Order Assignment by mask option

Version	C_0 to C_{87}(Pin name)
NJU6677A	Com_0 to Com_{87}
NJU6677B	Com_{87} to Com_0

- Useful Instruction Sets
  Display ON/OFF Cont, Display Start Line Set, Page Address Set, Column Address Set, Status Read, Display Data Read/Write, Inverse Display, All On/Off, Partial Display, Bias Select, n-Line Inverse, Voltage Booster Circuits Multiple Select(Maximum 5-time), Read Modify Write, Power Saving, ADC Select, etc.
- Power Supply Circuits for LCD; Programmable Voltage Booster Circuits(5-time Maximum, Voltage boosting polarity:Negative voltage(V_{DD} Common)),Regulator, Voltage Follower (x 4)
- Precision Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage   --- 2.5V to 3.3V
- LCD Driving Voltage   --- 6.0V to 18V
- Package Outline   --- Bumped Chip
- C-MOS Technology (Substrate:N)

■ PAD LOCATION

Pin labels (top to bottom, right side):

- DUMMY4
- DUMMY3
- DUMMY2
- DUMMY1
- V_{DD}
- V_1
- V_2
- V_3
- V_4
- V_5
- VR
- V_{DD}
- C1⁻
- C1⁺
- C2⁻
- C2⁺
- C3⁻
- C3⁺
- C4⁻
- C4⁺
- V_{OUT}
- V_{SS}
- D_7
- D_6
- D_5
- D_4
- D_3
- D_2
- D_1
- D_0
- $\overline{RD}$
- $\overline{WR}$
- A0
- $\overline{CS}$
- OSC_2
- OSC_1
- T_1
- T_2
- V_{SS}
- $\overline{RES}$
- SEL86
- P/S
- V_{DD}
- DUMMY0   (1)

Left side labels: S_0 C_{43}, S_1, S_2, C_0 (top), S_{129}, S_{130}, S_{131} C_{87}, C_{44} (bottom)

X / Y axis indicator at chip center

Chip Center	: X=0um, Y=0um
Chip Size	: X=8.31mm, Y=2.93mm
Chip Thickness	: 675um ± 30um
Bump Size	: 45um x 83um
Pad pitch	: 60um(Min)
Bump Height	: 17.5um TYP.
Bump Material	: Au
Voltage boosting polarity	:Negative voltage (VDD Common)
Substrate	:N

■TERMINAL DESCRIPTION

Chip Size 8.31 x 2.93mm (Chip Center X=0um,Y=0um)

PAD No.	Terminal	X= um	Y= um	PAD No.	Terminal	X= um	Y= um
1	DUMMY0	-3884.0	-1305.0	51	C_6	3995.0	-958.1
2	V_{DD}	-3179.2	-1305.0	52	C_7	3995.0	-898.1
3	P/S	-3014.1	-1305.0	53	C_8	3995.0	-838.1
4	SEL68	-2793.7	-1305.0	54	C_9	3995.0	-778.1
5	$\overline{RES}$	-2557.3	-1305.0	55	C_{10}	3995.0	-718.1
6	V_{SS}	-2400.1	-1305.0	56	C_{11}	3995.0	-658.1
7	T_2	-2242.9	-1305.0	57	C_{12}	3995.0	-598.1
8	T_1	-2007.3	-1305.0	58	C_{13}	3995.0	-538.1
9	OSC_1	-1786.9	-1305.0	59	C_{14}	3995.0	-478.1
10	OSC_2	-1550.5	-1305.0	60	C_{15}	3995.0	-418.1
11	$\overline{CS}$	-1330.1	-1305.0	61	C_{16}	3995.0	-358.1
12	A0	-1093.7	-1305.0	62	C_{17}	3995.0	-298.1
13	$\overline{WR}$	-873.3	-1305.0	63	C_{18}	3995.0	-238.1
14	$\overline{RD}$	-636.9	-1305.0	64	C_{19}	3995.0	-178.1
15	D_0	-400.2	-1305.0	65	C_{20}	3995.0	-118.1
16	D_1	-179.8	-1305.0	66	C_{21}	3995.0	-58.1
17	D_2	40.6	-1305.0	67	C_{22}	3995.0	1.9
18	D_3	261.0	-1305.0	68	C_{23}	3995.0	61.9
19	D_4	481.4	-1305.0	69	C_{24}	3995.0	121.9
20	D_5	701.8	-1305.0	70	C_{25}	3995.0	181.9
21	$D_6(SCL)$	922.2	-1305.0	71	C_{26}	3995.0	241.9
22	$D_7(SI)$	1142.6	-1305.0	72	C_{27}	3995.0	301.9
23	V_{SS}	1300.1	-1305.0	73	C_{28}	3995.0	361.9
24	V_{OUT}	1370.1	-1305.0	74	C_{29}	3995.0	421.9
25	C_4^+	1466.0	-1305.0	75	C_{30}	3995.0	481.9
26	C_4^-	1614.8	-1305.0	76	C_{31}	3995.0	541.9
27	C_3^+	1674.8	-1305.0	77	C_{32}	3995.0	601.9
28	C_3^-	1823.6	-1305.0	78	C_{33}	3995.0	661.9
29	C_2^+	1883.6	-1305.0	79	C_{34}	3995.0	721.9
30	C_2^-	2032.4	-1305.0	80	C_{35}	3995.0	781.9
31	C_1^+	2092.4	-1305.0	81	C_{36}	3995.0	841.9
32	C_1^-	2241.2	-1305.0	82	C_{37}	3995.0	901.9
33	V_{DD}	2311.2	-1305.0	83	C_{38}	3995.0	961.9
34	VR	2491.2	-1305.0	84	C_{39}	3995.0	1021.9
35	V_5	2561.2	-1305.0	85	C_{40}	3995.0	1081.9
36	V_4	2631.2	-1305.0	86	C_{41}	3995.0	1141.9
37	V_3	2701.2	-1305.0	87	C_{42}	3995.0	1201.9
38	V_2	2771.2	-1305.0	88	C_{43}	3995.0	1261.9
39	V_1	2841.2	-1305.0	89	S_0	3995.0	1321.9
40	V_{DD}	2911.2	-1305.0	90	S_1	3870.0	1305.0
41	DUMMY1	3119.2	-1305.0	91	S_2	3810.0	1305.0
42	DUMMY2	3179.2	-1305.0	92	S_3	3750.0	1305.0
43	DUMMY3	3239.2	-1305.0	93	S_4	3690.0	1305.0
44	DUMMY4	3884.0	-1305.0	94	S_5	3630.0	1305.0
45	C_0	3995.0	-1318.1	95	S_6	3570.0	1305.0
46	C_1	3995.0	-1258.1	96	S_7	3510.0	1305.0
47	C_2	3995.0	-1198.1	97	S_8	3450.0	1305.0
48	C_3	3995.0	-1138.1	98	S_9	3390.0	1305.0
49	C_4	3995.0	-1078.1	99	S_{10}	3330.0	1305.0
50	C_5	3995.0	-1018.1	100	S_{11}	3270.0	1305.0

PAD No.	Terminal	X= um	Y= um	PAD No.	Terminal	X= um	Y= um
101	S_{12}	3210.0	1305.0	151	S_{62}	210.0	1305.0
102	S_{13}	3150.0	1305.0	152	S_{63}	150.0	1305.0
103	S_{14}	3090.0	1305.0	153	S_{64}	90.0	1305.0
104	S_{15}	3030.0	1305.0	154	S_{65}	30.0	1305.0
105	S_{16}	2970.0	1305.0	155	S_{66}	-30.0	1305.0
106	S_{17}	2910.0	1305.0	156	S_{67}	-90.0	1305.0
107	S_{18}	2850.0	1305.0	157	S_{68}	-150.0	1305.0
108	S_{19}	2790.0	1305.0	158	S_{69}	-210.0	1305.0
109	S_{20}	2730.0	1305.0	159	S_{70}	-270.0	1305.0
110	S_{21}	2670.0	1305.0	160	S_{71}	-330.0	1305.0
111	S_{22}	2610.0	1305.0	161	S_{72}	-390.0	1305.0
112	S_{23}	2550.0	1305.0	162	S_{73}	-450.0	1305.0
113	S_{24}	2490.0	1305.0	163	S_{74}	-510.0	1305.0
114	S_{25}	2430.0	1305.0	164	S_{75}	-570.0	1305.0
115	S_{26}	2370.0	1305.0	165	S_{76}	-630.0	1305.0
116	S_{27}	2310.0	1305.0	166	S_{77}	-690.0	1305.0
117	S_{28}	2250.0	1305.0	167	S_{78}	-750.0	1305.0
118	S_{29}	2190.0	1305.0	168	S_{79}	-810.0	1305.0
119	S_{30}	2130.0	1305.0	169	S_{80}	-870.0	1305.0
120	S_{31}	2070.0	1305.0	170	S_{81}	-930.0	1305.0
121	S_{32}	2010.0	1305.0	171	S_{82}	-990.0	1305.0
122	S_{33}	1950.0	1305.0	172	S_{83}	-1050.0	1305.0
123	S_{34}	1890.0	1305.0	173	S_{84}	-1110.0	1305.0
124	S_{35}	1830.0	1305.0	174	S_{85}	-1170.0	1305.0
125	S_{36}	1770.0	1305.0	175	S_{86}	-1230.0	1305.0
126	S_{37}	1710.0	1305.0	176	S_{87}	-1290.0	1305.0
127	S_{38}	1650.0	1305.0	177	S_{88}	-1350.0	1305.0
128	S_{39}	1590.0	1305.0	178	S_{89}	-1410.0	1305.0
129	S_{40}	1530.0	1305.0	179	S_{90}	-1470.0	1305.0
130	S_{41}	1470.0	1305.0	180	S_{91}	-1530.0	1305.0
131	S_{42}	1410.0	1305.0	181	S_{92}	-1590.0	1305.0
132	S_{43}	1350.0	1305.0	182	S_{93}	-1650.0	1305.0
133	S_{44}	1290.0	1305.0	183	S_{94}	-1710.0	1305.0
134	S_{45}	1230.0	1305.0	184	S_{95}	-1770.0	1305.0
135	S_{46}	1170.0	1305.0	185	S_{96}	-1830.0	1305.0
136	S_{47}	1110.0	1305.0	186	S_{97}	-1890.0	1305.0
137	S_{48}	1050.0	1305.0	187	S_{98}	-1950.0	1305.0
138	S_{49}	990.0	1305.0	188	S_{99}	-2010.0	1305.0
139	S_{50}	930.0	1305.0	189	S_{100}	-2070.0	1305.0
140	S_{51}	870.0	1305.0	190	S_{101}	-2130.0	1305.0
141	S_{52}	810.0	1305.0	191	S_{102}	-2190.0	1305.0
142	S_{53}	750.0	1305.0	192	S_{103}	-2250.0	1305.0
143	S_{54}	690.0	1305.0	193	S_{104}	-2310.0	1305.0
144	S_{55}	630.0	1305.0	194	S_{105}	-2370.0	1305.0
145	S_{56}	570.0	1305.0	195	S_{106}	-2430.0	1305.0
146	S_{57}	510.0	1305.0	196	S_{107}	-2490.0	1305.0
147	S_{58}	450.0	1305.0	197	S_{108}	-2550.0	1305.0
148	S_{59}	390.0	1305.0	198	S_{109}	-2610.0	1305.0
149	S_{60}	330.0	1305.0	199	S_{110}	-2670.0	1305.0
150	S_{61}	270.0	1305.0	200	S_{111}	-2730.0	1305.0

PAD No.	Terminal	X= um	Y= um
201	S_{112}	-2790.0	1305.0
202	S_{113}	-2850.0	1305.0
203	S_{114}	-2910.0	1305.0
204	S_{115}	-2970.0	1305.0
205	S_{116}	-3030.0	1305.0
206	S_{117}	-3090.0	1305.0
207	S_{118}	-3150.0	1305.0
208	S_{119}	-3210.0	1305.0
209	S_{120}	-3270.0	1305.0
210	S_{121}	-3330.0	1305.0
211	S_{122}	-3390.0	1305.0
212	S_{123}	-3450.0	1305.0
213	S_{124}	-3510.0	1305.0
214	S_{125}	-3570.0	1305.0
215	S_{126}	-3630.0	1305.0
216	S_{127}	-3690.0	1305.0
217	S_{128}	-3750.0	1305.0
218	S_{129}	-3810.0	1305.0
219	S_{130}	-3870.0	1305.0
220	S_{131}	-3995.0	1321.9
221	C_{87}	-3995.0	1261.9
222	C_{86}	-3995.0	1201.9
223	C_{85}	-3995.0	1141.9
224	C_{84}	-3995.0	1081.9
225	C_{83}	-3995.0	1021.9
226	C_{82}	-3995.0	961.9
227	C_{81}	-3995.0	901.9
228	C_{80}	-3995.0	841.9
229	C_{79}	-3995.0	781.9
230	C_{78}	-3995.0	721.9
231	C_{77}	-3995.0	661.9
232	C_{76}	-3995.0	601.9
233	C_{75}	-3995.0	541.9
234	C_{74}	-3995.0	481.9
235	C_{73}	-3995.0	421.9
236	C_{72}	-3995.0	361.9
237	C_{71}	-3995.0	301.9
238	C_{70}	-3995.0	241.9
239	C_{69}	-3995.0	181.9
240	C_{68}	-3995.0	121.9
241	C_{67}	-3995.0	61.9
242	C_{66}	-3995.0	1.9
243	C_{65}	-3995.0	-58.1
244	C_{64}	-3995.0	-118.1
245	C_{63}	-3995.0	-178.1
246	C_{62}	-3995.0	-238.1
247	C_{61}	-3995.0	-298.1
248	C_{60}	-3995.0	-358.1
249	C_{59}	-3995.0	-418.1
250	C_{58}	-3995.0	-478.1

PAD No.	Terminal	X= um	Y= um
251	C_{57}	-3995.0	-538.1
252	C_{56}	-3995.0	-598.1
253	C_{55}	-3995.0	-658.1
254	C_{54}	-3995.0	-718.1
255	C_{53}	-3995.0	-778.1
256	C_{52}	-3995.0	-838.1
257	C_{51}	-3995.0	-898.1
258	C_{50}	-3995.0	-958.1
259	C_{49}	-3995.0	-1018.1
260	C_{48}	-3995.0	-1078.1
261	C_{47}	-3995.0	-1138.1
262	C_{46}	-3995.0	-1198.1
263	C_{45}	-3995.0	-1258.1
264	C_{44}	-3995.0	-1318.1

■ BLOCK DIAGRAM
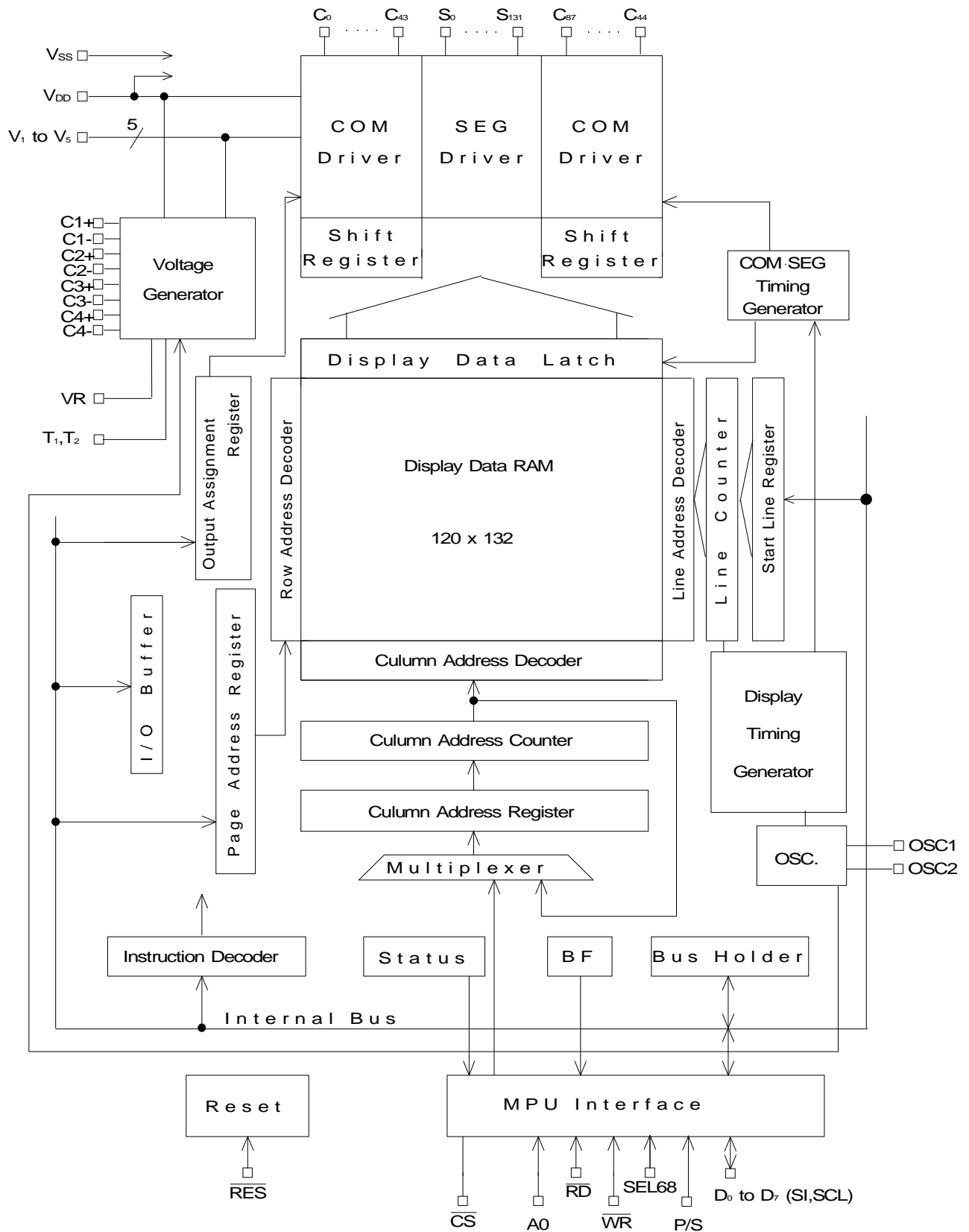
■ TERMINAL DESCRIPTION

No.	Symbol	I/O	Function
1,41 to 44	DUMMY0 to DUMMY5		Dummy Terminals. These are open terminals electrically.
2,33,40	V_{DD}	Power	Power Supply Terminal (+2.4V - +3.6V)
6,23	V_{SS}	GND	Ground Terminal (0V)
39 38 37 36 35	V_1 V_2 V_3 V_4 V_5	Power	LCD Driving Voltage Supplying Terminals. In case of the external power supply operation without internal power supply operation, each level of LCD driving voltage is supplied from outside fitting with following relation. $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_{OUT}$ In case of the internal power supply, LCD driving voltages V1-V4 depending on the Bias selection are supplied as shown in follows; (see table below)

Bias	V1	V2	V3	V4
1/4Bias	$V_5+3/4V_{LCD}$	$V_5+2/4V_{LCD}$	$V_5+2/4V_{LCD}$	$V_5+1/4V_{LCD}$
1/5Bias	$V_5+4/5V_{LCD}$	$V_5+3/5V_{LCD}$	$V_5+2/5V_{LCD}$	$V_5+1/5V_{LCD}$
1/6Bias	$V_5+5/6V_{LCD}$	$V_5+4/6V_{LCD}$	$V_5+2/6V_{LCD}$	$V_5+1/6V_{LCD}$
1/7Bias	$V_5+6/7V_{LCD}$	$V_5+5/7V_{LCD}$	$V_5+2/7V_{LCD}$	$V_5+1/7V_{LCD}$
1/8Bias	$V_5+7/8V_{LCD}$	$V_5+6/8V_{LCD}$	$V_5+2/8V_{LCD}$	$V_5+1/8V_{LCD}$
1/9Bias	$V_5+8/9V_{LCD}$	$V_5+7/9V_{LCD}$	$V_5+2/9V_{LCD}$	$V_5+1/9V_{LCD}$
1/10Bias	$V_5+9/10V_{LCD}$	$V_5+8/10V_{LCD}$	$V_5+2/10V_{LCD}$	$V_5+1/10V_{LCD}$

($V_{LCD}=V_{DD}-V_5$)

No.	Symbol	I/O	Function
31,32 29,30 27,28 25,26	$C1^+,C1^-$ $C2^+,C2^-$ $C3^+,C3^-$ $C4^+,C4^-$	O	Capacitor connecting terminals for Internal Voltage Booster. Boosting time is programmed by instruction (2 to 5 times)
24	V_{OUT}	O	Boosted voltage output terminal. Connects the capacitor between V_{OUT} terminal and V_{SS}.
34	VR	I	V_{LCD} voltage adjustment terminal. The gain of V_{LCD} setup circuit for V5 level is adjusted by external resistors.
8 7	T_1 T_2	I	LCD bias voltage control terminals. (see table below)

T_1	T_2	Voltage booster Cir.	Voltage Adj.	V/F Cir.
L	L/H	Available	Available	Available
H	L	Not Avail.	Available	Available
H	H	Not Avail.	Not Avail.	Available

No.	Symbol	I/O	Function
15 to 22	D0 to D7 (SI) (SCL)	I/O	Data Input/Output terminals. In Pararel Interface Mode (P/S="H") I/O terminals of 8-bit bus. In Serial Interface Mode (P/S="L") D7: Input terminal of serial data (SI). D6: Input terminal of serial data clock (SCL). D0 to D5 terminals are Hi-impedance. When $\overline{CS}$="H", D0 to D7 terminals are Hi-impedance.
12	A0	I	Data discremination signal input terminal. The signal from MPU discreminates transmoitted data between Display data and Instruction. (see table below)

A0	H	L
Distin.	Display Data	Instruction

No.	Symbol	I/O	Function
5	$\overline{RES}$	I	Reset terminal. Reset operation is executing during "L" state of $\overline{RES}$.
11	$\overline{CS}$	I	Chip select signal input terminal. Data Input/Output are available during $\overline{CS}$ ="L".

No	Symbol	I/O	Function

14	$\overline{RD}(E)$	I	RD(80 type) or E(68 type) signal input terminal.
			<In 80 type MPU mode >(SEL68="L")
			  $\overline{RD}$ signal from 80 type MPU input terminal. Active "L".
			  D_0 to D_7 terminals are output during "L" level.
			<In 68 type MPU mode >(SEL68="H")
			  Enable signal from 68 type MPU input terminal. Active "H".

13	$\overline{WR}(RW)$	I	WR(80 type) or R/W(68 type) signal input terminal
			<In 80 type MPU mode >(SEL68="L")
			  $\overline{WR}$ signal from 80 type MPU input terminal. Active "L".
			  The data transmitted during WR="L" are fetched at the rising edge of $\overline{WR}$.
			<In 68 type MPU mode > (SEL68="H")
			  R/W signal from 68 type MPU input terminal.<table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>State</td><td>Read</td><td>Write</td></tr></table>

4	SEL68	I	MPU interface type selection terminal. This terminal must connect to V_{DD} or V_{SS}.<table><tr><td>SEL68</td><td>H</td><td>L</td></tr><tr><td>State</td><td>68 Type</td><td>80 Type</td></tr></table>
3	P/S	I	Parallel or Serial interface selection signal input terminal.<table><tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>serial Clock</td></tr><tr><td>"H"</td><td>$\overline{CS}$</td><td>A</td><td>D_0 to D_7</td><td>$\overline{RD},\overline{WR}$</td><td>-</td></tr><tr><td>"L"</td><td>$\overline{CS}$</td><td>A0</td><td>SI(D_7)</td><td>-</td><td>SCL(D_6)</td></tr></table>In case of serial interface(P/S="L") RAM data and status read operation do not work in mode of the serial interface. $\overline{RD}$ and $\overline{WR}$ terminals must fix to "H" or "L". D_0 to D_5 terminals are Hi-impedance.
9 10	OSC_1 OSC_2	I	External clock input terminal. In Internal oscillation operation, OSC1 and OSC2 terminals should be Open.In External clock operation, the external clock input to OSC1 terminal.

45 to 88	C_0 to C_{43}	O	LCD driving signal output terminals.
			  Common output terminals:C_0 to C_{87}
			  Segment output terminals:S_0 to S_{131}
			
			Common output terminal
			Following output voltage is selected by the combination of alternating (FR) signal and Common scanning data.

89 to 220	S_0 to S_{131}	O	<table><tr><td>Scan data</td><td>FR</td><td>Output Voltage</td></tr><tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr><tr><td>L</td><td>V_{DD}</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr><tr><td>L</td><td>V_4</td></tr></table> Segment output terminal Following output voltage is selected by the combination of alternating (FR) signal and display data in the DD RAM.
264 to 221	C_{44} to C_{87}	O	<table><tr><td rowspan="2">RAM Data</td><td rowspan="2">FR</td><td colspan="2">Output Voltage</td></tr><tr><td>Normal</td><td>Reverse</td></tr><tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr><tr><td>L</td><td>V_5</td><td>V_3</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr><tr><td>L</td><td>V_3</td><td>V_5</td></tr></table>

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

The Busy Flag (BF) is set to logical "1" in busy of internal execution by an instruction, and any instruction excepting for the "Status Read" is disable at this time. Busy Flag is outputted through D_7 terminal by "Status Read" instruction. Although another instructions should be inputted after check of Busy Flag, no need to check Busy flag if the system cycle time (t_{CYC}) as shown in ■AC Characteristics is secured completely.

(1-2)Display Start Line Register

The Display Start Line Register is a register to set a display data RAM address corresponding to the COM_0 display line (the top line normally) for the vertical scroll on the LCD, Page address change and so forth. The Display Start Line Address set instruction sets the 8-bit display start address into this register.

(1-3) Line Counter

Line Counter is reset when the internal FR signal is switched and outputs the line address of the display data RAM by count up operation synchronizing with common cycle of **NJU6677**.

(1-4) Column Address Counter

Column Address Counter is the 8-bit preset-able counter to point the column address of the display data RAM (DD RAM) as shown in Figure 1. The counter is incremented automatically after the display data read/write instructions execution. When the Column address counter reaches to the maximum existing address by the increment operations, the count up operation (increment) is frozen. However, when new address is set to the column address counter again, it restarts the count up operation from a set address. The operation of Column Address Counter is independent against Page Address Register.

By the address inverse instruction (ADC select) as shown in Figure 1, Column Address Decoder reverses the correspondence between Column address and Segment output of display data RAM.

(1-5) Page address Register

Page Address Register assigns the page address of the display data RAM as shown in Figure 1. In case of accessing from the MPU with changing the page address, Page Address Set instruction is required.

(1-6) Display Data RAM

The Display data RAM (DD RAM) is the bit map RAM consisting of 15,840 bits to store the display data corresponding to the LCD pixel on LCD panel.

The DD RAM data and the state of the LCD:

        In Normal Display : "1"=Turn-On Display, "0" =Turn-Off Display
        In Reveres Display : "1"=Turn-Off Display, "0" =Turn-On Display

DD RAM output 132 bits parallel data addressed by line address counter then the data latched in the display data latch. Asynchronous data access to the DD RAM is available due to the access to the DD RAM from the CPU and latch to the display data latch operation are done independently.

(1-7) Common Driver Assignment

This circuit determines the scanning direction of the common output.

Table 1

PAD No.	COM Outputs Terminals				
PAD No.	45	88		221	264
Pin name	C_0	C_{43}		C_{87}	C_{44}
Ver.A	COM_0 ———————→COM_{43}			COM_{87} ←——————— COM_{44}	
Ver.B	COM_{88} ←——————— COM_{44}			COM_0 ———————→COM_{43}	

The Mask fixes the common scanning direction between version A and B that can not be changed by the instruction.

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Page Address	DATA	Display Pattern	Line Address
D3,D2,D1,D0 (0,0,0,0)	D0	Pege 0	00
	D1		01
	D2		02
	D3		03
	D4		04
	D5		05
	D6		06
	D7		07
D3,D2,D1,D0 (0,0,0,1)	D0	Pege 1	08
	D1		09
	D2		0A
	D3		0B
	D4		0C
	D5		0D
	D6		0E
	D7		0F
D3,D2,D1,D0 (0,0,1,0)	D0	Pege 2	10
	D1		11
	D2		12
	D3		13
	D4		14
	D5		15
	D6		16
	D7		17
	D0		18
	D1		19
	D6		5E
	D7		5F
D3,D2,D1,D0 (1,1,0,0)	D0	Pege 12	60
	D1		61
	D2		62
	D3		63
	D4		64
	D5		65
	D6		66
	D7		67
D3,D2,D1,D0 (1,1,0,1)	D0	Pege 13	68
	D1		69
	D2		6A
	D3		6B
	D4		6C
	D5		6D
	D6		6E
	D7		6F
D3,D2,D1,D0 (1,1,1,0)	D0	Pege 14	70
	D1		71
	D2		72
	D3		73
	D4		74
	D5		75
	D6		76
	D7		77

Cn Out: C0, C1, C2, C3, C4, C5, C6, C7, C8, C9 ... C78, C79, C80, C81, C82, C83, C84, C85, C86, C87

For example the Display start line is 10H

Column Address	ADC	D0="0"	00	01	02	03	04	05	06	07	08	09		7A	7B	7C	7D	7E	7F	80	81	82	83
		D0="1"	83	82	81	80	7F	7E	7D	7C	7B	7A		09	08	07	06	05	04	03	02	01	00
	Segment Output		0	1	2	3	4	5	6	7	8	9		122	123	124	125	126	127	128	129	130	131

Fig.1 Correspondence with Display Data RAM Address

(1-8) Reset Circuit

When the input signal to $\overline{\text{RES}}$ terminal goes to "L", the reset circuit executes initialization as below;

The Initialization state (default)

1. Display Off
2. Normal Display (not inverse)
3. ADC Select : Normal (ADC Instruction D_0 ="0")
4. Read Modify Write Mode Off
5. Voltage Booster off, Voltage Regulator off, Voltage follower off
6. Static Drive Off
7. Driver Output Off
8. Clear the data of serial interface register
9. Set the Column Address Counter to 00H
10. Set the Display Start Line Register to 00H
11. Set the Page Address Register to page "0"
12. Set the EVR register to FFH
13. Set the Partial Display(1/88 duty)
14. Set the Bias select(1/10 Bias)
15. Set the Voltage Booster(5 times)
16. Set the n-line inverse register to 0H

The $\overline{\text{RES}}$ terminal connects to the reset terminal of the MPU synchronization with the MPU initialization as shown in " the MPU interface " in the Application Circuit section. The "L" level input signal as reset signal must keep the period over than 10us as shown in DC Characteristics. The **NJU6677** takes 1us for the reset operation after the rising edge of the $\overline{\text{RES}}$ signal.

The reset operation by $\overline{\text{RES}}$ ="L" initializes each resister setting as above reset status, but the internal oscillation circuit and output terminals (D0 to D7) are not affected.

To avoid the lock-up, the reset operation by the $\overline{\text{RES}}$ terminal must be required every time when power terns on.

The reset operation by the reset instruction, function 9 to 16 operations mentioned above is performed.

The $\overline{\text{RES}}$ terminal must be keep "L" level when the power terns on in not use of the built-in LCD power supply circuit for no affect to the internal execution.

(1-9) LCD Driving Circuit

(a) LCD Driving Circuits

LCD driver is 220 sets of multiplexer consisting of 132 segments and 88 commons drivers to output LCD driving voltage. The common driver outputs the common scan signals formed with the shift register. The segment driver outputs the segment driving signal determined by a combination of display data in the DD RAM, common timing, FR signal, and alternating signal for LCD. The output wave forms of segment/common are shown in ■LCD DRIVING WAVEFORM.

(b) Display Data Latch Circuits

Display Data Latch Circuit latches the 132-bit display data outputted from the DD RAM addressed by the Line address counter to LCD driver at every common signal cycle temporarily. The original data in the DD RAM is not changed because of the Normal/Reverse display, Display On/Off, Static drive On/Off instruction processes only stored data in this Display Data Latch Circuit.

(c) Signal forming to Line Counter and Display Data Latch Circuit

The count clock to Line Counter and the latch clock to Display Data Latch Circuit are formed using the internal display clock (CL). The display data of 132 bits from Display Data RAM pointed by the line address synchronizing with the internal display clock are latched into the Display Data Latch Circuit and are outputted to LCD driving circuits.

The display data read out operation from DD RAM to the LCD Driver Circuit is completely independent operation with an access to the display data RAM from MPU.

(d) Display Timing Generation Circuit

The display timing generation circuit generates the internal timing of the display system by the master clock and the internal FR signal. As for it, the internal FR signal and the LCD alternating signal generate the wave form of 2-frame alternating drive wave form or the n-line inverse drive method for the LCD Driving circuit.

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(e)Common Timing Generator
   The Common Timing Generator generates the common timing signal from the display clock (CL).

-2-frame alternating drive mode
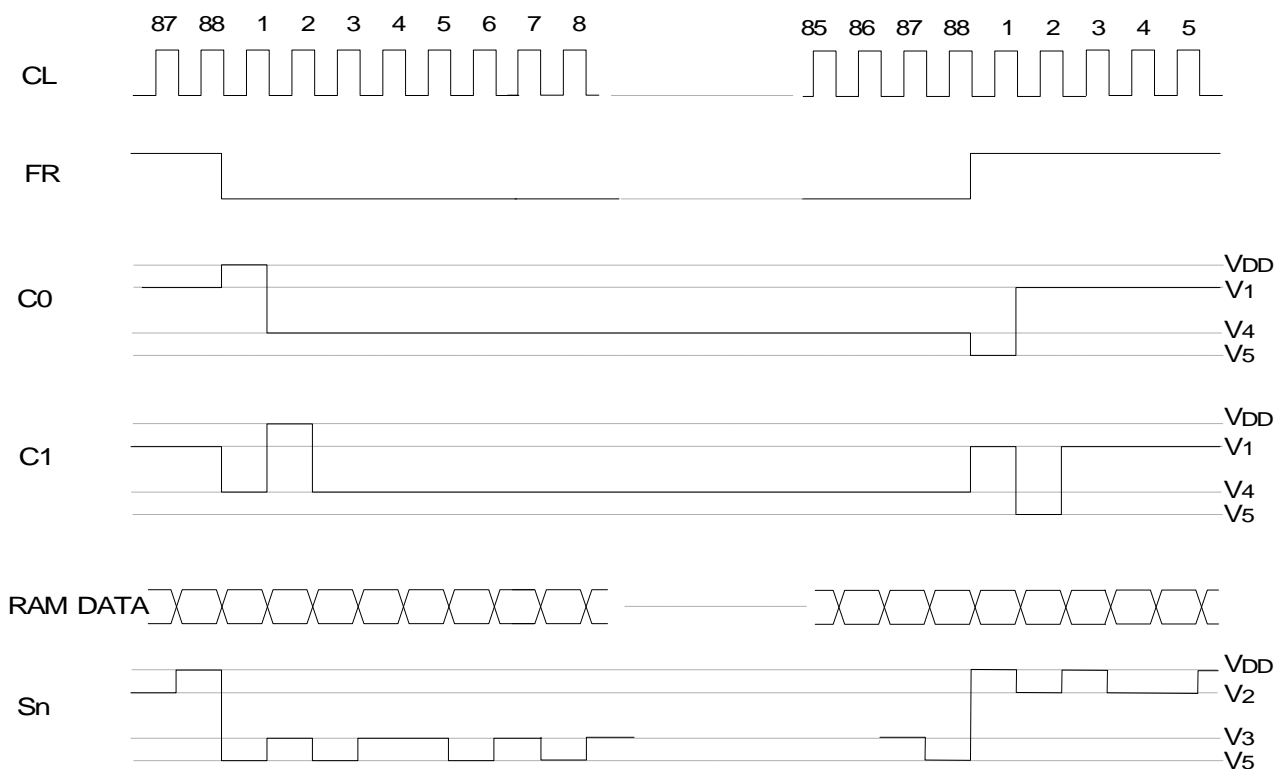
Fig.2

-n-line inverse drive mode (n=7, line inverting register sets to 6)
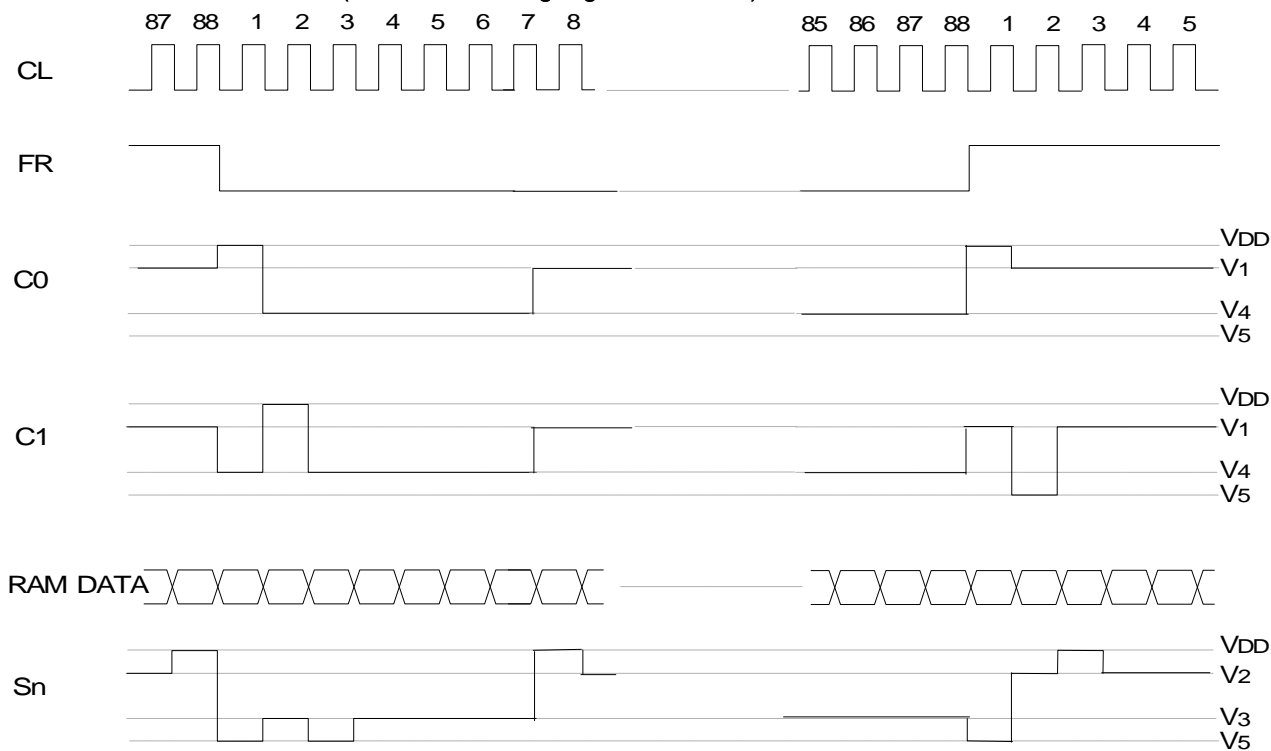
Fig.3

(f) Oscillation Circuit

The Oscillation Circuit is a low power type CR oscillator using an internal resistor and capacitor. The oscillator output is using for the display timing clock and for the voltage booster circuit. And the display clock(CL) is generated from this oscillator output frequency by dividing.

  -The relation between duty and divide

Table 2

Duty	1/8	1/16	1/24	1/32	1/40	1/48	1/56,64	1/72	1/80,88
Divide	1/44	1/22	1/15	1/11	1/9	1/7	1/6	1/5	1/4

(g) Power Supply Circuit

The internal power supply circuit generates the voltage for driving LCD. It consists of voltage booster circuits (from 2 times to 5 times), voltage regulator circuits, and voltage followers.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the voltage booster circuits, regulator circuits, voltage follower circuits are turned off. In this time, the bias voltage of V_1, V_2, V_3, V_4,V_5 and V_{OUT} for the LCD should be supplied from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$, $C3^+$, $C3^-$, $C4^+$, $C4^-$, and VR should be open. The status of internal power supply is selected by T_1 and T_2 terminal. Furthermore the external power supply operates with some of internal power supply function.

Table 3

T_1	T_2	Voltage Booster	Voltage Adj.	Buffer(V/F)	Ext.Pow Supply	C1+,C1- to C4+,C4-	VR Term.
L	L/H	ON	ON	ON	-		
H	L	OFF	ON	ON	V_{OUT}	Open	
H	H	OFF	OFF	ON	V_5,V_{OUT}	Open	Open

When (T_1, T_2)=(H, L), $C1^+$, $C1^-$, $C2^+$, $C2^-$,$C3^+$, $C3^-$, $C4^+$, $C4^-$ terminals for voltage booster circuits are open because the voltage booster circuits doesn't operate. Therefore LCD driving voltage to the V_{OUT} terminal should be supplied from outside.

When (T_1, T_2)=(H, H), terminals for voltage booster circuits and VR are open, because the voltage booster circuits and Voltage adjust circuits do not operate.

The internal power supply Circuits is designed specially for a small-size LCD like as normal cellular phone size LCD panel. When **NJU6677** apply to the large size LCD panel application (large capacitive load), external power supply is required to keep good display condition..

To keep good display condition, external component of the capacitors connecting to the V1 to V5 terminals and voltage booster circuits and the feedback resistors for the V5 operational amplifier must fix each optimized constant after checking various display patterns on LCD panel actually in the application.

○Power Supply applications

(1) Internal Power Supply Example.
All of the Internal Booster, Voltage Regulator,
Voltage Follower using.
Internal power supply ON (instruction)　(T1,T2)=(L,L)
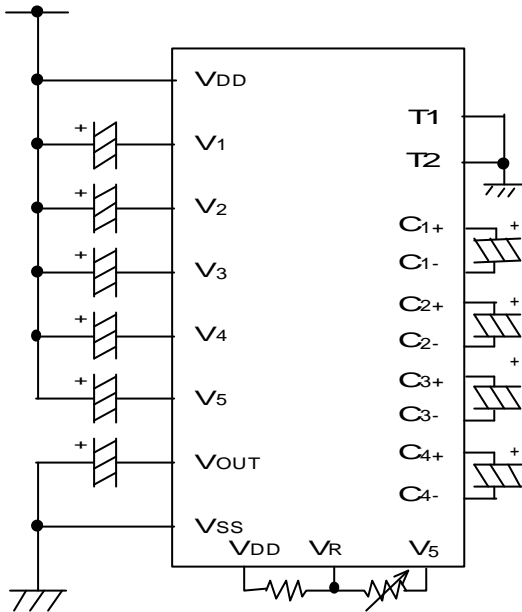
(2) Only V$_{OUT}$ Supply from outside Example.
Internal Voltage Regulator, Voltage Follower using
Internal power supply ON (Instruction)　(T1,T2) = (H,L)
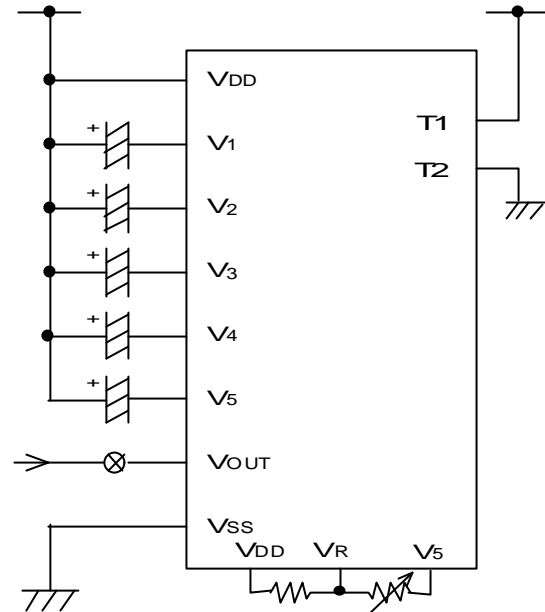
(3) V$_{OUT}$ and V5 supply from outside Example.
Internal Voltage Follower using.
Internal power supply (Instruction)　(T1,T2) =(H,H)
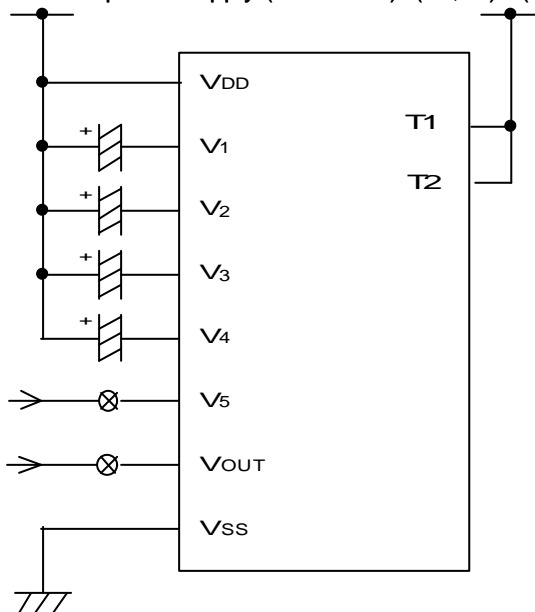
(4) External Power Supply Example
All of V1 to V5 and V$_{OUT}$ supply from outside
Internal power supply (Instruction)　(T1,T2) =(H,H)
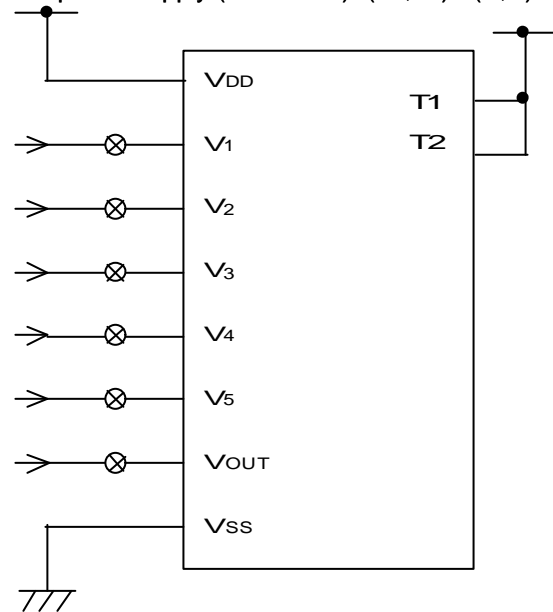
⊗ : These switches should be open during the power save mode.

(2) Instruction

The **NJU6677** distinguishes the data on the data bus D0 to D7 as an instruction by combination of A0, $\overline{RD}$, and $\overline{WR}$(R/W) signals. The decoding of the instruction and exection performes with only high speed internal timing without relation to the external clock. Therefore, no busy flag check required normally. In case of the serial interface, the data input as MSB(D7) first serially. Table.4 shows the instruction codes of the **NJU6677**.

Table 4. Instruction Code (*:Don't Care)

| Instruction		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Description
(a)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	LCD Display ON/OFF 0:OFF 1:ON
(b)	Display Start Line Set High Order 4bits	0	1	0	0	1	0	1	High Order Address				Determine the Display Line of RAM to the COM0. (Set the Higher order 4bits)
	Display Start Line Set Lower Order 4bits	0	1	0	0	1	1	0	Lower Order Address				Determine the Display Line of RAM to the COM0. (Set the Lower order 4bits)
(c)	Page Address Set High Order 1bits	0	1	0	0	1	0	0	*	*	*	Hi.	Set the Higher order 1bit page of DD RAM to the Page Address Register
	Page Address Set Lower Order 4bits	0	1	0	1	1	0	0	Lower Order Page Address				Set the Lower order 4 bit page of DD RAM to the Page Address Register
(d)	Column Address Set High Order 4bits	0	1	0	0	0	0	1	High Order Column Add.				Set the Higher order 4 bits Column Address to the Reg.
	Column Address Set Lower Order 4bits	0	1	0	0	0	0	0	Lower Order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(e)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status
(f)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(g)	Read Display Data	1	0	1	Read Data								Read the data from the Display Data RAM
(h)	Normal or Inverse ON/OFF Set	0	1	0	1	0	1	0	0	1	1	0/1	Inverse the ON and OFF Display 0:Normal 1:Inverse
(i)	Static Drive ON /Normal Display	0	1	0	1	0	1	0	0	1	0	0/1	Whole Display Turns ON 0:Normal 1:Whole Disp. ON
(j)	Sub instruction table mode	0	1	0	0	1	1	1	0	0	0	0	Set the Sub instruction table.
Sub inst.	**(k)Partial Display**												
	1st Block, Set Start display unit	0	1	0	0	0	0	0	Start display unit				Set the Start display unit of 1st Block.
	1st Block, Set The number of display units	0	1	0	0	0	0	1	number of display units				Set the number of display units of 1st Block.
	2nd Block, Set Start display unit	0	1	0	0	0	1	0	Start display unit				Set the Start display unit of 2nd Block.
	2nd Block, Set The number of display units	0	1	0	0	0	1	1	number of display units				Set the number of display units of 2nd Block.
	Partial display on	0	1	0	0	1	0	0	0	0	0	0	It comes off the mode to set and a display is executed.
	(l)n-line Inverse Drive Set												
	Register Set Higher order 2 bits	0	1	0	0	1	0	1	*	*	higher order		Set the number of inverse drive line.
	Register Set Lower order 4 bits	0	1	0	0	1	1	0	Lower order				Set the number of inverse drive line.
	n-line Inverse Drive Set is executed.	0	1	0	0	1	1	1	0	0	0	0	The execution of the line inverse drive.
	(m)EVR Register Set												
	EVR Register Set Higher order 4 bits	0	1	0	1	0	0	0	EVR Data Higher order				Set the V5 output level to the EVR register. (Higher order 4 bits)
	EVR Register Set Lower order 4 bits	0	1	0	1	0	0	1	EVR Data Lower order				Set the V5 output level to the EVR register. (Lower order 4 bits)
	EVR Register Set is executed.	0	1	0	1	0	1	0	0	0	0	0	The execution of the EVR.
(n)	End of sub instruction table mode	0	1	0	0	1	1	1	0	0	0	1	It ends the setting of sub instruction table.

(*:Don't Care)

Instruction		A0	RD̄	W̄R̄	D7	D6	D5	D4	D3	D2	D1	D0	Description
(o)	Bias Select	0	1	0	1	0	1	1	*	Bias			Select the bias (7 Patterns)
(p)	Boost Level Select	0	1	0	0	0	1	1	0	0	Boost Multiple		Set the Booster circuits
(q)	Read Modify Write /End	0	1	0	1	1	1	0	0	0	0	0/1	Read Modify Write mode D0=0:On D0=1:End
(r)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(s)	Internal Power Supply ON/OFF	0	1	0	0	0	1	0	0	0	0	0/1	0:Int. Power Supply OFF 1:Int. Power Supply ON
(t)	Driver Outputs ON/OFF	0	1	0	0	0	1	0	0	0	1	0/1	D0=0: LCD Driver Outouts OFF D0=1: LCD Driver Outputs ON
(u)	Power Save (Complex Command)	0	1	0	1	0	1	0	1	1	1	0	Set the Power Save Mode (LCD Display OFF +Static Drive ON)
		0	1	0	1	0	1	0	0	1	0	1	
(v)	ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	Set the DD RAM vs Segment D0=0:Normal D0=1:Inverse

(2-1) Explanation of Instruction Code

(a) Display On/Off
It executes the ON/OFF control of the whole display without relation to the DD RAM or any internal conditions.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

D 0:Display Off
 1:Display On

(b) Display Start Line
It sets the DD RAM line address corresponding to the COM0 terminal (normally assigned to the top display line). In this instruction execution, the display area is automatically set by the lines that correspond to the display duty ratio to the upward direction of the line address. Changing the line address by this instruction performs smooth scrolling to a vertical direction. In this time, the DD RAM data are unchanged.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	A7	A6	A5	A4

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line Address(HEX)
0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	01
			:	:				:
0	1	1	1	0	1	1	1	77

(c) Page Address Set
When MPU access to the DD RAM, a page address is set by page Address Set instruction before writing the data. (Note: the change of page address is not affected to the display.)

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	0	*	*	*	A4

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	A3	A2	A1	A0

(*:Don't Care)

A4	A3	A2	A1	A0	Page
0	0	0	0	0	0
0	0	0	0	1	1
		:	:		:
0	1	1	1	0	14

(d) Column Address

When MPU accesses to the DD RAM , the row address set by Page Address Set instruction is required with the column address before writing the data. The column address set requires twice address set which are higher order 4 bits address set and lower order 4 bits.

When the MPU access to the DD RAM continuously, the column address increments automatically from the set address after each data access. Therefore, the MPU can transmit only the Data continuously without setting the column address at every transmission time. The increment of column address is stopped at the maximum column address plus 1 limited by each display mode. When the column address count up is stopped, the row address is not changed.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	A7	A6	A5	A4	Higher Order
0	1	0	0	0	0	0	A3	A2	A1	A0	Lower Order

A7	A6	A5	A4	A3	A2	A1	A0	Column Address(HEX)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
			:					:
			:					:
1	0	0	0	0	0	1	1	83

(e) Status Read

This instruction reads out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET" described as follows.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY　: BUSY=1 indicate the operating or the Reset cycle.
　　　　All instructions can be input after the BUSY status change to "0".

ADC　　: Indicate the output correspondence of column (segment) address and segment driver.
　　　0 :Counterclockwise Output (Inverse)
　　　1 :Clockwise Output　　　(Normal)
　　(Note) The data "0=Inverse" and "1=Normal" of ADC status is inverted with the ADC select
　　　　　Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
　　　　0 : Whole Display "On
　　　　1 : Whole Display "Off"
　　(Note) The data "0=On" and "1=Off" of Display On/Off status is inverted with the Display On/Off
　　　　　instruction data of "1=On" and "0=Off".

RESET　: Indicate the initializing by $\overline{RES}$ terminal signal or reset instruction.
　　　　0 : Not Reset status
　　　　1 : In the Reset status
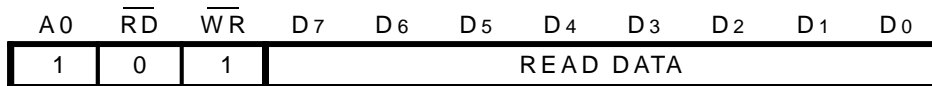
(f) Write Display Data

It writes the data on the data bus into the DD RAM. column address increments automatically after data writing, therefore, the MPU can write the data into the DD RAM continuously without the address setting at every writing time once the starting address is set.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	WRITE DATA							
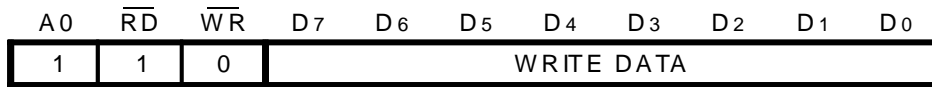
(g) Read Display Data

This instruction reads out the 8-bit data from DD RAM addressed by the column and the page address. The column address automatically increments after the 8-bit data read out, therefore, the MPU can read the data from the DD RAM continuously without the address setting at every reading time once the starting address is set. Note that the dummy read is required just after setting the column address (see "(4-4) Access to the DD RAM and the Internal Register").
 In the serial interface mode, the display data is unable to read out.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	READ DATA							

(h) Normal or Inverse On/Off Set

It changes the display condition of normal or reverse for entire display area. The execution of this instruction does not change the display data in the DD RAM.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D
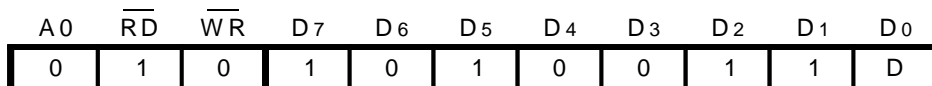
D 0 : Normal   RAM data "1" correspond to "On"
  1 : Inverse   RAM data "0" correspond to "On"

(i) Static Drive

 This instruction turns all the pixels ON regardless the data stored in the DD RAM. In this time, the data in DD RAM are remained and unchanged. This instruction is executed prior to the "Normal or Inverse On/Off Set" Instruction.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D
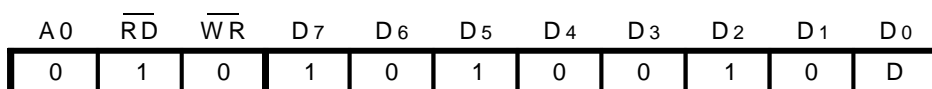
D 0 : Normal Display
  1 : Whole Display turns On

When the "Static Drive ON" instruction is executed at Display OFF status, the **NJU6677** operates in Power Save Mode. (Refer " Power Save Mode ")

(j) Sub Instruction table mode

This instruction switches the instruction table from the main to the sub. The sub instruction table contains instructions of partial display, n-line inverse drive set and EVR register set as mentioned in (k), (l) and (m).
The instruction of sub instruction table mode must be executed before above 3 sub instructions execution. The instruction of end of sub instruction table mode (n) switches the instruction table from the sub to the main. If any main instructions are written in the sub instruction mode, the **NJU6677** will malfunction.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	0

-Set sub Instruction table flow is shown below:

Sub Instruction table mode	Switches to Sub instruction table mode.
Set sub instructions.	
End of Sub Instruction table mode.	Switches to Main instruction mode.
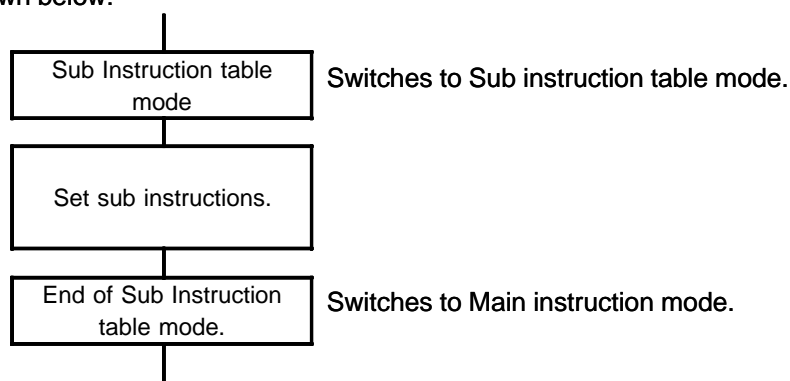
(k) Partial Display

It selects two active display areas on the LCD Panel partially. The display area is divided to 11 units with four commons each and selected two display blocks by setting Unit number and number of Unit required (not overlap, not over than 11 units) to display on the LCD panel. These two display blocks are assigned optionally on the LCD panel. Duty selects an adapted ratio number corresponding to the total number of two display blocks automatically.
Partial Display function adjusts the LCD driving voltage, Voltage boosting times and E.V.R level by the instruction to generate the optimum LCD driving voltage for display quality. As result, the operating current is reduced.

· Display Unit Structure

UNIT	0	(8 commons)	
UNIT	1		
UNIT	2		
UNIT	3		
UNIT	4		
UNIT	5		88-common
UNIT	6		
UNIT	7		
UNIT	8		
UNIT	9		
UNIT	10	(8 commons)	

132-segment

Partial display instruction
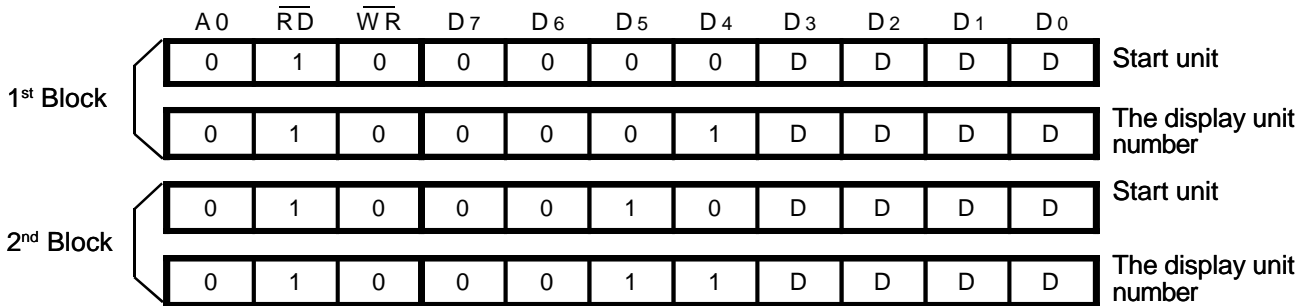When Partial Display functions, both of Top Unit Number of display area (the Start Unit) and the number of the effective continuous unit (Display Unit) from the Start Unit for the first display block and the second. Attention that the first display block and the second definition must not be overlap of display area and not be over than 11 units in total.

In case of whole display (1/88 duty), the first display block defines Start Unit=0 (0,0,0,0) and Display Unit = 11 (1,0,1,1) for all of display area selection. In this time, the definition of the second display block is ignored.
In case of only the first block display, the second display block defines Start Unit=0 (0,0,0,0) and Display Unit = 0 (0,0,0,0) for no display area.

	A_0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1st Block	0	1	0	0	0	0	0	D	D	D	D	Start unit
	0	1	0	0	0	0	1	D	D	D	D	The display unit number
2nd Block	0	1	0	0	0	1	0	D	D	D	D	Start unit
	0	1	0	0	0	1	1	D	D	D	D	The display unit number

By input following instruction, the duty ratio is changed automatically and executes the partial display function.

A_0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	1	0	0	0	0	0	0	Partial display on
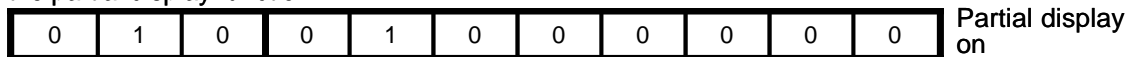
D :unit number (Hex.)

Notes) Attention followings due to prevent from mulfunction
· The input order of Partial Display instructions must follow above.
· Prohibits the overlap of the 1st partial display block and the 2nd.
· The Start Unit of the 1st partial display block must not be over 10.
· The total Display Unit Number (the sum of the 1st and 2nd partial display block Unit Number) must not be over 11.
· On the LCD panel, no active display area inserts between the 1st display block and the 2nd. However, the display data of the 1st display block and the 2nd must store continuously in the display data RAM.

Example of the Partial Display setting.

(display diagram)	1st Block
	2nd Block

UNIT 0
UNIT 1
UNIT 2
UNIT 3
UNIT 4
UNIT 5
UNIT 6
UNIT 7
UNIT 8
UNIT 9
UNIT 10
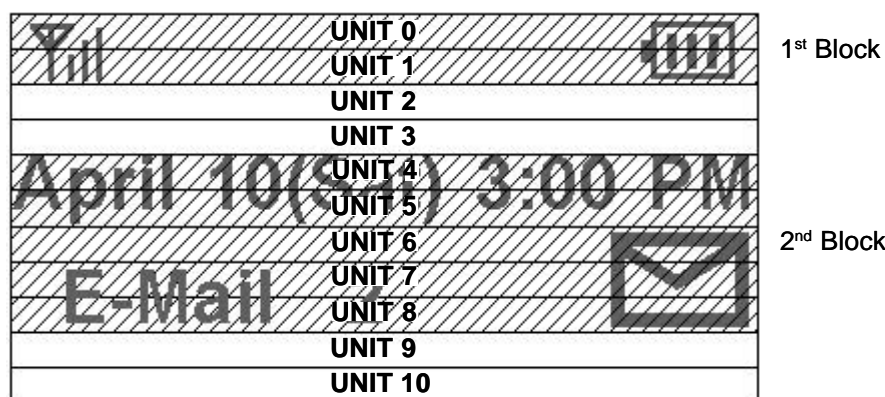
☐ active display-block

The above partial display condition is set as follows:

1)Set sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	0	Set sub instruction mode.

2)Set partial display conditions

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	0	0	0	0	0	1st Block, Set start unit to "0"
0	1	0	0	0	0	1	0	0	1	0	1st Block, Set the display unit number to "2"
0	1	0	0	0	1	0	0	1	0	0	2nd Block, Set start unit to "4"
0	1	0	0	0	1	1	0	1	0	1	2nd Block, Set the display units number to "5"
0	1	0	0	1	0	0	0	0	0	0	Execute Partial display.

The Duty is changed to 1/56 automatically.

3)End sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	1	End sub instruction mode. Back to main instruction mode.

Duty is changed automatically when Partial Display execution. But LCD Driving Voltage, Bias, Driving form like as 2-frame alternating driving or n-line inverse are not changed. Therefore, Display Off should operate before Partial Display execution for prevention of unexpected display, and Voltage Booster Select instruction, E.V.R Register Set, Bias Select and n-line Inverse Driving Set should set optimum conditions for good display in the mean time of Partial Display instruction execution. The optimum conditions should fix refering the result of actual display eveluation.

-Set Partial Display flow is shown below:

Internal Power Supply OFF
Sub Instruction Table Mode
Set a Start Unit of the first display unit
Set a number of Display Unit of the first
Set a Start Unit of the second display unit
Set a number of Display Unit of the second
Executes Partial Display function
n-line Inverse Drive Set
EVR Register Set
End Sub Instruction Table Mode
Bias Select
Voltage Booster Times Select
Wait Time
Internal Power Supply ON

(I) n-line Inverse Drive Mode

n-Line Inverse Register Set (refer +Functional Description Fig.3 n-line Inverse alternative drive mode)
It sets a line number to inverse the polarity of common driver and segment.
The instructions must be input in order of followings. These instructions are sub instruction sets and must be set after (j)Sub instruction table mode.

1)Set sub instruction mode

A_0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	1	1	1	0	0	0	0	Set sub instruction mode.

2)Set n-line Inverse number

A_0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	1	0	1	*	*	A_5	A_4	Higher order
0	1	0	0	1	1	0	A_3	A_2	A_1	A_0	Low order

A_5	A_4	A_3	A_2	A_1	A_0	Inverse line	
0	0	0	0	0	0	-(*)	(*:2-frame alternating drive mode.)
0	0	0	0	0	1	2	
			:			:	
1	1	1	1	1	1	64	

3)Execute the n-line Inverse

A_0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	1	0	0	0	0

4)End sub instruction mode

A_0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	1	1	1	0	0	0	1	End sub instruction mode. Back to main instruction mode.

(m) EVR Register Set

It controls the voltage regulator circuit of the internal LCD power supply to adjust the LCD display contrast by changing the LCD driving voltage "V5". By data setting into the EVR register, the LCD driving voltage "V5" selects out of 201 steps of regulated voltage. The voltage adjustable range of "V5" is fixed by the external resistors. For details, refer the section "(3-2) Voltage Adjust Circuits".

1)Set sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	0	Set sub instruction mode.

2)Set EVR Register

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	A7	A6	A5	A4

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	1	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	VLCD		
0	0	1	1	0	1	1	1	Low		
			:	:				:		
			:	:				:		
1	1	1	1	1	1	1	1	High		

$V_{LCD}=V_{DD}-V5$
When EVR doesn't use, set the EVR register to (1,1,1,1,1,1,1,1).

3)Execute the EVR

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	0

4)End sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	1	End sub instruction mode. Back to main instruction mode.

(n) End of Sub instruction table mode

"End of sub instruction table mode" instruction switches instruction table from sub to main.
(k)Partial display, (l)n-line inverse drive mode, and (m)EVR are sub instruction sets on the sub instruction table. The instruction of "END of sub instruction mode" must be set after these sub instruction sets. The **NJU6677** may occur incorrect operation if any main instructions on the main instruction table are input in mode of sub instruction table.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	1

(o) Bias Select
This instruction sets the bias voltage.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	*	A2	A1	A0	(*:Don't Care)

| A2	A1	A0	Bias
0	0	0	1/4
0	0	1	1/5
0	1	0	1/6
0	1	1	1/7
1	0	0	1/8
1	0	1	1/9
1	1	*	1/10

(p) Boost Level Select

This instruction sets the boost level (2 to 5 times). When "Partial Display Instruction" execution, the "Boost Level Select" also must be executed. If the external capasitors are connected as the lower than 5 times boost level, don't set the boost level by the instruction over than the boost level by conecting capasitors. If set the boost level over than it, the device will make malfunction.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	0	0	A1	A0

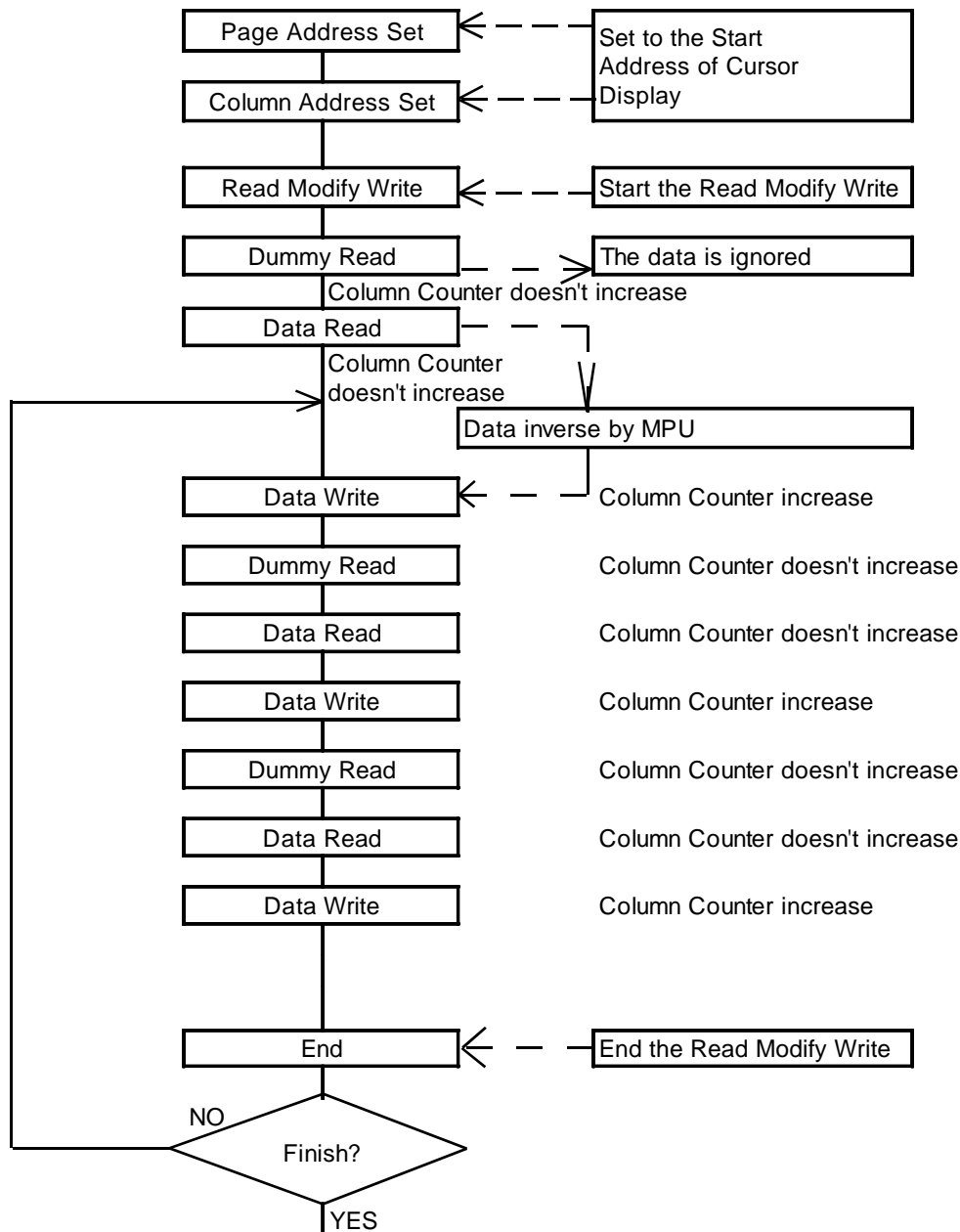| Command		Booster Multiple			
A1	A0	5times external capacitors connections	4times external capacitors connections	3times external capacitors connections	2times external capacitors connections
0	0	2-time			
0	1	3-time	2-time		
1	0	4-time	3-time	2-time	
1	1	5-time	4-time	3-time	2-time

(q) Read Modify Write/End

This instruction sets the Read Modify Write controlling the page address increment. In this mode, the Column Address only increments when execute the display data "Write" instruction; but no change when the display data "Read" Instruction. This status is continued until the End instruction execution. When the End instruction is executed, the Column Adddress goes back to the start address before the execution of this "Read Modify Write" instruction. This function reduces the load of MPU for repeating display data change of the fixed area (ex. cursor blink).

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	D
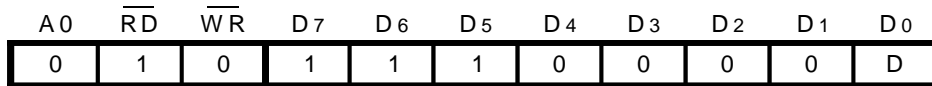
D 0 : Read Modify Write On

1 : End

Note) In this "Read Modify Write" mode, out of display dara "Read"/"Write", any instructions except "Column Address Set" can be executed.

- The Example of Read Modify Write Sequence

```
Page Address Set  ⇐ ─ ─ ┐   Set to the Start
                         │   Address of Cursor
Column Address Set ⇐ ─ ─ ┘   Display

Read Modify Write ⇐ ─ ─ ─  Start the Read Modify Write

Dummy Read  ─ ─ ─>  The data is ignored
Column Counter doesn't increase

Data Read  ─ ─ ┐
Column Counter   │
doesn't increase │
                 V
          Data inverse by MPU

Data Write  ⇐ ─ ┘   Column Counter increase

Dummy Read          Column Counter doesn't increase

Data Read           Column Counter doesn't increase

Data Write          Column Counter increase

Dummy Read          Column Counter doesn't increase

Data Read           Column Counter doesn't increase

Data Write          Column Counter increase

End  ⇐ ─ ─  End the Read Modify Write

        NO
         <Finish?>
         YES
```

(r) Reset

This instruction executes the following initialization.
The reset by the reset signal input to the $\overline{\text{RES}}$ terminal (hardware reset) is required when power turns on. This reset instruction does not use instead of this hardware reset when power turns on.

Initialization

1	Set the Column Address Counter to 00H
2	Set the Display Start Line Register to 00H
3	Set the Page Address Register to page "0"
4	Set the EVR register to FFH
5	Set the Partial Display(1/88 duty)
6	Set the Bias select(1/10 Bias)
7	Set the Voltage Booster(5 times)
8	Set the n-line inverse register to 0H

The DD RAM is not affected in this initialization.

A 0	$\overline{\text{R D}}$	$\overline{\text{W R}}$	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	1	0	1	1	1	0	0	0	1	0

(s) Internal Power Supply ON/OFF

This instruction control ON and OFF for the internal Voltage Converter, Voltage Regulator and Voltage Follower circuits. For the Booster circuits operation, the oscillation circuits must be in operation.

A 0	$\overline{\text{R D}}$	$\overline{\text{W R}}$	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	1	0	0	0	1	0	0	0	0	D

D 0 : Internal Power Supply Off
  1 : Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

*1 The set up period of internal power supply On depends on the step up capacitors, voltage stabilizer capacitors, V_{DD} and V_{LCD}.
Therefore it requires the actual evaluation using the LCD module to get the correct time. (Refer to the (3-4) Fig.5)

(t) Driver Outputs ON/OFF

This instruction controlls ON/OFF of the LCD Driver Outputs.

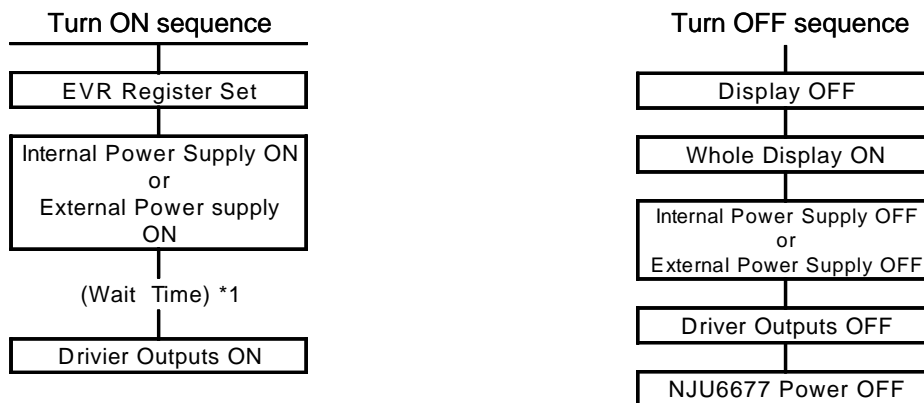| A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	1	D

D 0 : LCD driving waveform output Off

1 : LCD driving waveform output On

The **NJU6677** implements low power LCD driving voltage generator circuit and requires the following Power Supply ON/OFF sequence.

- LCD Driving Power Supply ON/OFF Sequences

The sequences below are required when the power supply turns ON/OFF.

For the power supply turning on operation after the power-save mode, refer the "power save release sequence" mentioned after.

Turn ON sequence

```
          |
┌─────────────────────┐
│   EVR Register Set   │
└─────────────────────┘
          |
┌─────────────────────┐
│ Internal Power Supply ON │
│           or          │
│  External Power supply │
│           ON           │
└─────────────────────┘
          |
     (Wait  Time) *1
          |
┌─────────────────────┐
│   Drivier Outputs ON  │
└─────────────────────┘
```

Turn OFF sequence

```
          |
┌─────────────────────┐
│     Display OFF      │
└─────────────────────┘
          |
┌─────────────────────┐
│   Whole Display ON   │
└─────────────────────┘
          |
┌─────────────────────┐
│ Internal Power Supply OFF │
│           or          │
│ External Power Supply OFF │
└─────────────────────┘
          |
┌─────────────────────┐
│  Driver Outputs OFF  │
└─────────────────────┘
          |
┌─────────────────────┐
│  NJU6677 Power OFF   │
└─────────────────────┘
```

*1 The Internal Power Supply rise time is depending on the condition of the Supply Voltage, VLCD=VDD-V5, External Capacitor of Booster, and External Capacitor connected to V1 to V5. To know the rise time correctly, test by using the actual LCD module.

(u) Power Save (complex comand)

When Static Drive ON at the Display OFF status (inverse order also same), the internal circuits goes to the Power Save Mode and the operating current is dramatically reduced, almost same as the standby current.
The internal status in the Power Save Mode is shown as follows;

1: The Oscillation Circuits and the Internal Power Supply Circuits stop the operation.
2: LCD driving is stopped. Segment and Common drivers output V_{DD} level voltage.
3: The display data and the internal operating condition are remained and kept as just before enter the Power Save Mode.
4: All the LCD driving bias voltage (V1 to V5) is fixed to the V_{DD} level.

The power save and its release perform according to the following sequences.

Power Save Sequence	Power Save Release Sequence
Display OFF	Normal Display (Static Drive ON)
Static Drive ON	Display ON
Driver Outputs OFF	(Wait Time)
	Driver Outputs ON
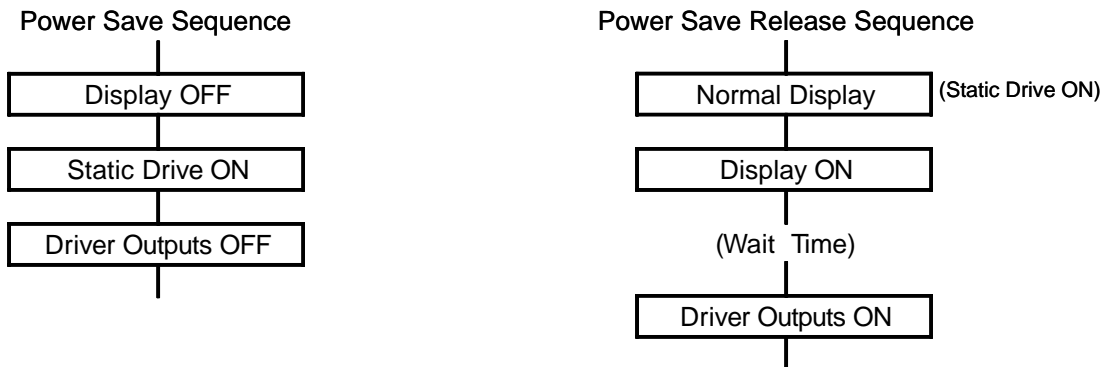
The **NJU6677** constantly spends the current without the execution of the Driver Outputs OFF instruction. The LCD drive waveform is not output until the Driver Outputs ON instruction is executed.

*1 In the Power Save sequence, the Power Save Mode starts after the Static Drive ON command is executed.
*2 In the Power Save Release sequence, the Power Save Mode releases just after the Static Drive OFF instruction execution. The Display ON instruction is allowed to execute at any time after the Static Drive OFF instruction is completed.
*3 The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V5$, External Capacitor of Booster, and External Capacitor connected to V1 to V5. To know the rise time correctly, test by using the actual LCD module.
*4 LCD driving waveform is output after the exection of the Driver Outputs ON instruction execution.
*5 In case of the external power supply operation, the external power supply should be turned off before the Power Save Mode and connected to the V_{DD} for fixing the voltage. In this time, V_{OUT} terminal also should be made codition like as disconection or connection to V_{SS}.

(v) ADC Select

This instruction determines the correspondence of Column in the DD RAM with the Segment Driver Outputs. Segment Driver Output order is inverse, when this instruction executes, therefore, the placement the **NJU6677** against the LCD panel becomes easy.

A0	$\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

D 0 : Clockwise Output (Normal)　　Segment Driver S_0 to S_{131}
　　1 : Counterclockwise Output (Inverse) Segment Driver S_{131} to S_0

(3) Internal Power Supply

(3-1) 5-time voltage booster circuits

The 5-time voltage booster circuit outputs the negative Voltage(V_{DD} Common) boosted 5 times of V_{DD}-V_{SS} from the V_{OUT} terminal with connecting the five capacitors between C_1^+ and C_1^-, C_2^+ and C_2^-, C_3^+ and C_3^-, C_4^+ and C_4^-, and V_{SS} and V_{OUT}. The boosting time is selected out of 2 times to 5 by the combination of changing the external capacitors connection and "Booster Level Select" instruction. (refer (2-1)Instruction (p)Voltage Boost time select)

Voltage Booster circuits requires the clock signals from internal oscillation circuit or the external clock signal, therefore, the internal oscillation circuits or the external clock supplier must be operating when the voltage booster is in operation.

The boosted voltage of V_{DD}-V_{OUT} must be 18V or less.

The boost voltage and the capacitor connection are shown below.

● The boosted voltage and V_{DD},V_{SS}

V_{DD}=+3V
V_{SS}=±0V
V_{OUT}=-V_{DD}=-3V
V_{OUT}=-2V_{DD}=-6V
V_{OUT}=-3V_{DD}=-9V
V_{OUT}=-4V_{DD}=-12V

| 2-time voltage | 3-time voltage | 4-time voltage | 5-time voltage |
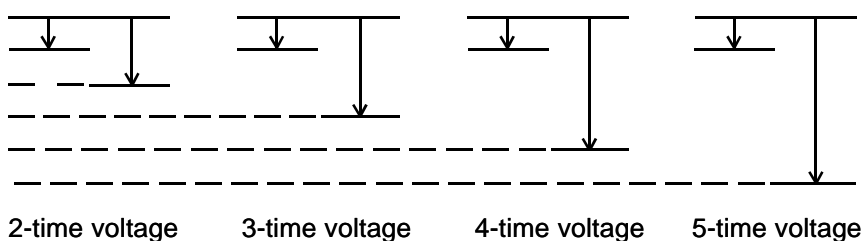
● Example of the external capacitor connection to the voltage booster circuits

5-time voltage

Vss	
C1+	
C1-	
C2+	
C2-	
C3+	
C3-	
C4+	
C4-	
VOUT	

4-time voltage

Vss	
C1+	
C1-	
C2+	
C2-	
C3+	
C3-	
C4+	
C4-	
VOUT	

3-time voltage

Vss	
C1+	
C1-	
C2+	
C2-	
C3+	
C3-	
C4+	
C4-	
VOUT	

2-time voltage

Vss	
C1+	
C1-	
C2+	
C2-	
C3+	
C3-	
C4+	
C4-	
VOUT	
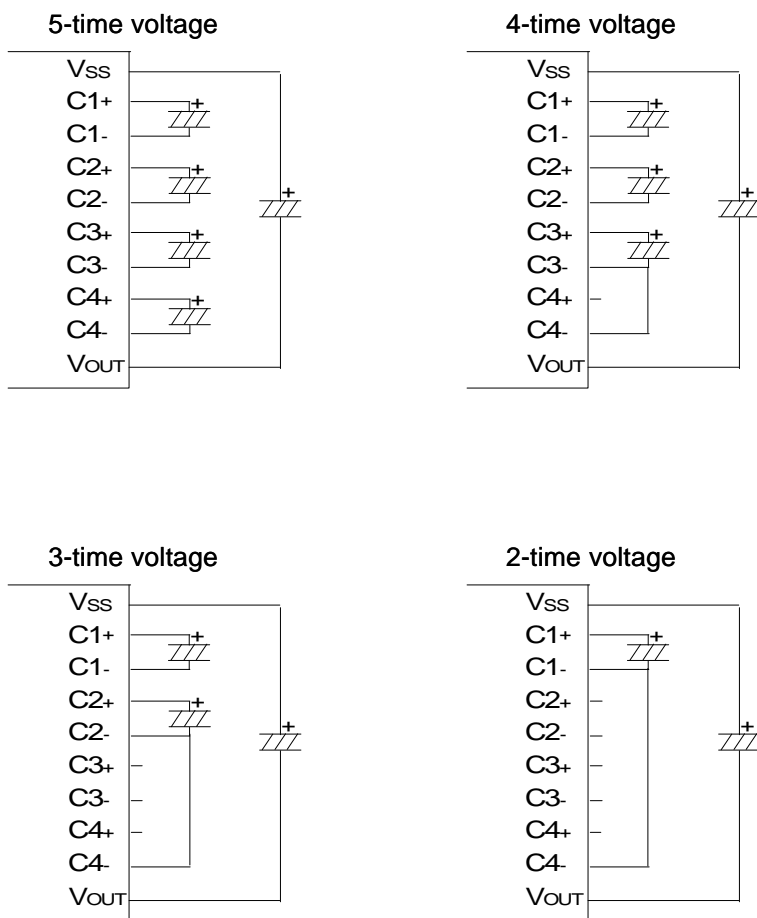
(3-2)Voltage Adjust Circuits

The boosted voltage of V_{OUT} outputs V5 for LCD driving through the voltage adjust circuits. The output voltage of V5 is adjusted by Ra and Rb within the range of $|V5| < |V_{OUT}|$.
The output is calculated by the following formula(1).

$$V_{LCD} = V_{DD}-V5 = (1+Rb/Ra)V_{REG} \qquad (1)$$

The V_{REG} voltage is a reference voltage generated by the built-in bleeder registance. V_{REG} is adjustable by EVR functions (see section 3-3).
For minor adjustment of V5, it is recommended that the Ra and Rb is composed of R2 as variable resistor and R1 and R3 as fixed resistors, constant should be connected to V_{DD} terminal,VR and V5 ,as shown below.
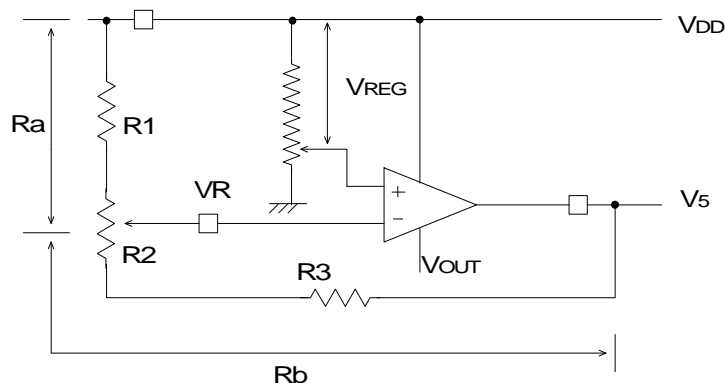
Fig. 4

< Design example for R1, R2 and R3 /Reference >
•R1+R2+R3=6MΩ
 (Determind by the current between V_{DD}-V5)
•Variable voltage range by the R2. -7V to -11V ($V_{LCD}=V_{DD}$-V5 : 10V to 12V)
 (Determind by the LCD electrical characteristics)
•VREG=3V
 (In case of V_{DD}=3V and EVR=FFh)

R1,R2 and R3 are calculated by above conditions and the fomula of (1) to below;
 R1=1.5MΩ
 R2=0.3MΩ
 R3=4.2MΩ

Note) V5 voltage is generated referencing with VREG voltage beased on the supply voltage (V_{DD} and V_{SS}) as shown in above figure. Therefore, V_{LCD} (V_{DD}-V5) is affected including the gain (Rb/Ra) by the fluctuation of V_{REG} voltage based on the supply voltage. The power supply voltage should be stabilized for V5 stable operation.

(3-3) Contrast Adjustment by the EVR function

The EVR selects the V_{REG} voltage out of the following 201 conditions by setting 8-bit data into the EVR register. With the EVR function, V_{REG} is controlled, and the LCD display contrast is adjusted. The EVR controls the voltage of V_{REG} by instruction and changes the voltage of V5.

A step with EVR is set like table shown below.

37H to 4FH available for use. If keeping 3% precision, sets EVR over 4FH.

EVR register		V_{REG}[V]	V_{LCD}
3FH	(0,0,1,1,0,1,1,1)	(100/300) x (V_{DD}-V_{SS})	Low
:	:	:	:
4FH	(0,1,0,0,1,1,1,1)	(124/300) x (V_{DD}-V_{SS})	:
:	:	:	:
:	:	:	:
FDH	(1,1,1,1,1,1,0,1)	(298/300) x (V_{DD}-V_{SS})	:
FEH	(1,1,1,1,1,1,1,0)	(299/300) x (V_{DD}-V_{SS})	:
FFH	(1,1,1,1,1,1,1,1)	(300/300) x (V_{DD}-V_{SS})	High

In use of the EVR function, the voltage adjustment circuit must turn on by the power supply instruction.

● Adjustable range of the LCD driving voltage by EVR function

The adjustable range is decided by the power supply voltage V_{DD} and the ratio of external resistors Ra and Rb.

[Design example for the adjustable range / Reference]

- Condition　V_{DD}=3.0V, V_{SS}=0V

　　　　　Ra=1MΩ, Rb=4MΩ　(Ra:Rb=1:4)

The adjustable range and the step voltage are calculated as follows in the above condition.

　　In case of setting 4FH in the EVR register,

　V_{LCD}　= ((Ra+Rb)/Ra)V_{REG}

　　　　= (5/1) x [(124/300) x 3.0]

　　　　= 6.2V

　　In case of setting FFH in the EVR register,

　V_{LCD}　= ((Ra+Rb)/Ra)V_{REG}

　　　　= (5/1) x [(300/300) x 3.0]

　　　　= 15.0V

	Min.4FH		Max.FFH
Adjustable Range	6.2	- - - - - - - - - - - - - - - - - -	15.0　[V]
Step Voltagre		50	[mV]

* In case of V_{DD}=3V

(3-4) LCD Driving Voltage Generation Circuits

The LCD driving bias voltage of V1,V2,V3,V4 are generated by dividing the V5 voltage with the internal bleeder resistance and is supplied to the LCD driving circuits after the impedence conversion by the voltage follower.
As shown in Figure 5, five external capacitors are required to connect to each LCD driving voltage terminal for voltage stabilization. The value of capacitors (C5 to C9) should be determined after the actual LCD panel display evaluation.

Using the internal Power Supply

Using the external Power Supply
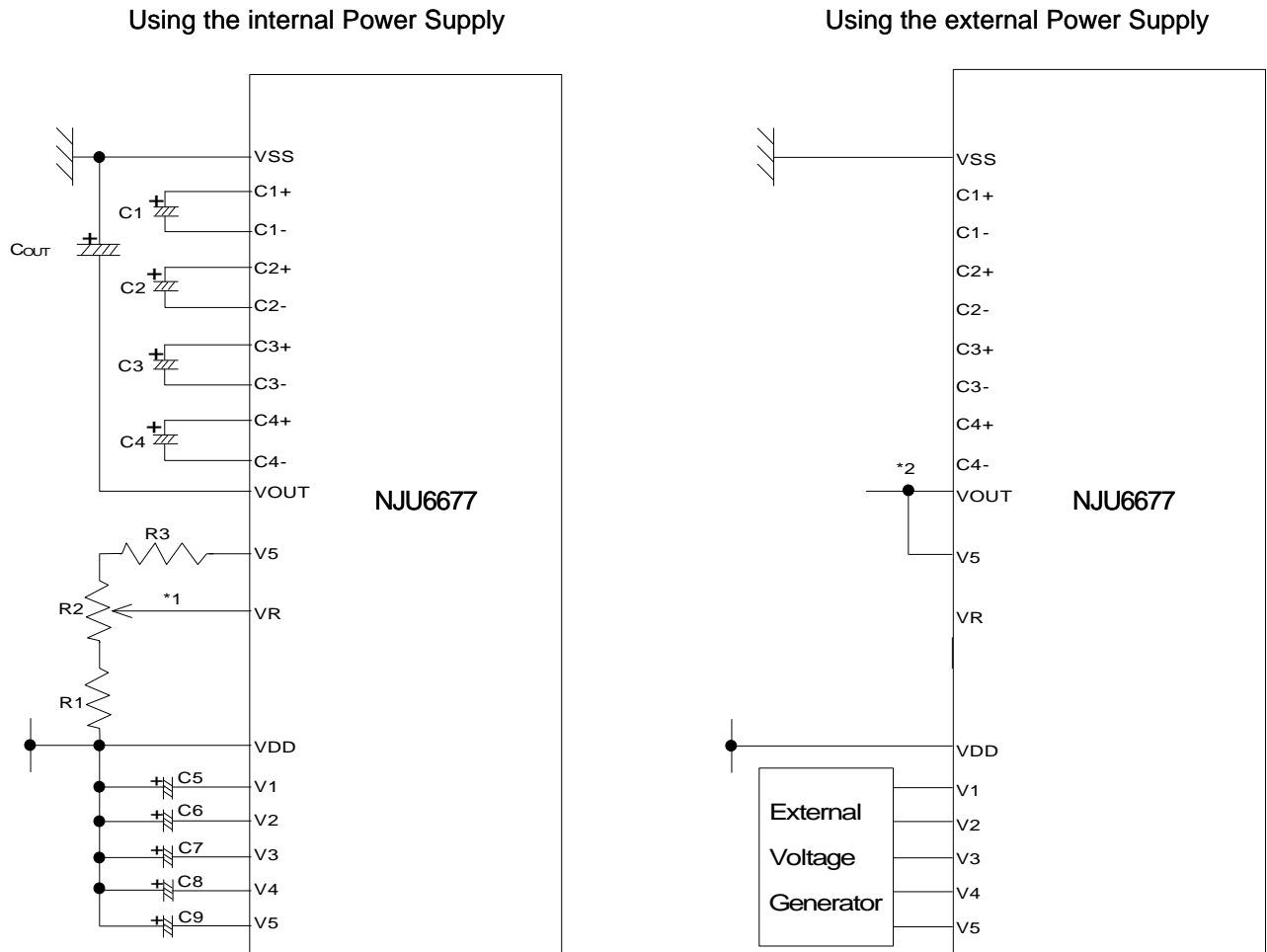
Reference set up value $V_{LCD}=V_{DD}-V5 = 10$ to $12V$

C_OUT	to 1uF
C1 to C4, C9	to 1uF
C5 to C8	0.1 to 0.47uF
R1	1.5MΩ
R2	0.3MΩ
R3	4.2MΩ

Fig.5

*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.
*2 Following connection of V_OUT is required when external power supply using.
    When V_SS > V5 --- V_OUT=V5
    When V_SS ≤ V5 --- V_OUT=V_SS

(4) MPU Interface

(4-1) Interface type selection

Two MPU interface types are available in the **NJU6677**: by 1) 8-bit bi-directional data bus (D7 to D0), 2) serial data input (SI:D7). The interface type (the 8 bit parallel or serial interface) is determined by the condition of the P/S terminals connecting to "H" or "L" level as shown in Table 5. In case of the serial interface, neither the status read-out nor the RAM data read-out operation is allowed.

Table 5

P/S	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D7	D6	D0 to D5
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D7	D6	D0 to D5
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	Hi-Z

Parallel Interface

The **NJU6677** interfaces the 68- or 80-type MPU directly if the parallel interface (P/S="H") is selected.
The 68-type or 80-type MPU is selected by connecting the SEL68 terminal to "H" or "L" as shown in table 6.

Table 6

SEL68	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
H	68 type MPU	$\overline{CS}$	A0	E	R/W	D0 to D7
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

(4-2) Discrimination of Data Bus Signal

The **NJU6677** discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD},\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
H	H	L	H	Read Display Data
H	L	H	L	Write Display Data
L	H	L	H	Status Read
L	L	H	L	Write into the Register(Instruction)

(4-3) Serial Interface.(P/S="L")

The serial interface of the **NJU6677** consists of the 8-bit shift register and 3-bit counter. In case the chip is selected ($\overline{CS}$=L), the input to D7(SI) and D6(SCL) becomes available, and in case that the chip isn't selected, the shift register and the counter are reset to the initial condition.
The data input from the terminal(SI) is MSB first like as the order of D7, D6, ●●●D0 by a serial interface, it is entered into with rise edge of serial clock(SCL). The data converted into parallel data of 8-bit with the rise edge of 8th serial clock and processed.
It discriminates display data or instructions by A0 input terminal. A0 is read with rise edge of (8 X n)th of serial clock (SCL), it is recognized display data by A0=H" and instruction by A0="L". A0 input is read in the rise edge of (8 X n)th of serial clock (SCL) after chip select and distinguished.
However,in case of RES="H" to "L" or $\overline{CS}$="L" to "H" with trasfered data does not fill 8 bit, attention is necessary because it will processed as there was command input. Always, input the data of (8 X n) style.
The SCL signal must be careful of the termination reflection by the wiring length and the external noise and confirmation by the actual machine is recommended by it.
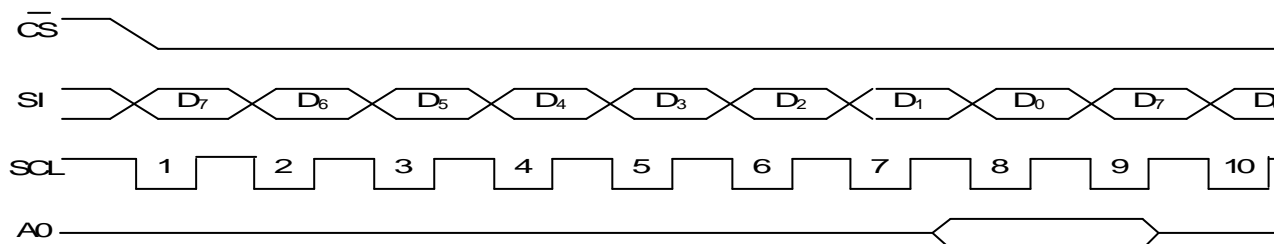

Fig. 6

(4-4) Access to the Display Data RAM and Internal Register.

The **NJU6677** transfers data to the CPU through the bus holder with the internal data bus.

In case of reading out the display data contents in the DD RAM, the data which was read in the first data read cycle (= the dummy read) is memorized in the bus holder. Then the data is read out to the system bus from the bus holder in the next data read cycle. Also, In case that the MPU writes into DD RAM, the data is temporarily stored in the bus holder and is then written into DD RAM by the next data write cycle.

Therefore, the limitation of the access to **NJU6677** from MPU side is not access time (t_{ACC},t_{DS}) of Display Data RAM and the cycle time becomes dominant. With this, speed-up of the data transfer with the MPU becomes possible. In case of cycle time isn't met, the MPU inserts NOP operation only and becomes an equivalent to an execution of wait operation on the sutisfy condition in MPU.

When setting an address, the data of the specified address isn't output immediately by the read operation after setting an address, and the data of the specified address is output at the the 2nd data read operation. Therefore, the dummy read is always necessary once after the address set and the write cycle. (See Fig. 7)

The exsample of Read Modify Write operaion is mentioned in (2-1)Instruction –(q)The sequence of Inverse Display.
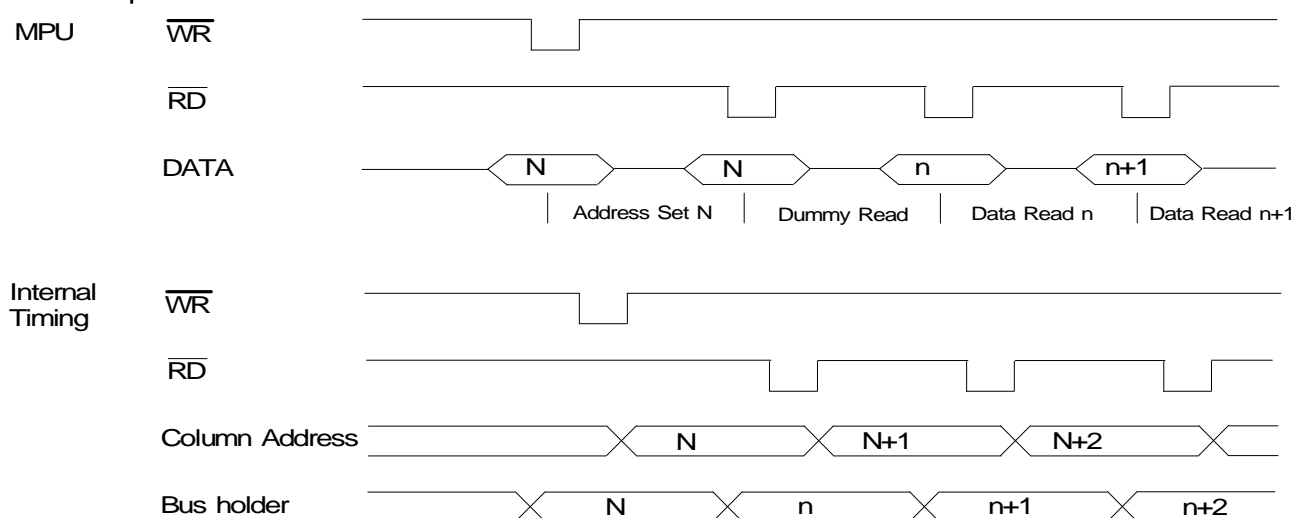
● Write Operation
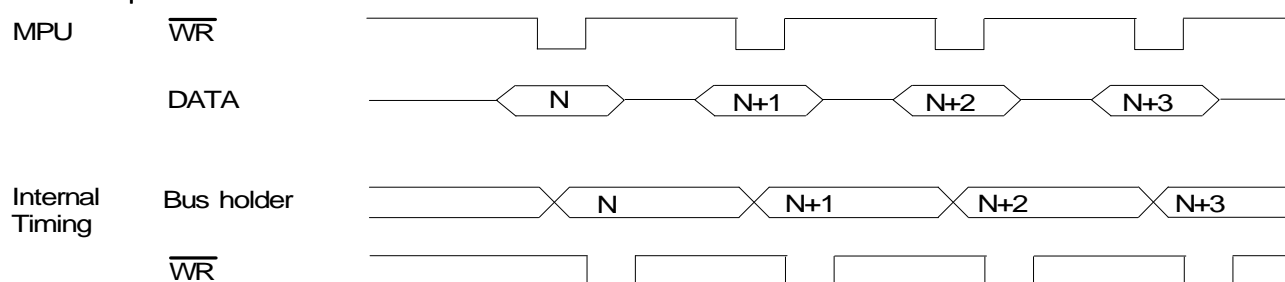
● Read Operation

Fig.7

(4-6) Chip Select

$\overline{CS}$ is the Chip Select terminal. In case of $\overline{CS}$="L", the interface with MPU is available.

In case of $\overline{CS}$="H" (Chip is not selected), the terminals of D_0 to D_7 are high impedance and A0, $\overline{RD}$, $\overline{WR}$, D_7(SI) and D_6(SCL) inputs are ignored. If the serial interface is selected when $\overline{CS}$="H", the shift register and the counter for the serial interface are reset.

However, the reset signal is always input and executed in any conditions of $\overline{CS}$.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage(1)	V_{DD}	-0.3 to +5.0	V
Supply Voltage(2)	V_5, V_{OUT}	V_{DD}-18.0 to V_{DD}+0.3	V
Supply Voltage(3)	V_1,V_2,V_3,V_4	V_5 to V_{DD}+0.3	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3 .	V
Operating Temperature	T_{opr}	-30 to +80	°C
Strage temperature	T_{stg}	-55 to +125	°C
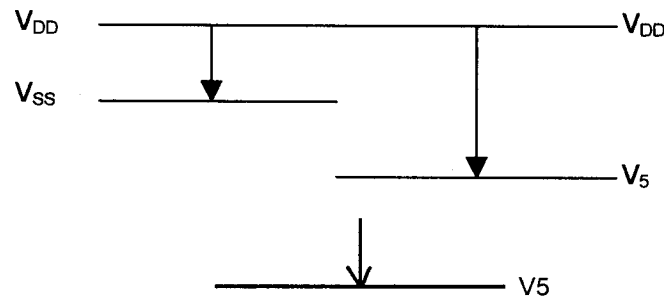
Note 1) All voltage values are specified as Vss=0V.
Note 2) The relation of $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 > VOUT; V_{DD} > Vss \geq V_{OUT}$ must be maintained.
In case of inputting external LCD driving voltage , the LCD drive voltage should start supplying to
NJU6677 at the mean time of turning on V_{DD} power supply or after turned on V_{DD} .
In use of the voltage boost circuit, the condition that the supply voltage: $18.0V \geq V_{DD}-V_{OUT}$ is necessary.
Note 3) If the LSI are used on condition beyond the absolute maximum rating, the LSI may be destroyed.
Using LSI within electrical characteristics is strongly recommended for normal operation.
Use beyond the erectric characteristics conditions will cause malfunction and poor reliability.
Note 4) Decoupling capacitor should be connected between V_{DD} and V_{ss} due to the stabilized operation for the
voltage converter.

NJU6677

■ DC Electrical Characteristics

$(V_{DD}=2.7$ to $3.6V$, $V_{SS}=0V$, $Ta=-30$ to $80°C)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating voltage (1)	V_{DD}		2.5		3.3	V	5
Operating voltage(2)	V_5		$V_{DD}-18.0$		$V_{DD}-6.0$	V	6
	V_1,V_2	$V_{LCD}=V_{DD}-V_5$	$V_{DD}-0.5V_{LCD}$		V_{DD}		
	V_3,V_4		V_5		$V_{DD}-0.5V_{LCD}$		
"H" level input voltage	V_{IHC1}	A0, D_0 to D_7, $\overline{RD}$, $\overline{WR}$, $\overline{RES}$, $\overline{CS}$, P/S, SEL68 Terminals	$0.8V_{DD}$		V_{DD}	V	
"L" level input voltage	V_{ILC1}		V_{SS}		$0.2V_{DD}$		
"H" level output voltage	V_{OHC11}	D_0 to D_7 Terminal, $I_{OH}=-0.5mA$	$0.8V_{DD}$		V_{DD}	V	
"L" level output voltage	V_{OLC11}	$I_{OL}=0.5mA$	V_{SS}		$0.2V_{DD}$		
Input Leagage Current	I_{LIO}	All input terminals	-1.0		1.0	μA	
Driver On-resistance	R_{ON1}	$Ta=25°C$, $V_{LCD}=15.0V$		2.0	3.0	kΩ	7
	R_{ON2}	$Ta=25°C$, $V_{LCD}=8.0V$		3.0	4.5		
Stand-by Current	I_{DDQ}	During Power Save Mode		0.05	5.0	μA	8
Operating Current	I_{DD12}	Display $V_{LCD}=15.0V$		15	40	μA	8
	I_{DD21}	Accessing $f_{CYC}=200kHz$		125	250		9
Input Terminal Capacitance	C_{IN}	$Ta=25°C$ A0, D_0 to D_7, $\overline{RD}$, $\overline{WR}$, $\overline{RES}$, $\overline{CS}$, P/S, SEL68, T_1, T_2 Terminals		10.0		pF	10
Oscillation Frequency	f_{OSC}	$V_{DD}=3.0V$ Ta $=25°C$	22.0	26.8	31.6	kHz	
Reset Time	t_R	$\overline{RES}$ terminal	1.0			μs	11
Reset "L" level pulse Width	t_{RW}	$\overline{RES}$ terminal	10.0			μs	12

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Voltage booster	Output voltage	V_{OUT1}	5-times boost, $V_{DD}=3.0V$	$V_{DD}-15.0$		$V_{DD}-14.5$	V	
	On-resistance	R_{TRI}	5-times boost, $V_{DD}=3.0V$, $C_{OUT}=1.0\mu F$		2000	4000	Ω	
	Adjustment range LCD driving voltage	V_{OUT2}	Voltage boost operation "OFF"	$V_{DD}-18.0$		$V_{DD}-6.0$	V	13
	Voltage Follower	V_5	Voltage adjustment circuit "OFF"	$V_{DD}-18.0$		$V_{DD}-6.0$	V	
	Operating Current	I_{OUT1}	$V_{DD}=3V$, $V_{LCD}=12V$ COM/SEG terminals Open No Access		160	320	μA	14
		I_{OUT2}			35	70		
		I_{OUT3}	Display Checkred pattern.		25	50		
	Voltage Regulator	$V_{REG\%}$	$V_{DD}=3.0V$; Ta $=25°C$, $V_{REG}=4F$ to FF_H			3.0	%	

Note 5) Although the **NJU6677** can operate in wide range of the operating voltage, it shall not be guaranteed in a sudden voltage fluctuation during the access with MPU.

Note 6) The operating voltage when using external power supply.

Note 7) R_{ON} is the resistance values in supplying 0.1V voltage-difference beteen power supply terminals (V1,V2,V3,V4) and each output terminals (common/ segment). This is specified within the range of Operating Voltage(2).

Note 8,9) The value of after Driver Output On instruction execution.

Note 8,9) Refers to the current consumption of the IC itself; external power supply is used for the LCD driving. In case of not use internal power supply circuit,meaning current of IC's. LCD driving power supply are external power supply.

Note 8) Applicable in case of not accessing to the MPU.

Note 9) The operating current when writing a vertical stripe pattern on the tcyc. Current consumption during the access is approximately proportional to the access frequency. When not accessed, it consumpts only I_{DD01}

Note 10) Apply to A0, D_0-D_7, $\overline{RD}$,$\overline{WR}$,$\overline{CS}$,$\overline{RES}$,SEL68,P/S,T_1,T_2 terminals.

Note 11) t_R (Reset Time) refers to the reset completion time of the internal circuits from the rise edge of the $\overline{\text{RES}}$ signal.

Note 12) Apply minimum pulse width of the $\overline{\text{RES}}$ signal. To reset, the "L" pulse over t_{RW} shall be input. .

Note 13) The voltage adjustment circuit controls V5 within the range of the voltage follower operating voltage.

Note 14) Each operating current shall be defined as being measured in the following condition.

SYMBOL	Status		Operating Condition				External Voltage Supply (Input terminal)
	T_1	T_2	Internal Oscillator	Voltage Booster	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	L/H	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use(V_{OUT},V5)

MEASUREMENT BLOCK DIAGRAM
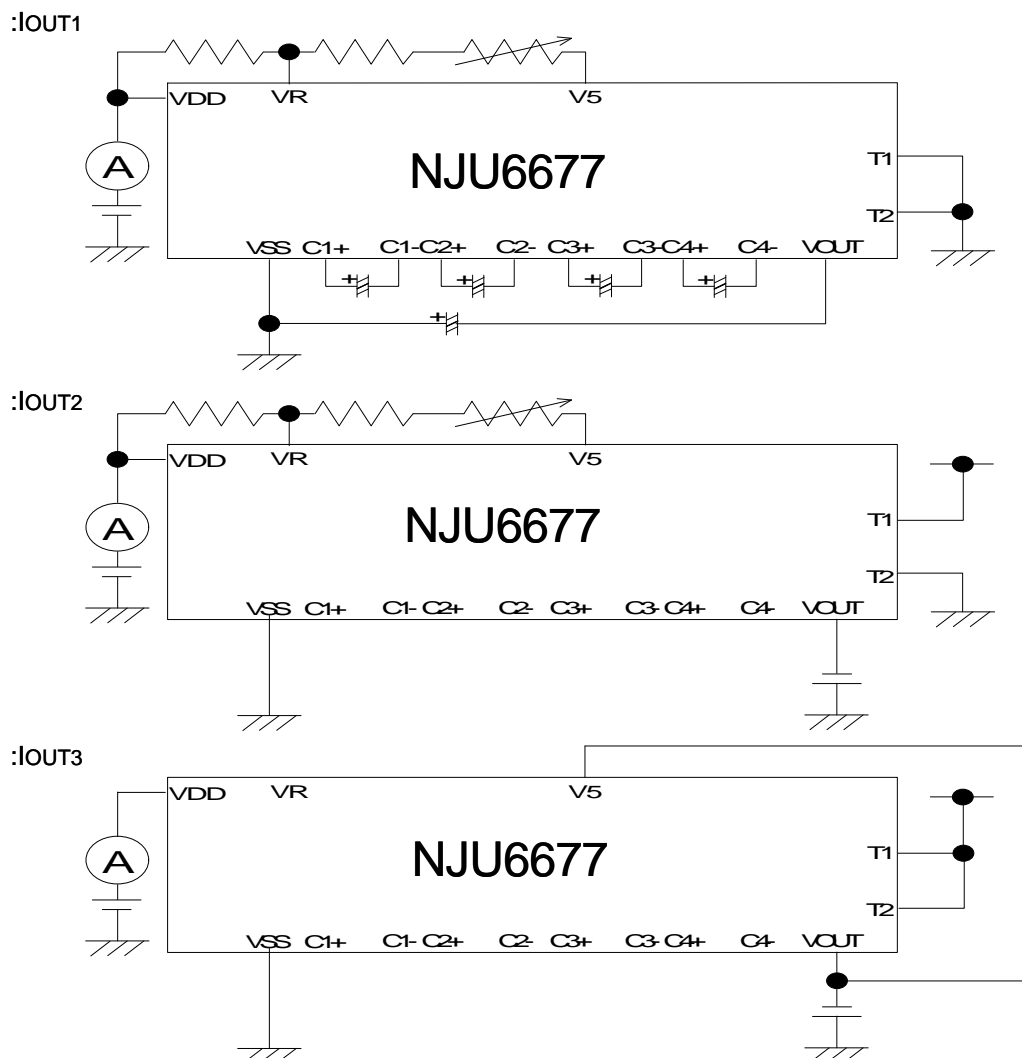
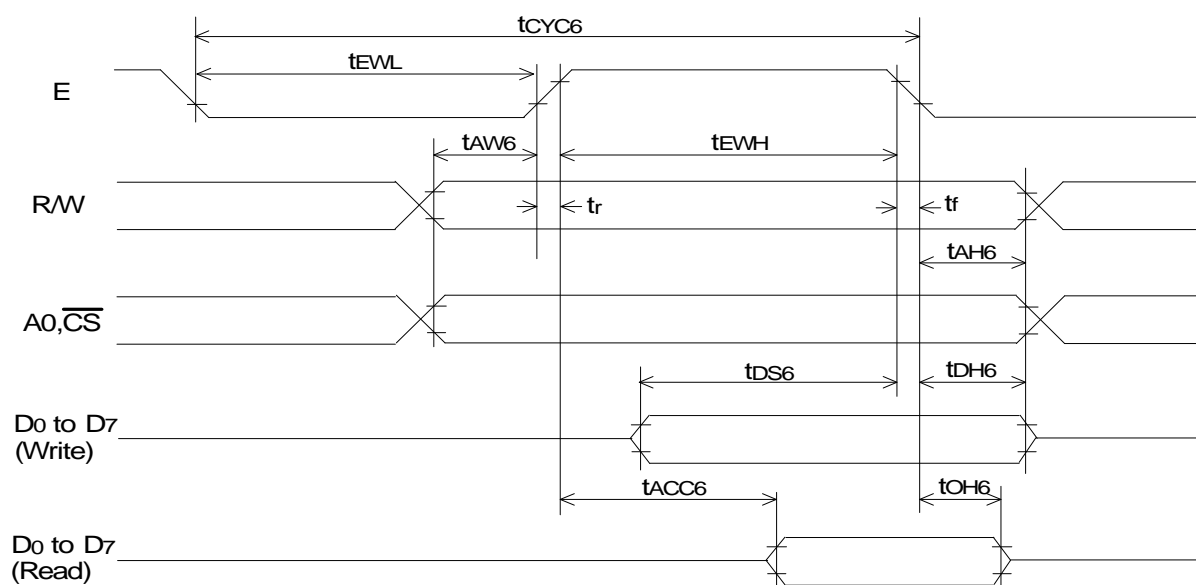■ BUS TIMING CHARACTERISTICS

- Read/Write operation sequence (80 Type MPU)
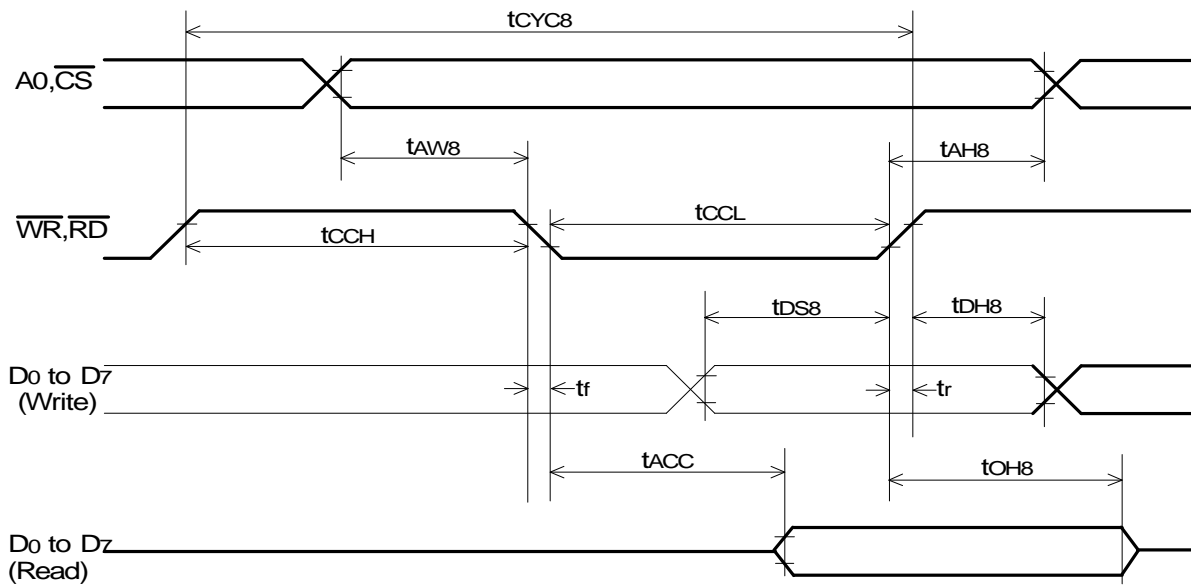
(VDD=2.4V to 3.6V,Ta=-30 to +80°C)

PARAMETER			SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Address Hold Time	A0,$\overline{CS}$ Terminals		tAH8		10			ns
Address Set Up Time			tAW8		0			ns
System Cycle Time	WR	$\overline{WR},\overline{RD}$ Terminals	tCYC8 (W)		220			ns
	RD		tCYC8 (R)		350			ns
Control Pulse Width	WR,"L"		tCCL(W)		50			ns
	RD,"L"		tCCL(R)		200			ns
	WR,"H"		tCCH(W)		160			ns
	RD,"H"		tCCH(R)		160			ns
Data Set Up Time	D0 to D7 Terminals		tDS8		35			ns
Data Hold Time			tDH8		15			ns
$\overline{RD}$ Access Time			tACC8		120		CL=100pF	ns
Output Disable Time			tOH8		50			ns
Rise Time, Fall Time	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, D0 to D7 Terminals		tr,tf		15			ns

Note 15) All timing based on 20% and 80% of VDD voltage level.

- Read/Write operation sequence (68 Type MPU)
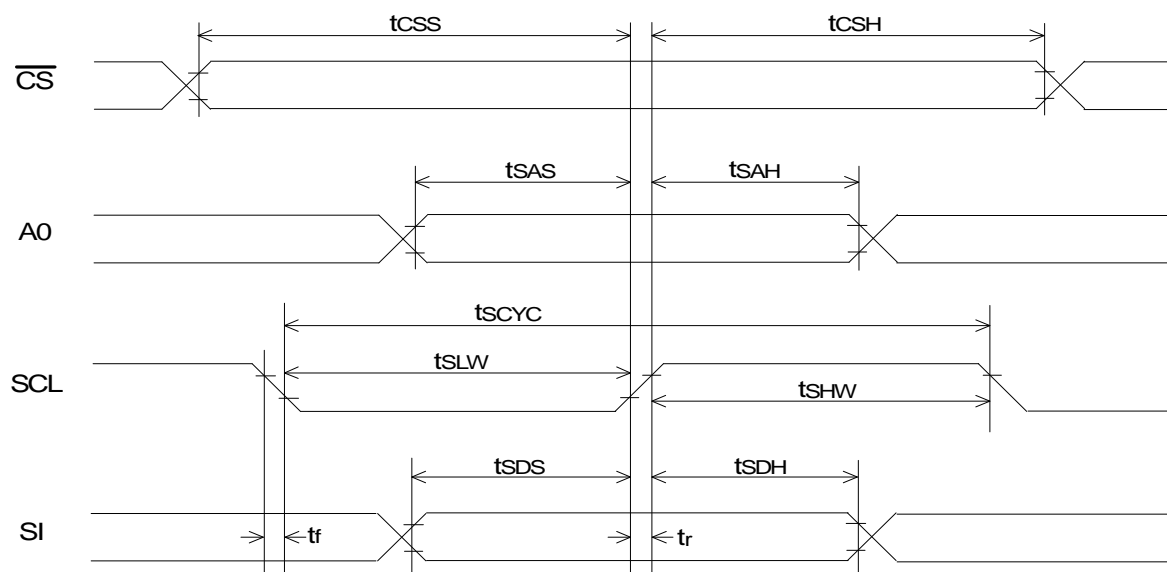

(VDD=2.4V to 3.6V,Ta=-30 to +80°C)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Address Hold Time	A0,$\overline{CS}$,R/W Terminals	tAH6		10			ns
Address Set Up Time		tAW6		0			ns
System Cycle Time(W)		tCYC6(W)		220			ns
System Cycle Time(R)		tCYC6(R)		350			ns
Enable Pulse Width	Read"H"	tEWH		200			ns
	Write"H"			50			ns
	Read"L"	tEWL		160			ns
	Write"L"			160			ns
Data Set Up Time	D0 to D7 Terminals	tDS6		35			ns
Data Hold Time		tDH6		15			ns
Access Time		tACC6		200		CL=100pF	ns
Output Disable Time		tOH6		50			ns
Rise Time, Fall Time	A0, $\overline{CS}$, R/W, E, D0 to D7 Terminals	tr,tf		15			ns

Note 16) All timing are based on 20% and 80% of VDD voltage level.

Note 17) tCYC6 shows the cycle of the E signal in active $\overline{CS}$.
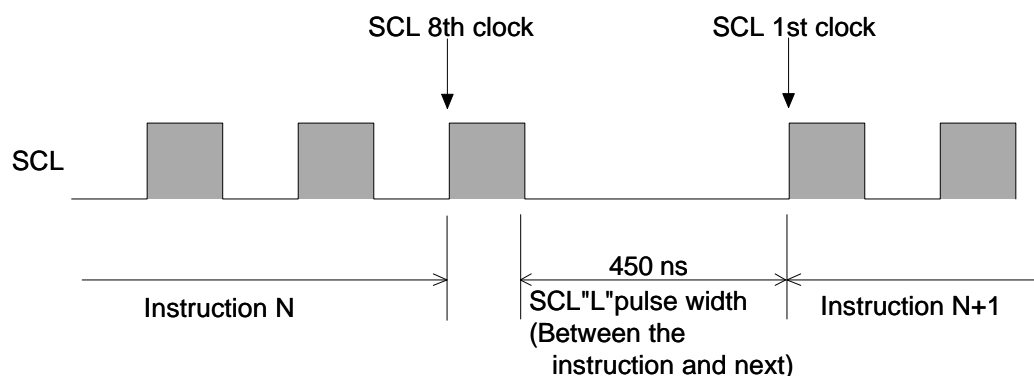
- Write operation sequence (Serial Interface)
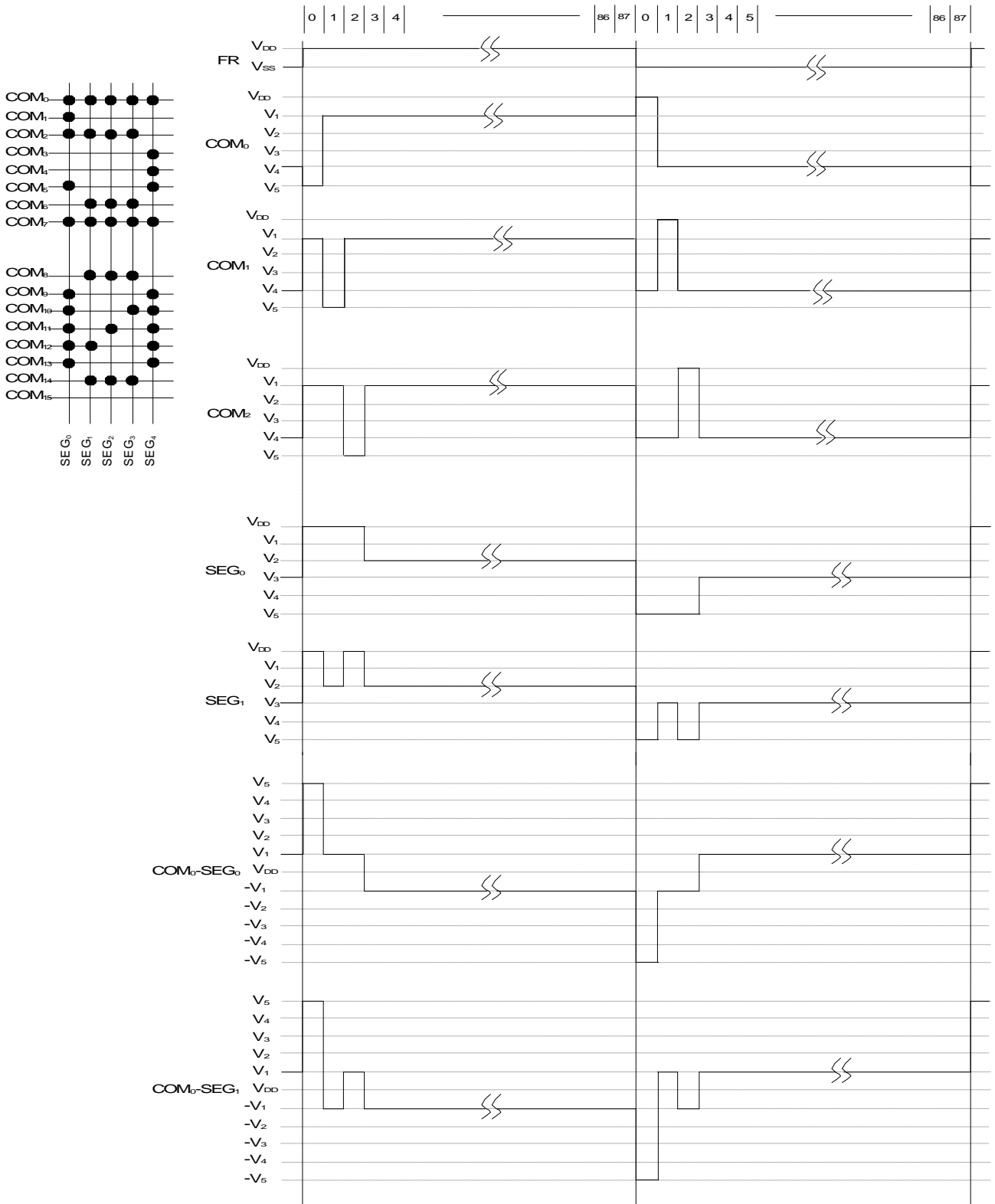

(VDD=2.4V to 3.6V,Ta=-30 to +80°C)

P A R A M E T E R		SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tSCYC		120			ns
SCL "H" pulse width		tSHW		40			ns
SCL "L" pulse width		tSLW		80			ns
Address Set Up Time	A0 Terminal	tSAS		0			ns
Address Hold Time		tSAH		150			ns
Data Set Up Time	SI Terminal	tSDS		25			ns
Data Hold Time		tSDH		10			ns
CS-SCL Time	CS Terminal	tCSS		10			ns
		tCSH		300			ns
Rise Time, Fall Time	SCL, A0, CS, SI Terminals	tr,tf		15			ns

Note 18) All timing are based on 20% and 80% of VDD voltage level.

Note 19) When inputting an instruction continuously, keep 450nS as the cycle of SCL between the instructions as follows

SCL 8th clock

SCL 1st clock

SCL

450 ns

Instruction N

SCL"L"pulse width
(Between the
instruction and next)

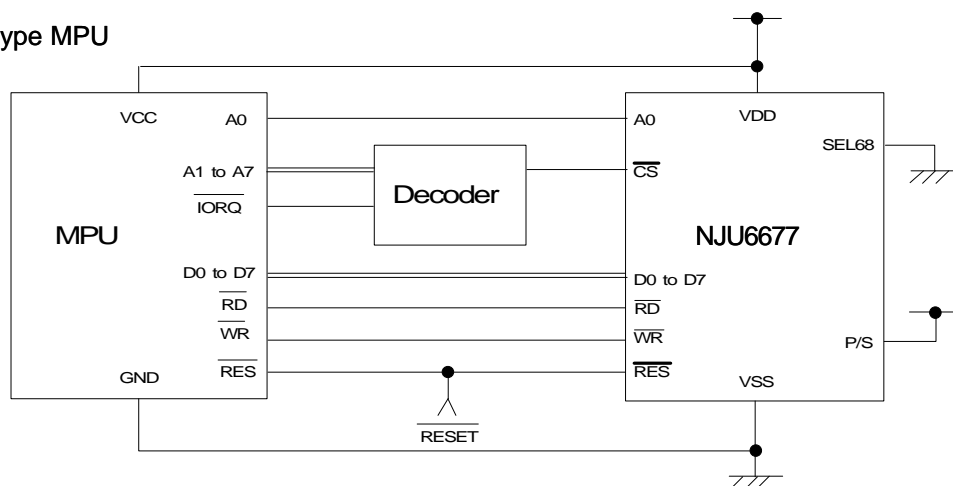Instruction N+1

NJU6677

■ LCD DRIVING WAVEFORM

NJU6677

■ APPLICATION CIRCUIT
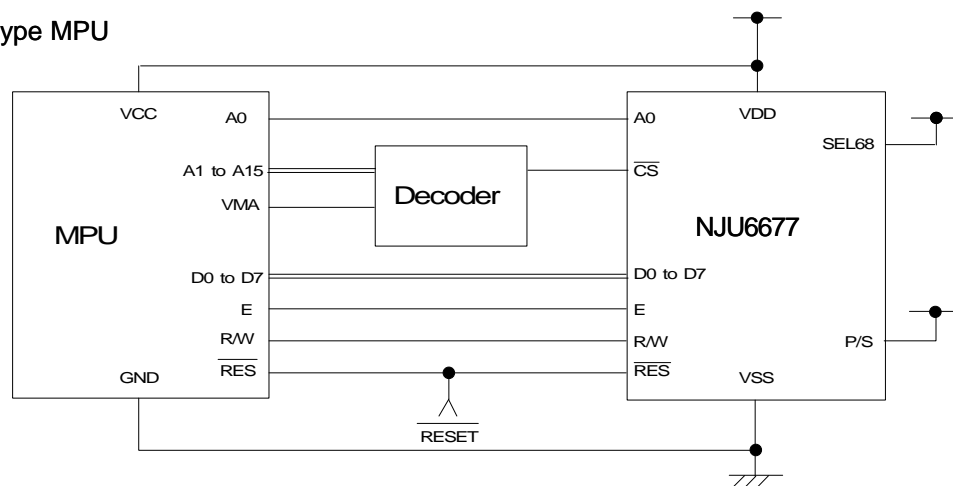
MPU Interface (examples)

The **NJU6677** is connectable to 80-type MPU or 68-type. In use of Serial Interface, it is possible to be controlled by the signal line with the more small being.
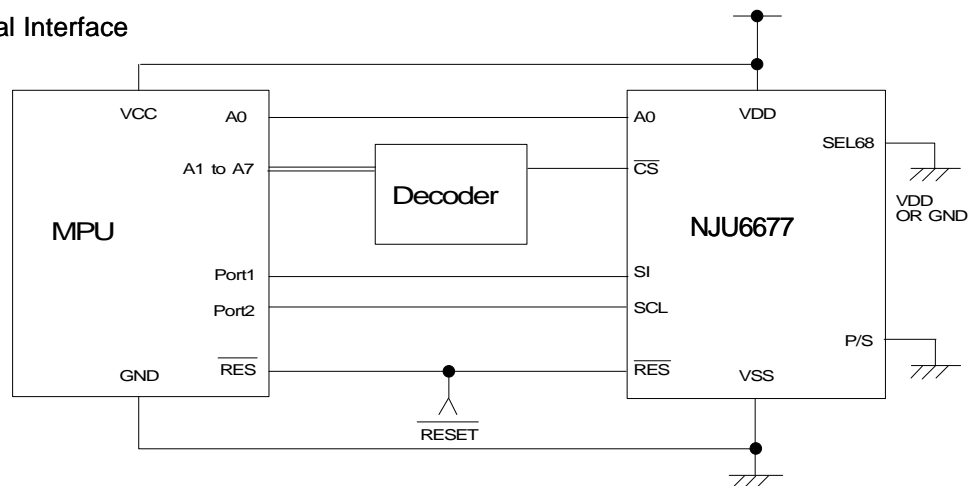
*:SEL68 terminal shall be connected to V_{DD} or V_{SS}.
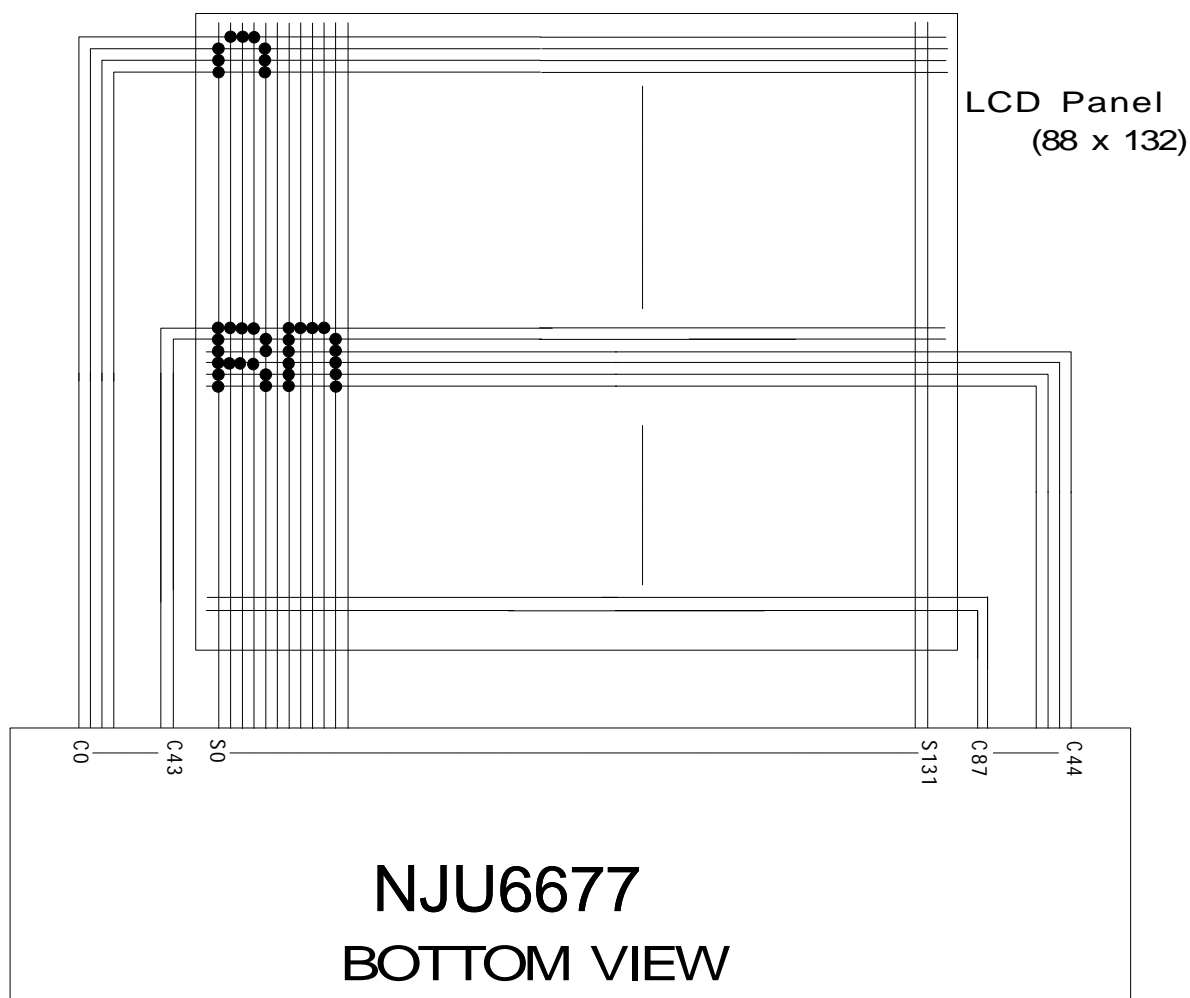
- 80 Type MPU

- 68 Type MPU

- Serial Interface

■ LCD Panel Interface Example

LCD Panel
(88 x 132)

C0 C43 S0   S131 C87 C44

NJU6677
BOTTOM VIEW