APPLICATION NOTE

Broadband impedance matching for S-Band Transistors

AN98029

Philips
Semiconductors

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CONTENTS

1 INTRODUCTION

Due to fact that no accurate model or S-parameters exist which describe RF power transistors, the design of RF power amplifiers is often done in an empirical way. Not only is this method very time consuming, but it also means that it is at least doubtful whether the optimum performance of the transistor is obtained, especially when broadband matching is required. In this paper a method of designing an input and output matching circuit for a broadband power transistor operating in the low S-band (2.7 – 3.1 GHz) is described. The design and evaluation of the transistor is left out in this paper.

2 DESIGN METHOD

The whole design can be separated into the design and evaluation of the input and output circuit. This is done in the same way for both circuits. The following steps can be distinguished:

- Impedance measurement
- Fit impedance data to an appropriate model
- Design of lumped element input and output circuit
- Translation of lumped element to stripline
- Evaluation of stripline circuit with CAD-tools.

In the following each step will be discussed separately.

3 IMPEDANCE MEASUREMENT

The first step is to measure the impedance at nominal output power. This is done by tuning the device with slugtuners at the input and output to maximum output power and minimum reflection at the input with gradually increased input power. In Fig.1 the impedance measurement test set up is depicted.

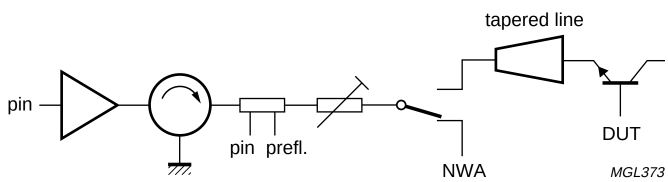

Fig.1 Impedance measurement set up.

In Fig.1 it can be seen that not the actual input impedance is measured, but the source-impedance. The input impedance is the complex conjugated of this source-impedance. This may be done under the assumption that minimum input reflection is achieved when source and load are complex conjugated. For the output the load impedance is directly measured. Also in Fig.1 it can be seen that between tuner and device a tapered line is connected. With this tapered line the relatively low impedance of the devices is transformed to a higher value thus ensuring that with the tuners all required impedance's can be obtained. This is especially required with high power devices where the slugtuners cannot handle a high VSWR. In the network analyzer the S-parameters of the tapered line are stored and the measured data is recalculated for the transformation of the tapered line. During deembedding of the tapered circuit the following errors can be introduced:

- Reference plane is not accurately defined
- Launcher is very thin compared to the lead of the transistor. This introduces a discontinuity (step in width) which can cause a large error.

The errors introduced may be as large as j6 Ω at 3 GHz. The Philips Data Handbook contains values for the input and load impedance of the transistor which are corrected for these errors.

4 FITTING DATA TO MODEL

Although no accurate two-port models exist to describe the transistor completely, simple equivalent one-port models which describe the input and output impedance of the transistor can be used to enable the use of CAD-Tools in the design of the matching circuit. In Fig.2 the model for the input of the transistor based on the internal matching topology is depicted in Fig.3 measured and fitted data are given in the Smith Chart. From the relation $B = \frac{f_0}{Q}$ it can be seen that for a large bandwidth a low Q-transformation at all stages is required. To evaluate this the one-port model proves to be a useful tool. The bandwidth limitations of the intrinsic transistor are dominated by the input rather than by the output. This also can be found in the transistor model. In the model the active die is represented by R_{DIE}. The first (internal) matching stage is formed by the first emitter bondwire (L_{E1}) and the prematch capacitor (C_{PRE}). L_{E2} represents the bondwire connecting die and prematch to the lead. L_P, C_P and L_{PAR} are parasitic elements caused by the header.

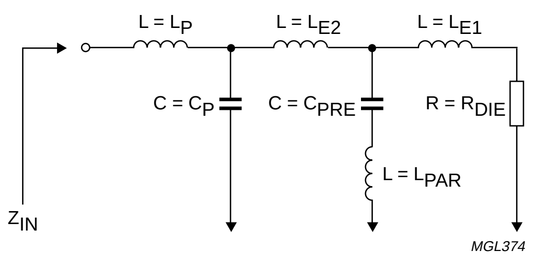

Fig.2 Input equivalent model.

Apart from bandwidth considerations, the location of the resonance frequency of the first matching stage at the input and of the resonance frequency of the internal shunt inductance (inshin) at the output also have a large influence on gain and efficiency. More on this subject can be found in Pitzalis(1)

(1) *"broad-band Microwave Class-C Transistor Amplifiers"*, Pitzalis and Gilson; IEEE Transactions on Microwave Theory and Techniques, November 1973.

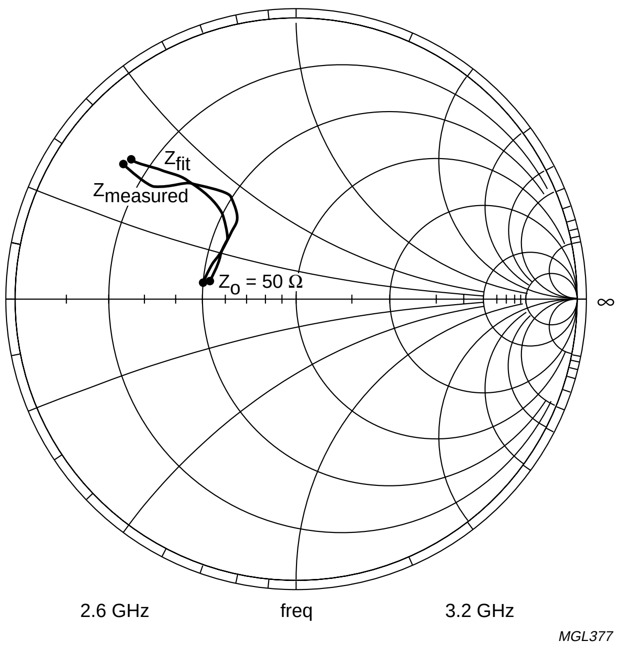

Fig.3 Measured and fitted data.

In Fig.4 the model of the output is given. Here the die is represented by a single resistor in combination with a capacitor which represents the output capacitance of the active die. The die is connected to the lead by means of L_{C1} and L_{C2}. The point of impact of the internal shunt inductance (L_{INS}) determines the ratio between L_{C1} and L_{C2}. C_{DC} is a DC-decoupling capacitor and C_{PAR} is modelling the parasitic capacitance caused by the header.

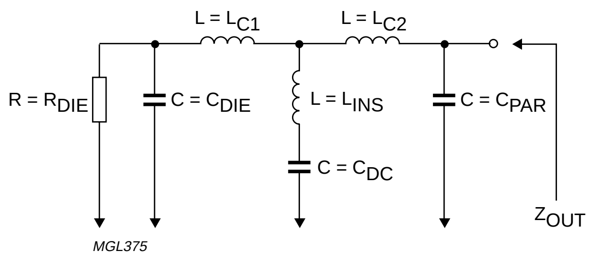

Fig.4 Output model.

A second method in designing the matching circuit is to use the measured data in a dataset. This has the disadvantage that inconsistency in data will have a larger influence than when a model is used.

A second advantage of the use of a model is that this gives the possibility to evaluate the influence of production spread of each parameter on the performance (e.g. Γ_{IN}).

5 LUMPED ELEMENT INPUT AND OUTPUT CIRCUIT

Before designing the input and output circuit with stripline techniques it is preferred to synthesize a low pass lumped element prototype first. The advantage of using a lumped element model first is:

- Optimum solution easier and faster found with CAD-Tools
- Better insight in feasibility of found solution. High inductance are very difficult to realize in stripline techniques. An inductance may also converge to zero (or negative values) indicating that the given low pass structure is not appropriate.

Similar to the requirements for the internal matching network, the external matching circuit (see Fig.5) must also be a low Q design to ensure broadband performance of the device.

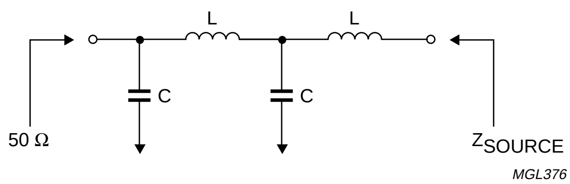

Fig.5 Lumped element model input circuit.

After having found the optimum values for the lumped elements, these can be translated to stripline elements.

This is done by using the basic formula's(1) to find the initial values for stripline circuit which then can be optimized with CAD-tools.

(1) A very good description of microstrip matching networks can be found in: *"Microwave Transistor Amplifiers"*, Guillermo Gonzalez.

6 EVALUATION OF STRIPLINE CIRCUIT

Although stripline models used in CAD-tools such as MDS are fairly accurate, they still have their limitations (such as steps, crosses and substrate thickness). To examine whether these limitations de not mask any significant errors in the design a field simulator can be used (e.g. Momentum). The output of such a simulator is a datafile containing the S-parameters of the stripline circuit. In order to prevent the introduction of additional errors in the simulator output, special attention should be paid to the following:

- Use the appropriate port definition and location of the reference plane. Be aware of any unexpected steps in width at the edge of the simulated circuit.
- Make sure that the MESH is sufficiently small, especially at discontinuities.
- Use a sufficient number of frequency points.

With the combination of simulator output and transistor model an accurate idea of the performance of the transistor in the matching circuit can be obtained without having to go through the time and money consuming process of ordering and assembling printed-circuit boards. When measuring the printed-circuit board with a network analyzer it should be noted that an error can be made due to the difference in width between printed-circuit board and launcher (see Chapter 3). In Fig.6 the input reflection can be seen of the BLS2731-10 in a 50 Ω matching circuit. Both measured and simulated data show a similar curve, only the minimum value is reached at a different frequency. this difference between measured and simulated curve can be explained by the following:

- Small air gaps between reference plane of transistor and edge of printed-circuit boards.
- Impedance data used in the design of the printed-circuit board is from an average device. The measured device may differ from average due to normal production spread.
- Placing components such as DC-blocking.
- Influence bias circuit.
- Connectors not incorporated in simulation.

Also in Fig.6 it can be seen that excellent matching is achieved over the entire frequency band from 2.7 – 3.1 GHz. For the output a similar performance is found.

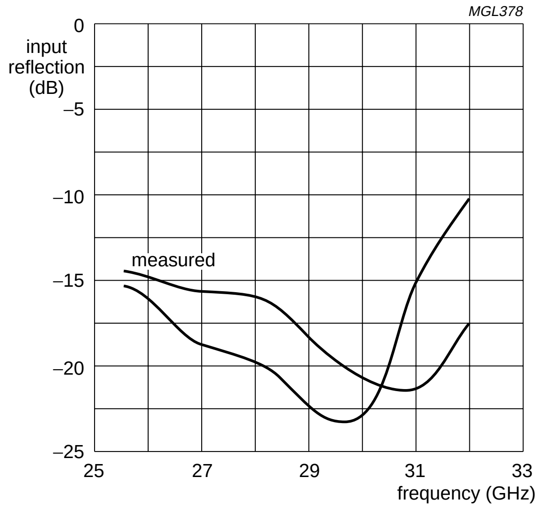

Fig.6 Measured and simulated input reflection of BLS2731-10.

7 CONCLUSIONS

Although the lack of an accurate model for S-band high power transistors would suggest that the use of CAD-tools in the design of matching circuits is impossible, it is shown that with the use of the impedance data from the data handbook and a simple model for the input and output impedance an excellent matching can be achieved. This enables RF-engineers not only to design and evaluate printed-circuit board much faster, but also over a much larger bandwidth.

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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