DATA SHEET

BLF145
HF power MOS transistor

Product specification

September 1992

Philips Semiconductors

PHILIPS

HF power MOS transistor BLF145

FEATURES

- High power gain
- Low noise figure
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for SSB transmitter applications in the HF frequency range. The transistor is encapsulated in a 4-lead, SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange. Matched gate-source voltage (V_{GS}) groups are available on request.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

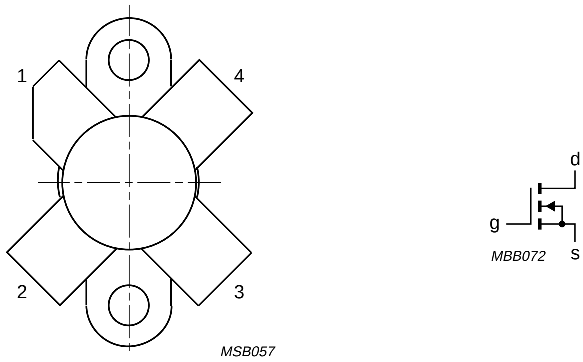


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	P_L (W)	G_p (dB)	η_D (%) (note 1)	d_3 (dB)
SSB, class-A	28	28	1.3	8 (PEP)	> 24	–	< –40
SSB, class-AB	28	28	–	30 (PEP)	typ. 20	typ. 40	typ. –35

Note

1. 2-tone efficiency.

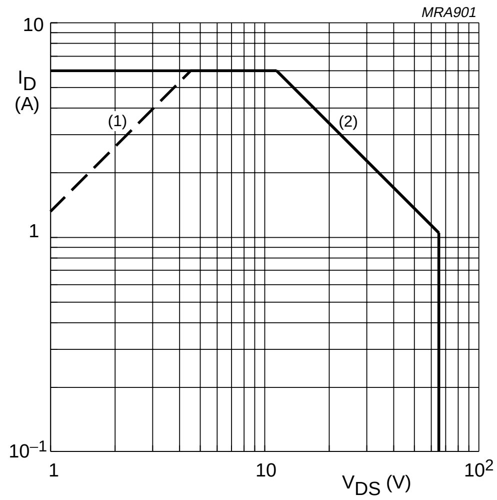
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	drain-source voltage		–	65	V
$\pm V_{GSS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	6	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	68	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

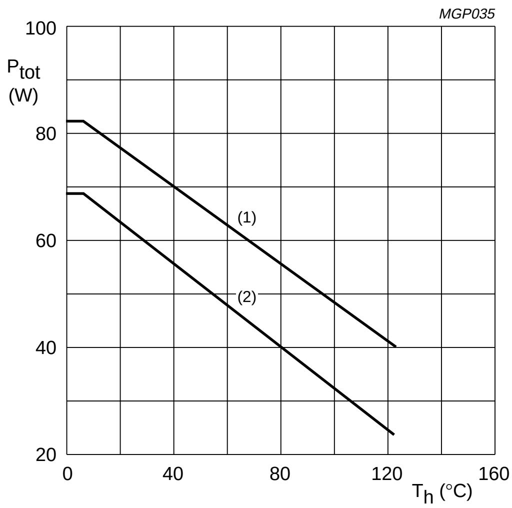
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	2.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



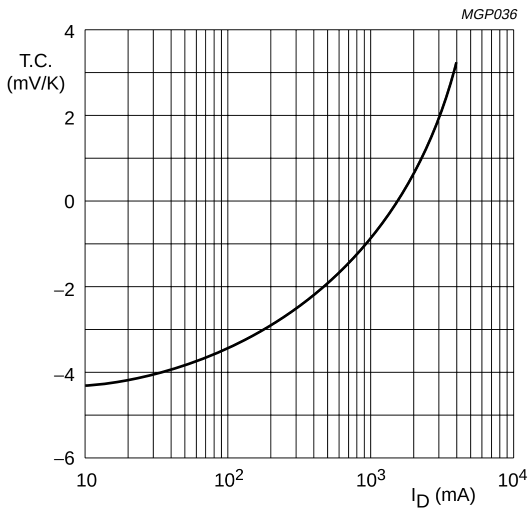
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

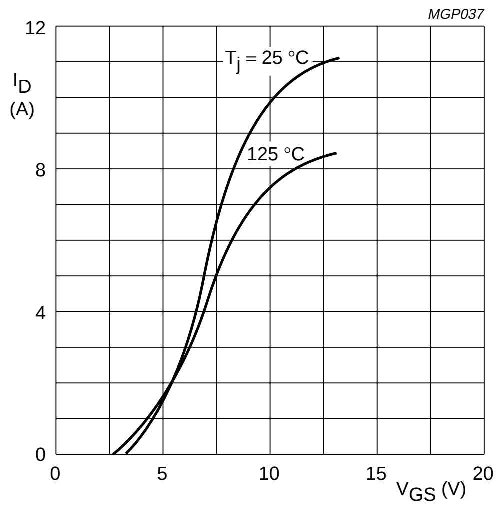
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched devices	I_D = 10 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.5 A; V_{DS} = 10 V	1.2	–	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	0.4	0.75	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	125	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	75	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	7	–	pF



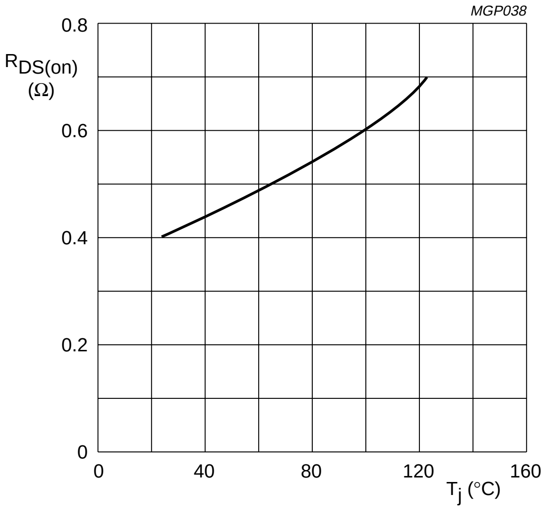
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



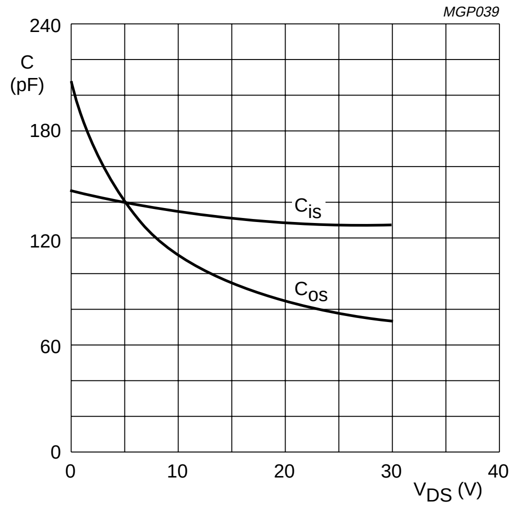
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



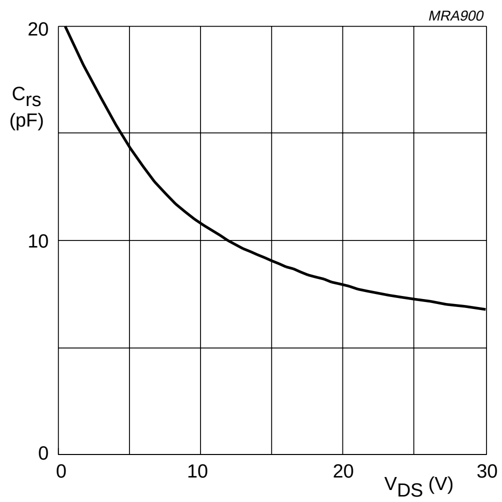
I_D = 1.5 A;
V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-A OPERATION

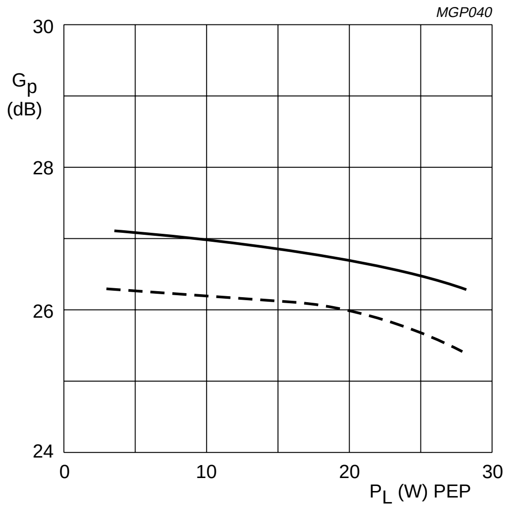
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; R1 = 26 Ω; unless otherwise specified.

RF performance in SSB operation in a common source class-A circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	P_L (W)	G_P (dB)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	Z_L (Ω)
SSB, class-A	28	28	1.3	8 (PEP)	> 24 typ. 27	> –40 typ. –43	< –40 typ. –70	18.4 + j5.2

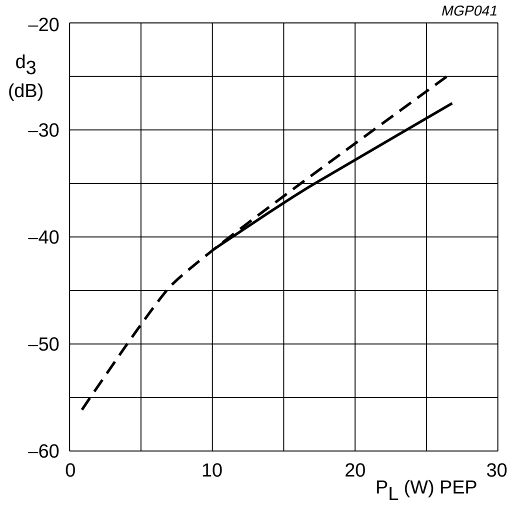
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.



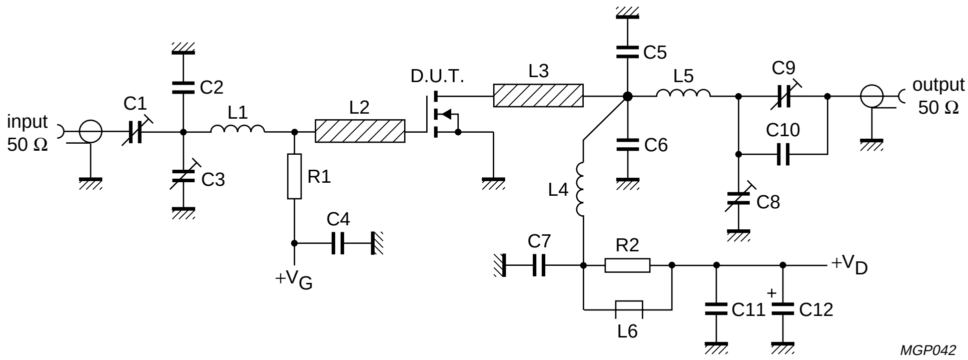
Class-A operation; V_{DS} = 28 V; I_D = 1.3 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.9 Power gain as a function of load power, typical values.



Class-A operation; V_{DS} = 28 V; I_D = 1.3 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.10 Third order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

Fig.11 Test circuit for class-A operation.

List of components (class-A test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C3, C8, C9	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2, C10	multilayer ceramic chip capacitor (note 1)	39 pF		
C4, C7	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C5, C6	multilayer ceramic chip capacitor (note 1)	27 pF		
C11	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C12	electrolytic capacitor	2.2 μF, 63 V		2222 030 38228
L1	12 turns enamelled 0.5 mm copper wire	307 nH	length 8 mm; int. dia. 4 mm	
L2, L3	stripline (note 2)	30 Ω	length 15 × 6 mm	
L4	14 turns enamelled 1 mm copper wire	1039 nH	length 14 mm; int. dia. 9 mm	
L5	9 turns enamelled 1 mm copper wire	305 nH	length 10 mm; int. dia. 6 mm	
L6	grade 3B Ferroxcube wideband HF choke			4312 020 36640
R1	0.25 W metal film resistor	26 Ω		
R2	0.25 W metal film resistor	10 Ω		

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 4.5), thickness $^1/_{16}$ mm.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; R1 = 34 Ω; unless otherwise specified.
RF performance in SSB operation in a common source class-AB circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	Z_L (Ω)
SSB, class-AB	28	28	0.25	30 (PEP)	typ. 20	typ. 40	typ. –35	typ. –40	8.9 + j1.0

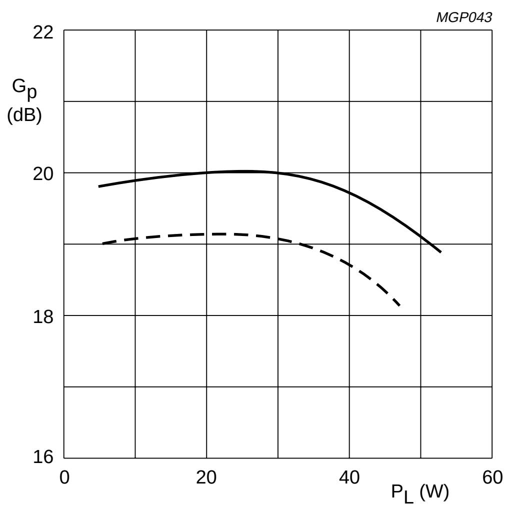
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.

Ruggedness in class-AB operation

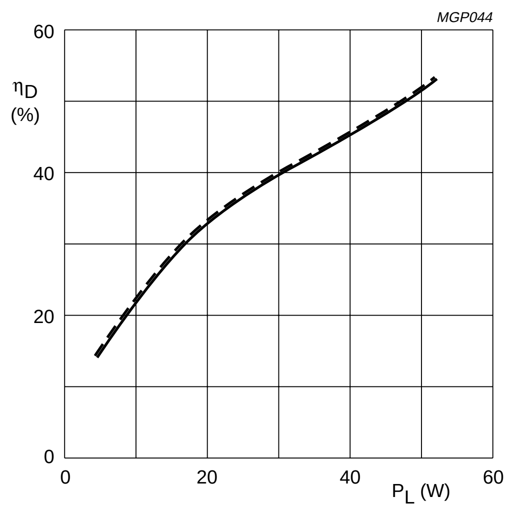
The BLF145 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases at P_L = 30 W single tone under the following conditions:

V_{DS} = 28 V; f = 28 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W at rated load power.



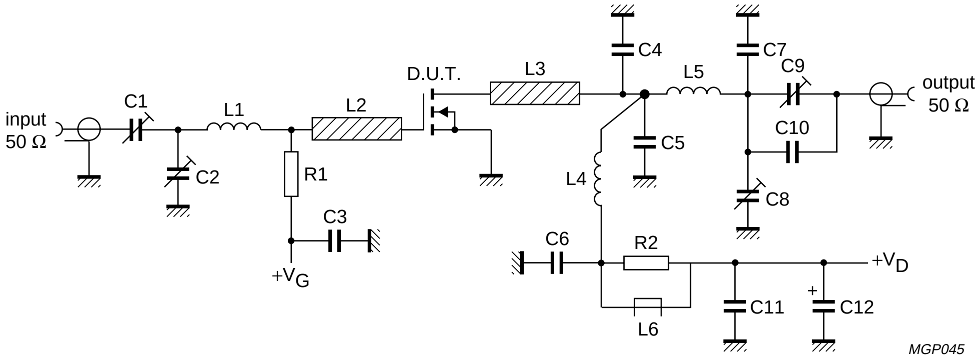
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
$R_{th\ mb-h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.12 Power gain as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
$R_{th\ mb-h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.13 Two tone efficiency as a function of load power, typical values.



f = 28 MHz.

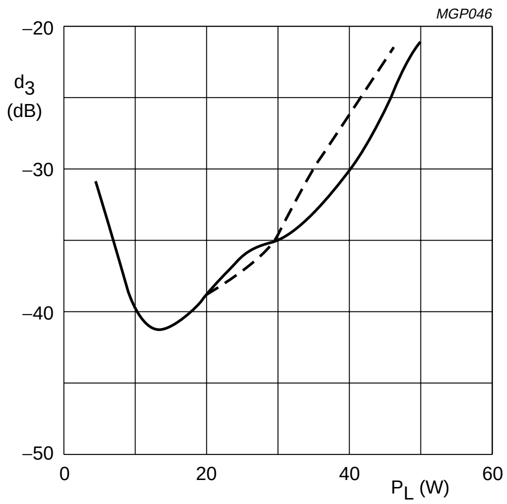
Fig.14 Test circuit for class-AB operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	film dielectric trimmer	5 to 60 pF		2222 809 07011
C3, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C4, C5	multilayer ceramic chip capacitor (note 1)	27 pF		
C7, C10	multilayer ceramic chip capacitor (note 1)	39 pF		
C8, C9	film dielectric trimmer	7 to 100 pF		2222 809 07015
C11	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C12	electrolytic capacitor	2.2 µF, 63 V		2222 030 38228
L1	13 turns enamelled 0.5 mm copper wire	415 nH	length 10 mm; int. dia. 5 mm	
L2, L3	stripline (note 2)	30 Ω	length 15 × 6 mm	
L4	10 turns enamelled 1 mm copper wire	390 nH	length 13 mm; int. dia. 7 mm	
L5	9 turns enamelled 1 mm copper wire	245 nH	length 10 mm; int. dia. 5 mm	
L6	grade 3B Ferroxcube wideband HF choke			4312 020 36640
R1	0.5 W metal film resistor	34 Ω		
R2	0.25 W metal film resistor	10 Ω		

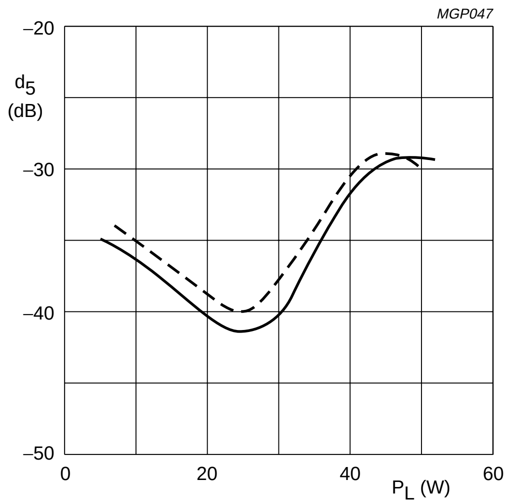
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 4.5), thickness $^1/_{16}$ mm.



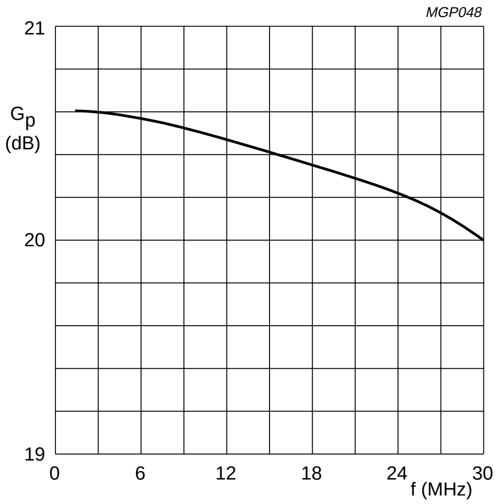
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.15 Third order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.16 Fifth order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W;
R_1 = 34 Ω; Z_L = 8.9 + j1 Ω.

Fig.17 Power gain as a function of frequency, typical values.

Table 1

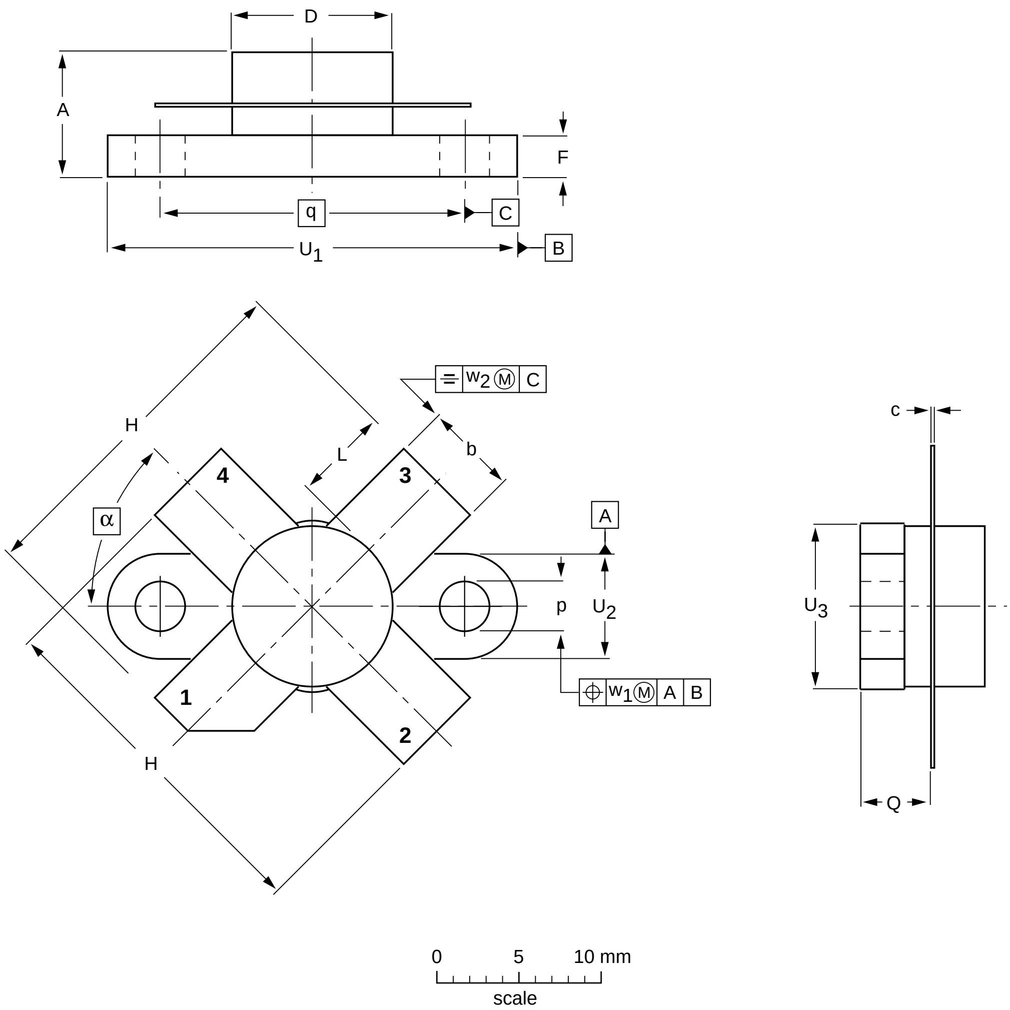
Input impedance as a function of frequency
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
P_L = 30 W; T_h = 25 °C;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; R1 = 34 Ω; Z_L = 8.9 + j1 Ω.

f (MHz)	Z_i (Ω)
1.5	32.9 – j2.2
3.0	32.4 – j4.3
6.0	30.7 – j8.1
10	27.4 – j11.9
15	32.9 – j14.6
20	18.5 – j15.4
25	15.1 – j15.3
30	12.5 – j14.6

HF power MOS transistor BLF145

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads **SOT123A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	F	H	L	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.63 9.42	2.72 2.31	20.71 19.93	5.61 5.16	3.33 3.04	4.63 4.11	18.42	25.15 24.38	6.61 6.09	9.78 9.39	0.51	1.02	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.397 0.371	0.107 0.091	0.815 0.785	0.221 0.203	0.131 0.120	0.182 0.162	0.725	0.99 0.96	0.26 0.24	0.385 0.370	0.02	0.04	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT123A						97-06-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.