

# DATA SHEET

## **BLF242** HF/VHF power MOS transistor

Product specification

September 1992

# HF/VHF power MOS transistor

# BLF242

## FEATURES

- High power gain
- Low noise
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

## DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for professional transmitter applications in the HF/VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

## PIN CONFIGURATION

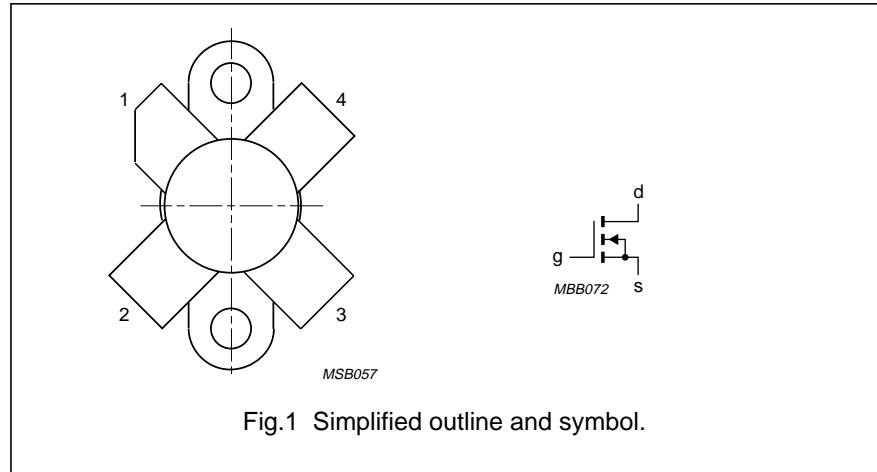


Fig.1 Simplified outline and symbol.

## PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

## CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

## WARNING

**Product and environmental safety - toxic materials**

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

## QUICK REFERENCE DATA

RF performance at  $T_h = 25\text{ °C}$  in a common source test circuit.

MODE OF OPERATION	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)
CW, class-B	175	28	5	> 13 typ. 16	> 50 typ. 60

# HF/VHF power MOS transistor

# BLF242

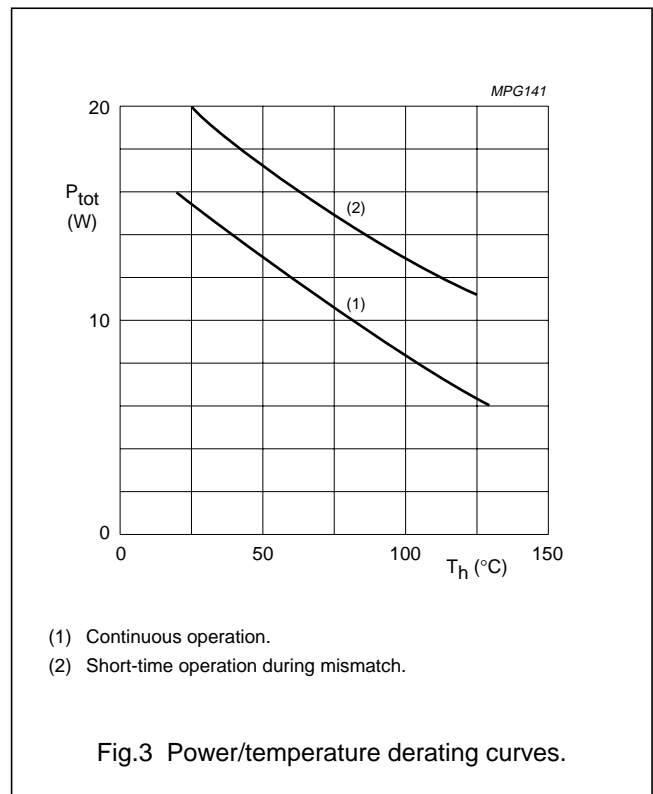
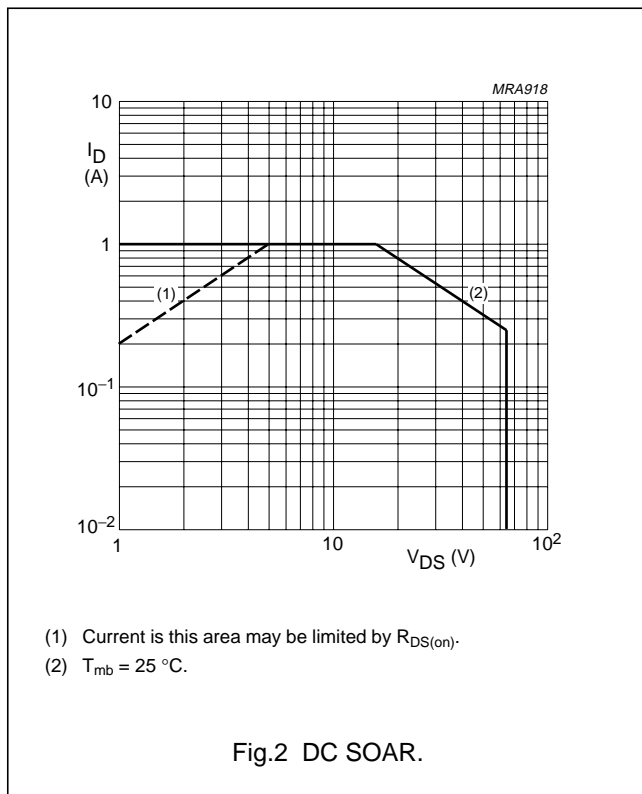
## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
$I_D$	DC drain current		–	1	A
$P_{tot}$	total power dissipation	up to $T_{mb} = 25\text{ °C}$	–	16	W
$T_{stg}$	storage temperature		–65	150	°C
$T_j$	junction temperature		–	200	°C

## THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	$T_{mb} = 25\text{ °C}; P_{tot} = 16\text{ W}$	11 K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink	$T_{mb} = 25\text{ °C}; P_{tot} = 16\text{ W}$	0.3 K/W



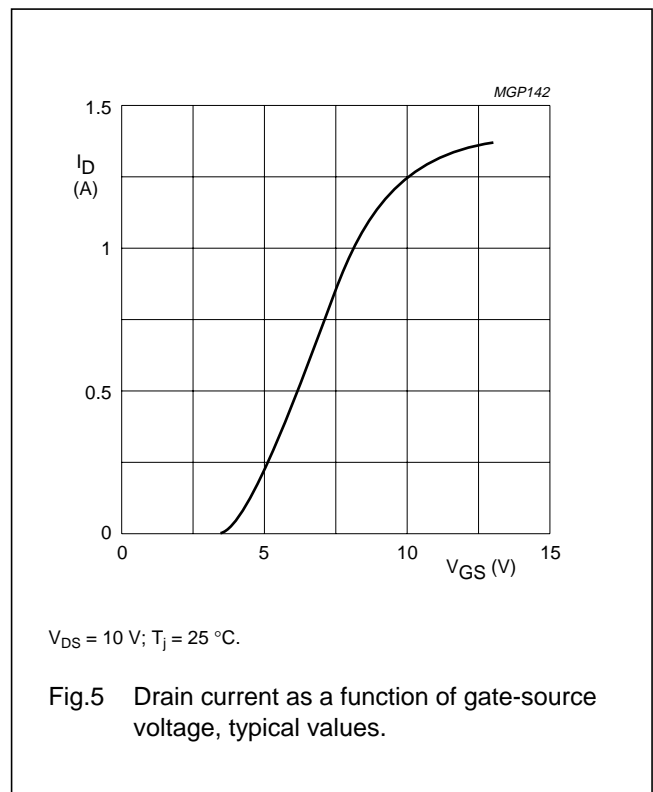
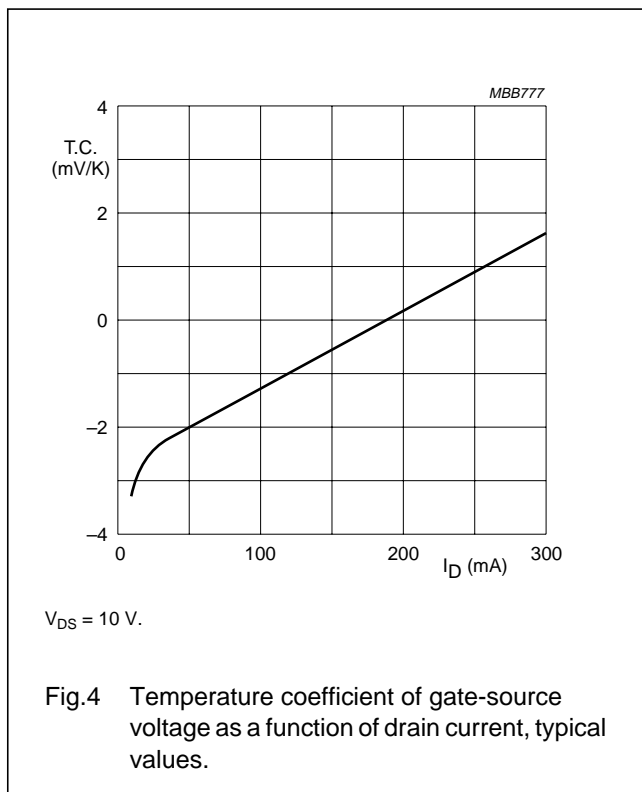
HF/VHF power MOS transistor

BLF242

**CHARACTERISTICS**

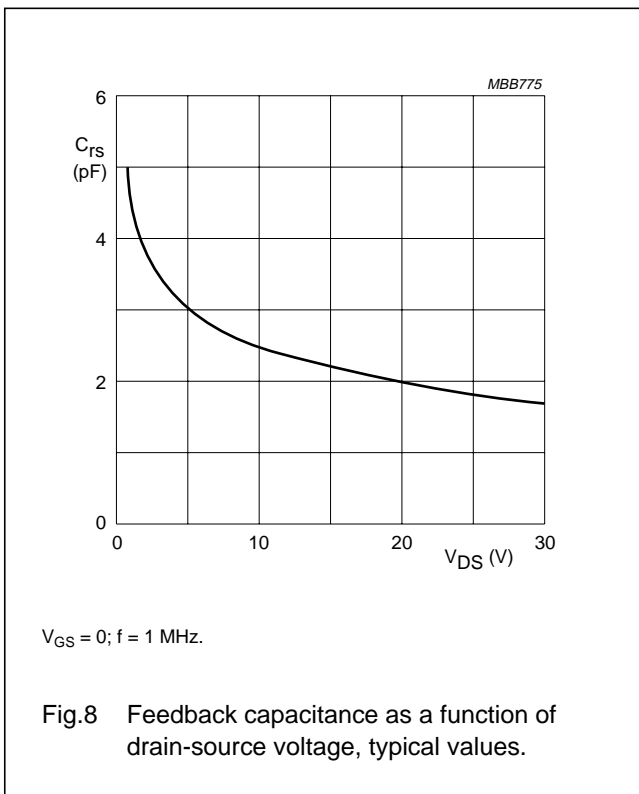
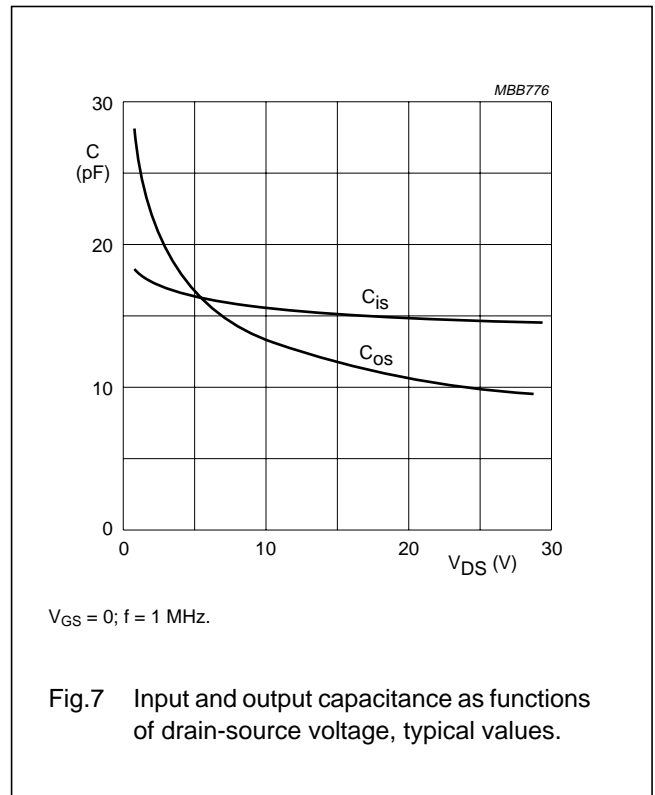
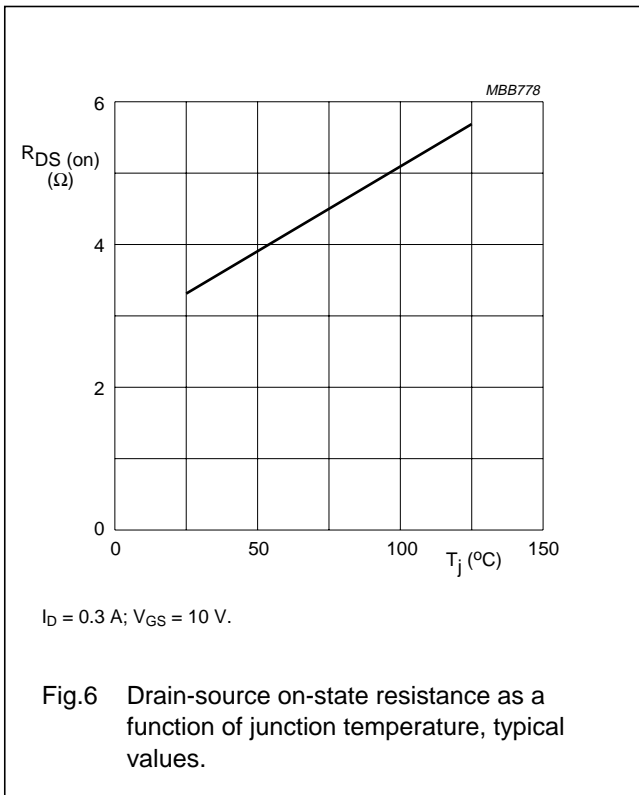
$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 0.1\text{ mA}$	65	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0; V_{DS} = 28\text{ V}$	–	–	10	$\mu\text{A}$
$I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\text{ V}; V_{DS} = 0$	–	–	1	$\mu\text{A}$
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 3\text{ mA}; V_{DS} = 10\text{ V}$	2	–	4.5	V
$g_{fs}$	forward transconductance	$I_D = 0.3\text{ A}; V_{DS} = 10\text{ V}$	0.16	0.24	–	S
$R_{DS(on)}$	drain-source on-state resistance	$I_D = 0.3\text{ A}; V_{GS} = 1\text{ V}$	–	3.3	5	$\Omega$
$I_{DSX}$	on-state drain current	$V_{GS} = 10\text{ V}; V_{DS} = 10\text{ V}$	–	1.2	–	A
$C_{is}$	input capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	13	–	pF
$C_{os}$	output capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	9.4	–	pF
$C_{rs}$	feedback capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	1.7	–	pF



HF/VHF power MOS transistor

BLF242



HF/VHF power MOS transistor

BLF242

**APPLICATION INFORMATION FOR CLASS-B OPERATION**

$T_h = 25\text{ }^\circ\text{C}$ ;  $R_{th\text{ mb-h}} = 0.3\text{ K/W}$ ; unless otherwise specified.

RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V <sub>DS</sub> (V)	I <sub>DQ</sub> (mA)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	R <sub>GS</sub> (Ω)
CW, class-B	175	28	10	5	> 13 typ. 16	> 50 typ. 60	47

**Ruggedness in class-B operation**

The BLF242 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

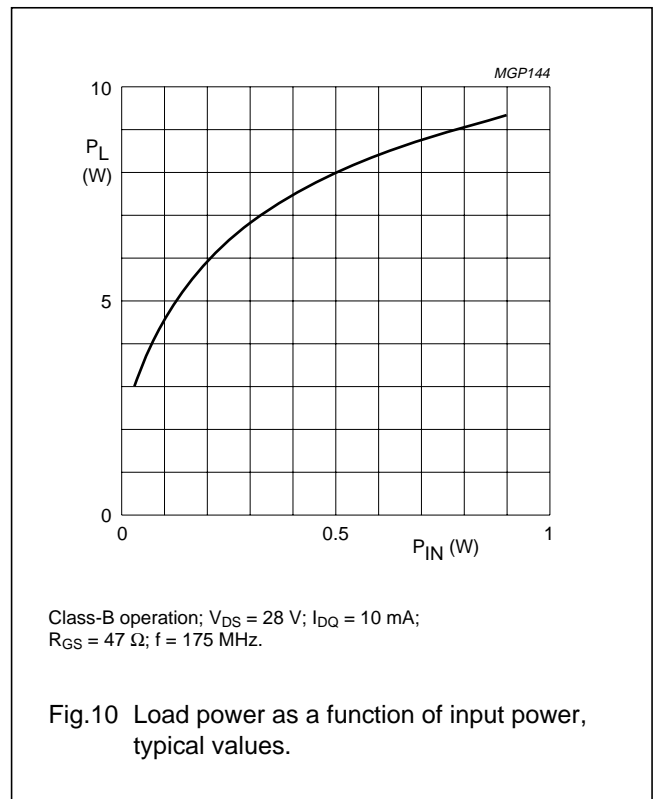
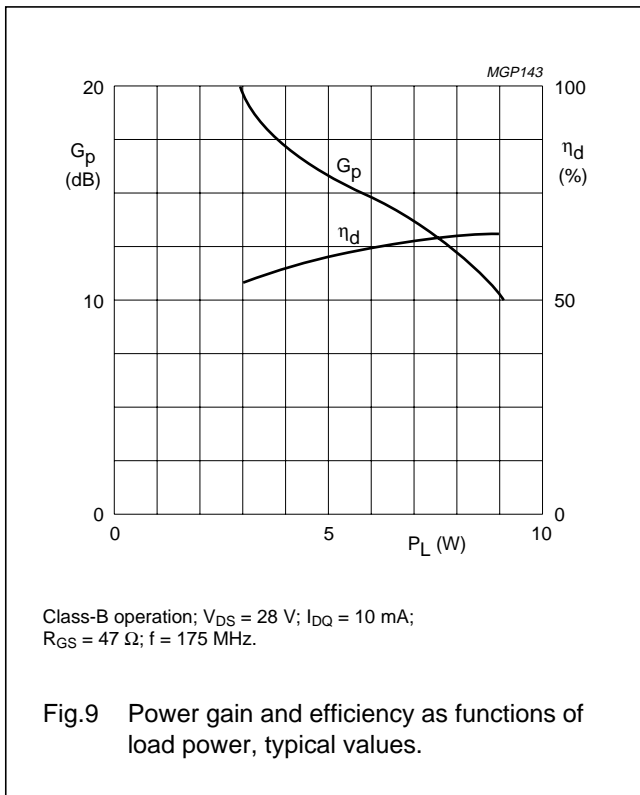
V<sub>DS</sub> = 28 V; f = 175 MHz at rated output power.

**Noise figure** (see Fig.11)

V<sub>DS</sub> = 28 V; I<sub>D</sub> = 0.2 A; f = 175 MHz;

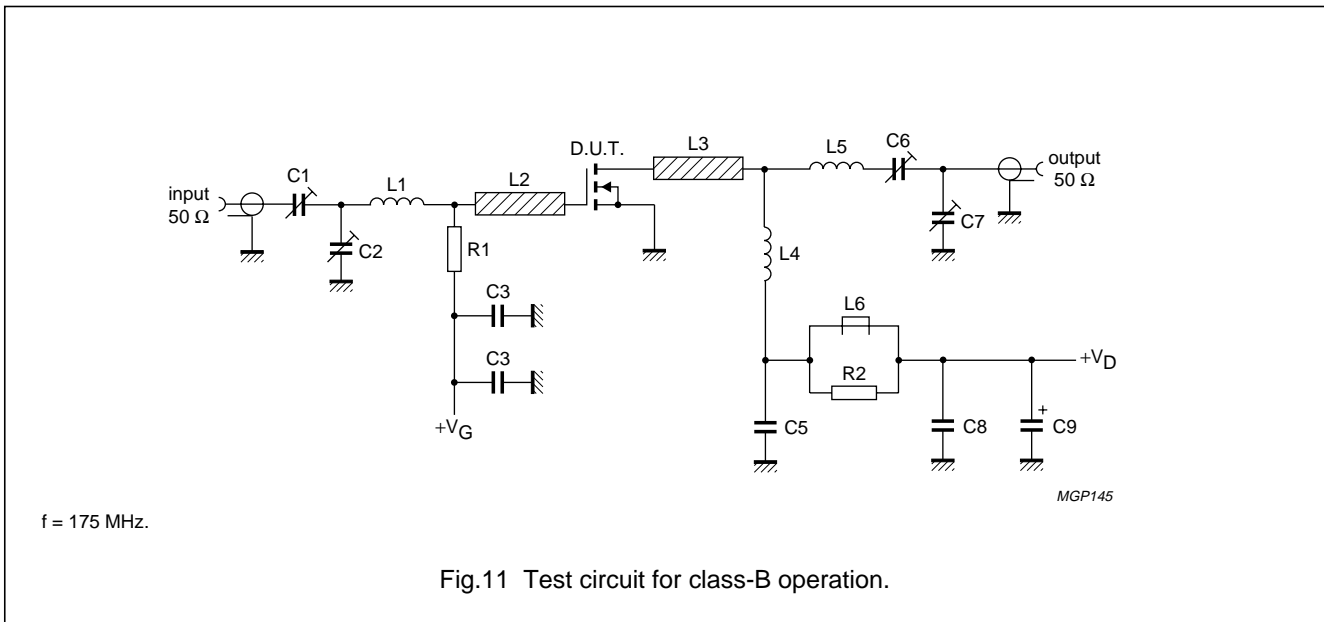
R<sub>GS</sub> = 47 Ω; T<sub>h</sub> = 25 °C. Input and output power matched for P<sub>L</sub> = 5 W;

F = typ. 5.5 dB.



HF/VHF power MOS transistor

BLF242



List of components (class-B test circuit)

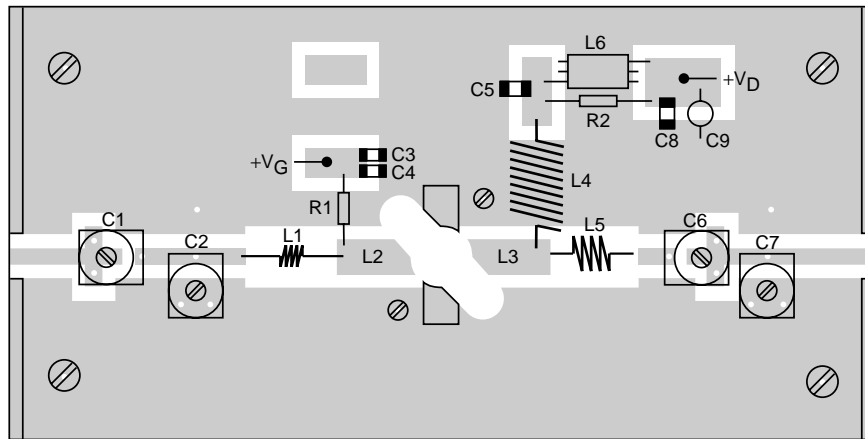
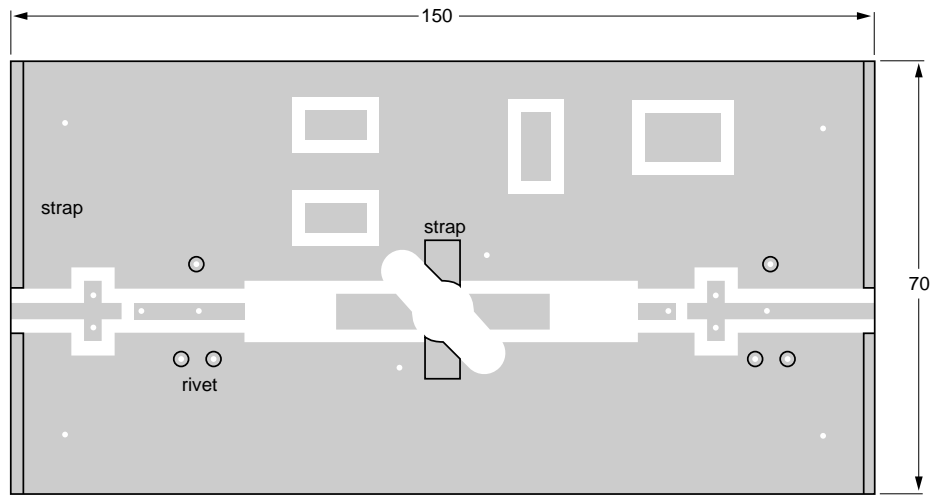
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C7	film dielectric trimmer	4 to 40 pF		2222 809 08002
C3	multilayer ceramic chip capacitor (note 1)	100 pF		
C4, C8	ceramic chip capacitor	100 nF		2222 852 47104
C6	film dielectric trimmer	5 to 60 pF		2222 809 08003
C9	electrolytic capacitor	2.2 μF, 40 V		
L1	5 turns enamelled 0.7 mm copper wire	53 nH	length 5.4 mm int. dia. 3 mm leads 2 × 5 mm	
L2, L3	stripline (note 2)	30 Ω	10 × 6 mm	
L4	11 turns enamelled 1 mm copper wire	500 nH	length 15.5 mm int. dia. 8 mm leads 2 × 5 mm	
L5	5 turns enamelled 1 mm copper wire	79 nH	length 9.1 mm int. dia. 5 mm leads 2 × 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36640
R1	0.5 W metal film resistor	47 Ω		
R2	0.5 W metal film resistor	10 Ω		

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy fibre-glass dielectric ( $\epsilon_r = 4.5$ ), thickness  $1/16$  inch.

HF/VHF power MOS transistor

BLF242



MGP146

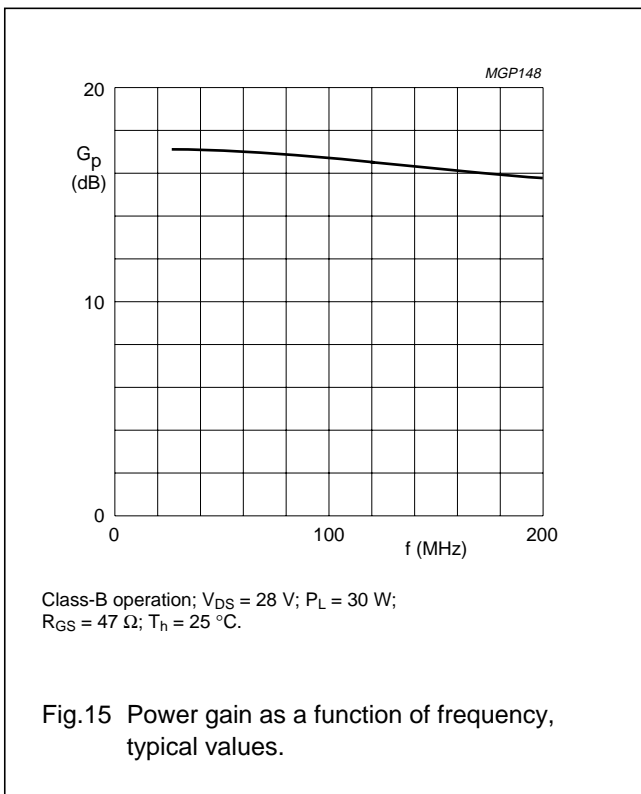
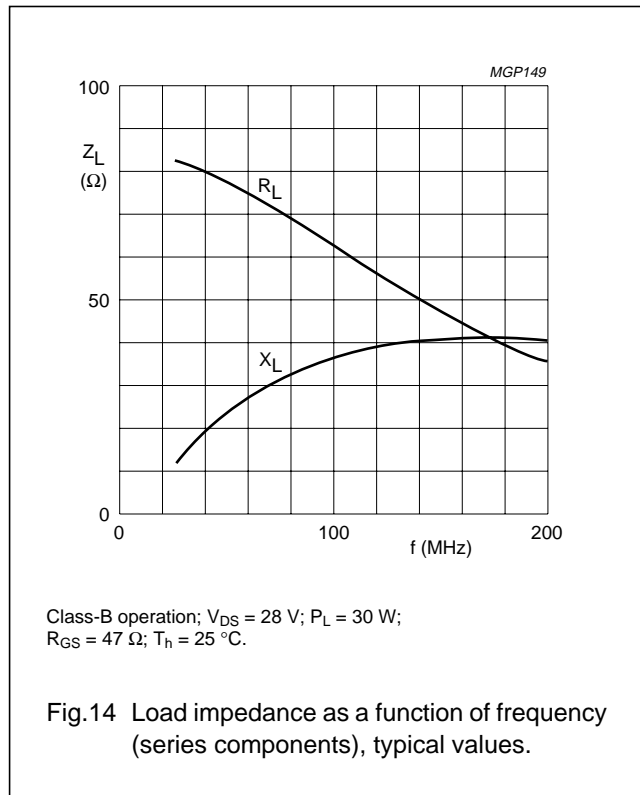
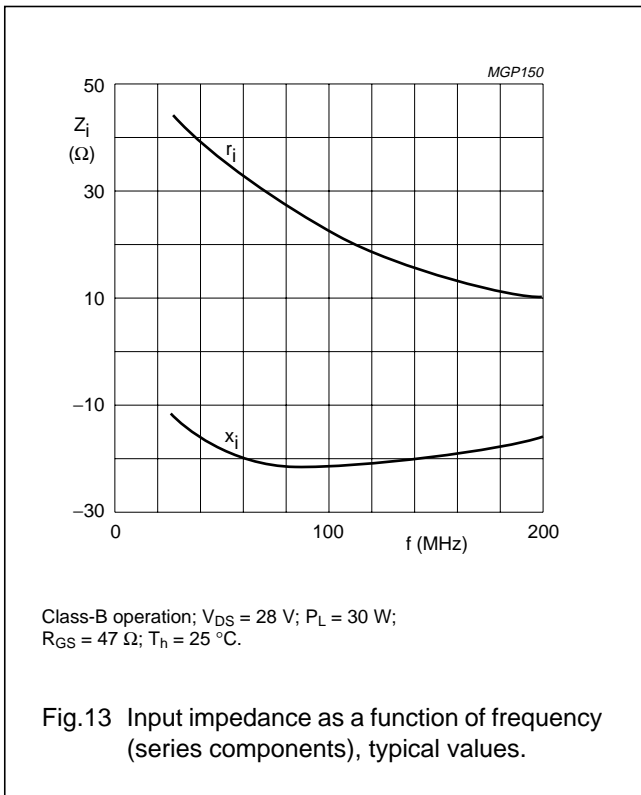
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by fixing screws, copper straps and hollow rivets at the edges of the board and under the source.  
 Dimensions in mm.

Fig.12 Component layout for 175 MHz class-B test circuit.



HF/VHF power MOS transistor

BLF242



HF/VHF power MOS transistor

BLF242

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads

SOT123A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	F	H	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	U <sub>3</sub>	w <sub>1</sub>	w <sub>2</sub>	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.63 9.42	2.72 2.31	20.71 19.93	5.61 5.16	3.33 3.04	4.63 4.11	18.42	25.15 24.38	6.61 6.09	9.78 9.39	0.51	1.02	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.397 0.371	0.107 0.091	0.815 0.785	0.221 0.203	0.131 0.120	0.182 0.162	0.725	0.99 0.96	0.26 0.24	0.385 0.370	0.02	0.04	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT123A						97-06-28

## HF/VHF power MOS transistor

BLF242

**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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