

# DATA SHEET

## **BSS87**

N-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# N-channel enhancement mode vertical D-MOS transistor

**BSS87**

**DESCRIPTION**

N-channel vertical D-MOS transistor in a SOT89 envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

**QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	280 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1 W
Drain-source on-resistance $I_D = 400\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DS(on)}$	max.	6 $\Omega$
		typ.	4.5 $\Omega$
Transfer admittance $I_D = 400\text{ mA}; V_{DS} = 25\text{ V}$	$ Y_{fs} $	typ.	350 mS
		min.	140 mS

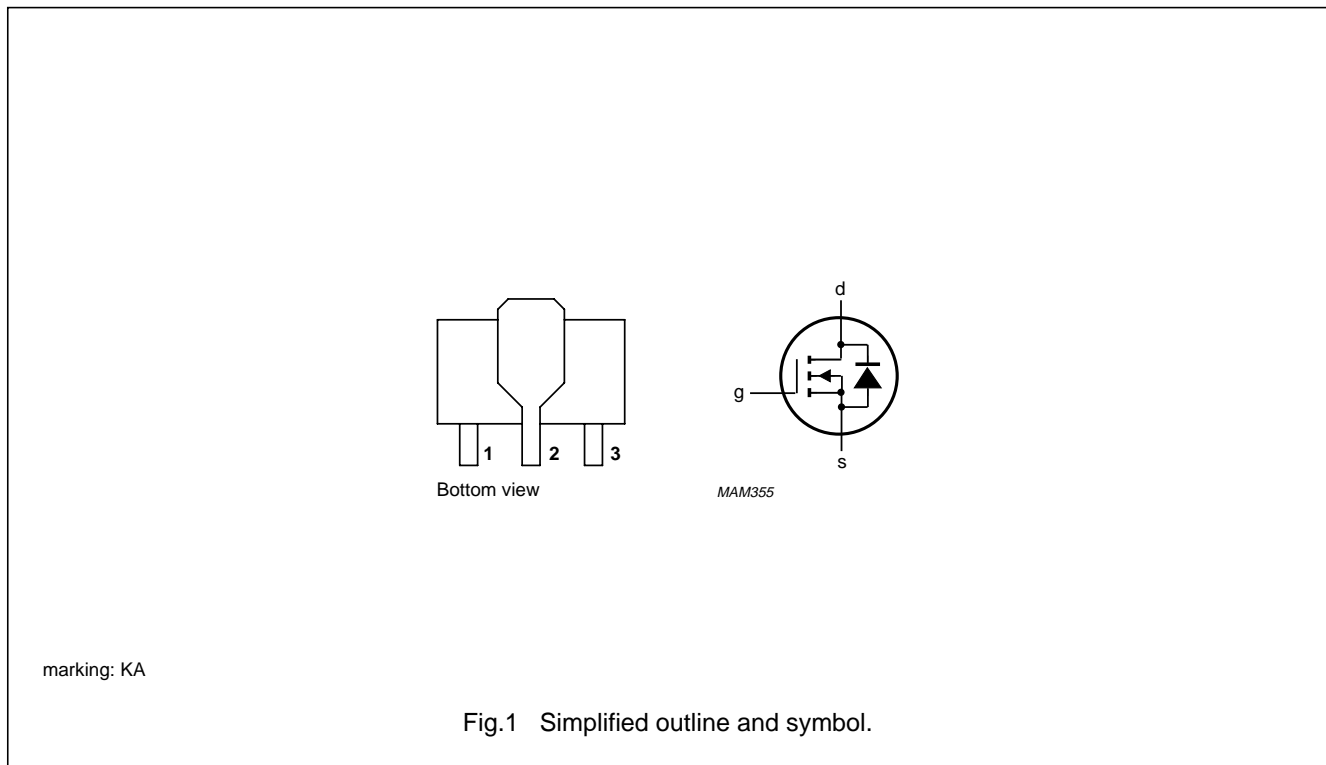
**FEATURES**

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.
- Low  $R_{DS(on)}$

**PINNING - SOT89**

- 1 = source
- 2 = drain
- 3 = gate

**PIN CONFIGURATION**



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### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	280 mA
Drain current (peak)	$I_{DM}$	max.	1.1 A
Total power dissipation up to $T_{amb} = 25\text{ °C}$ <sup>(1)</sup>	$P_{tot}$	max.	1 W
Storage temperature range	$T_{stg}$		-65 to + 150 °C
Junction temperature	$T_j$	max.	150 °C

### THERMAL RESISTANCE

From junction to ambient <sup>(1)</sup>	$R_{th\ j-a}$	=	125 K/W
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### Note

1. Transistor mounted on ceramic substrate area 2.5 cm<sup>2</sup>, thickness 0.7 mm.

### CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified

Drain-source breakdown voltage $I_D = 250\ \mu\text{A}; V_{GS} = 0$	$V_{(BR)\ DSS}$	min.	200 V
Drain-source leakage current $V_{DS} = 60\ \text{V}; V_{GS} = 0$ $V_{DS} = 200\ \text{V}; V_{GS} = 0$	$I_{DSS}$ $I_{DSS}$	max. max. typ.	200 nA 60 $\mu\text{A}$ 100 nA
Gate-source leakage current $V_{GS} = 20\ \text{V}; V_{DS} = 0$	$I_{GSS}$	max.	100 nA
Gate threshold voltage $I_D = 1\ \text{mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source on-resistance $I_D = 400\ \text{mA}; V_{GS} = 10\ \text{V}$	$R_{DS(on)}$	max. typ.	6 $\Omega$ 4.5 $\Omega$
Transfer admittance $I_D = 400\ \text{mA}; V_{DS} = 25\ \text{V}$	$ Y_{fs} $	typ. min.	350 mS 140 mS
Input capacitance $f = 1\ \text{MHz};$ $V_{DS} = 25\ \text{V}; V_{GS} = 0$	$C_{iss}$	max. typ.	60 pF 45 pF
Output capacitance $f = 1\ \text{MHz};$ $V_{DS} = 25\ \text{V}; V_{GS} = 0$	$C_{oss}$	max. typ.	25 pF 15 pF

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Feedback capacitance  $f = 1 \text{ MHz}$ ;

$V_{DS} = 25 \text{ V}$ ;  $V_{GS} = 0$

$C_{rss}$	max.	10 pF
	typ.	3.5 pF

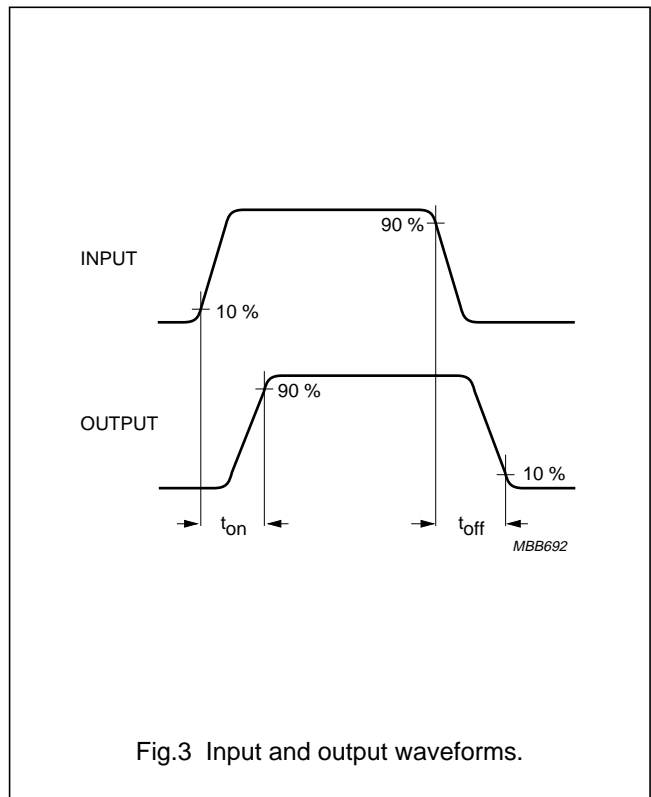
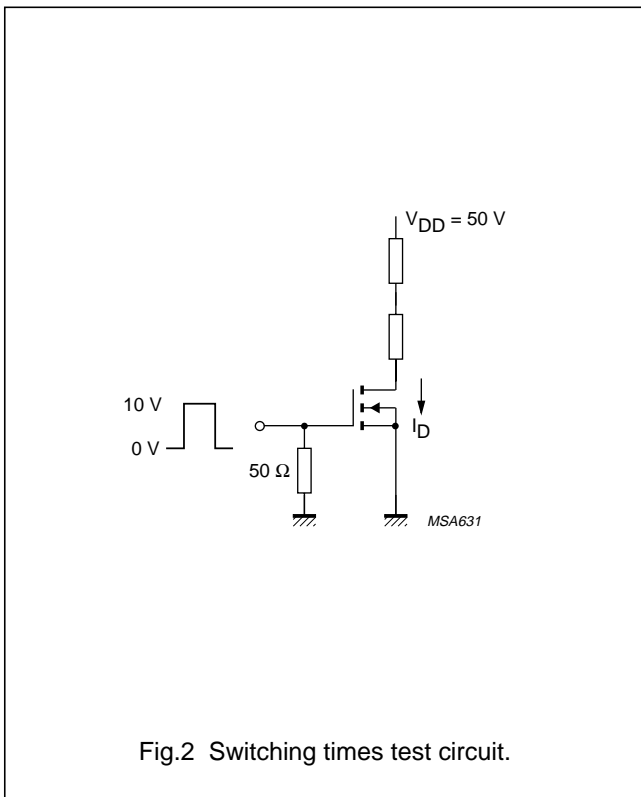
Switching times (see Figs 2 and 3)

$I_D = 250 \text{ mA}$ ;  $V_{DD} = 50 \text{ V}$ ;

$t_{on}$	typ.	5 ns
	max.	10 ns

$V_{GS} = 0 \text{ to } 10$

$t_{off}$	typ.	15 ns
	max.	25 ns



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PACKAGE OUTLINES

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

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**BSS87****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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D-MOS transistor

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Printed in The Netherlands

137107/00/01/pp8

Date of release: April 1995

Document order number: 9397 750 02492

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