

# TrenchMOS™ transistor Logic level FET

**BUK9775-55**

## GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

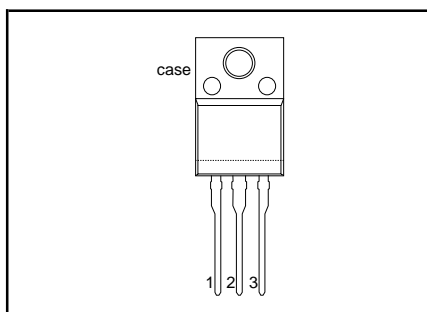
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	55	V
$I_D$	Drain current (DC)	11.7	A
$P_{tot}$	Total power dissipation	19	W
$T_j$	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 5\text{ V}$	75	mΩ

## PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

## PIN CONFIGURATION



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	55	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
$I_D$	Drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	11.7	A
$I_D$	Drain current (DC)	$T_{mb} = 100\text{ }^\circ\text{C}$	-	7.4	A
$I_{DM}$	Drain current (pulse peak value)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	47	A
$P_{tot}$	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	19	W
$T_{stg}, T_j$	Storage & operating temperature	-	- 55	150	°C

## ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

## THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to heatsink	with heatsink compound	-	6.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	55	-	K/W

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### STATIC CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 0.25 mA; T <sub>j</sub> = -55°C	55 50	- -	- -	V V
V <sub>GS(TO)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = 1 mA T <sub>j</sub> = 150°C T <sub>j</sub> = -55°C	1 0.6 -	1.5 - -	2 - 2.3	V V V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150°C	-	0.05	10	μA
I <sub>GSS</sub>	Gate source leakage current	V <sub>GS</sub> = ±5 V; V <sub>DS</sub> = 0 V T <sub>j</sub> = 150°C	-	0.02	100	μA
±V <sub>(BR)GSS</sub>	Gate-source breakdown voltage	I <sub>G</sub> = ±1 mA; T <sub>j</sub> = 150°C	10	-	5	μA V
R <sub>DS(ON)</sub>	Drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 7 A T <sub>j</sub> = 150°C	- -	58 -	75 139	mΩ mΩ

### DYNAMIC CHARACTERISTICS

T<sub>mb</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> = 25 V; I <sub>D</sub> = 10 A	5	10	-	S
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz	-	500	650	pF
C <sub>oss</sub>	Output capacitance		-	110	135	pF
C <sub>riss</sub>	Feedback capacitance		-	60	85	pF
t <sub>d on</sub>	Turn-on delay time	V <sub>DD</sub> = 30 V; I <sub>D</sub> = 10 A; V <sub>GS</sub> = 5 V; R <sub>G</sub> = 10 Ω Resistive load	-	10	15	ns
t <sub>r</sub>	Turn-on rise time		-	47	70	ns
t <sub>d off</sub>	Turn-off delay time		-	28	40	ns
t <sub>f</sub>	Turn-off fall time		-	33	45	ns
L <sub>d</sub>	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L <sub>s</sub>	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

### ISOLATION LIMITING VALUE AND CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>ISOL</sub>	R.M.S isolation voltage from all three terminals to external heatsink	f = 50-60Hz; sinusoidal waveform; R.H. ≤ 65% clean & dustfree	-	-	2500	V
C <sub>ISOL</sub>	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

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**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS**
 $T_j = 25^\circ\text{C}$  unless otherwise specified

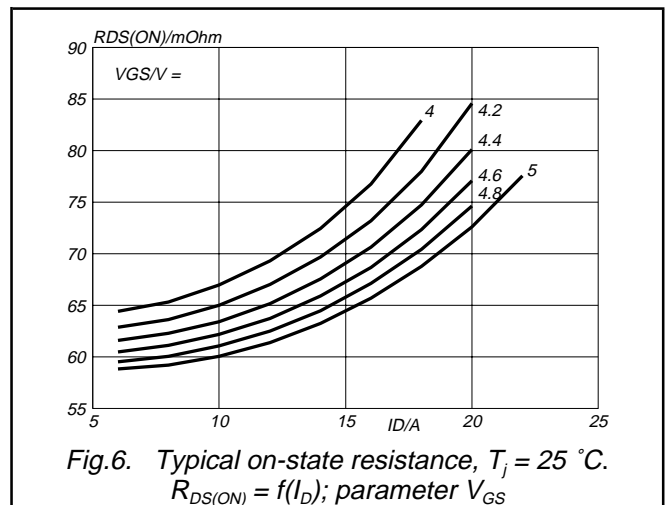
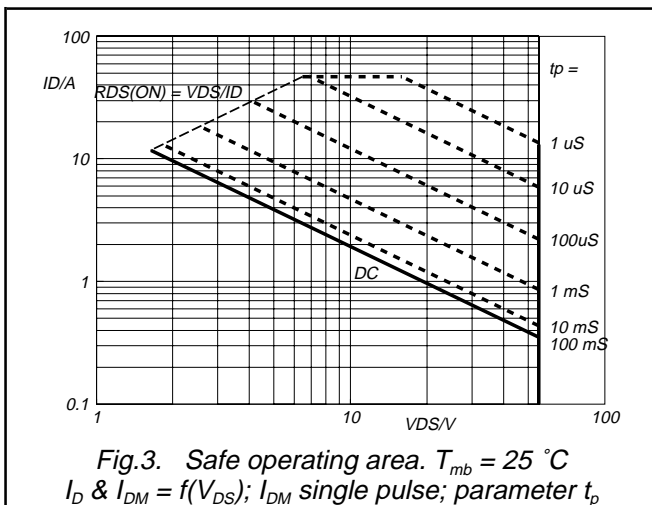
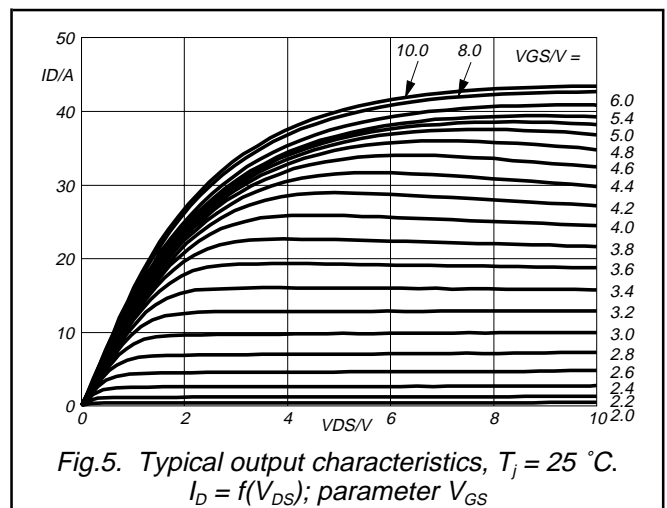
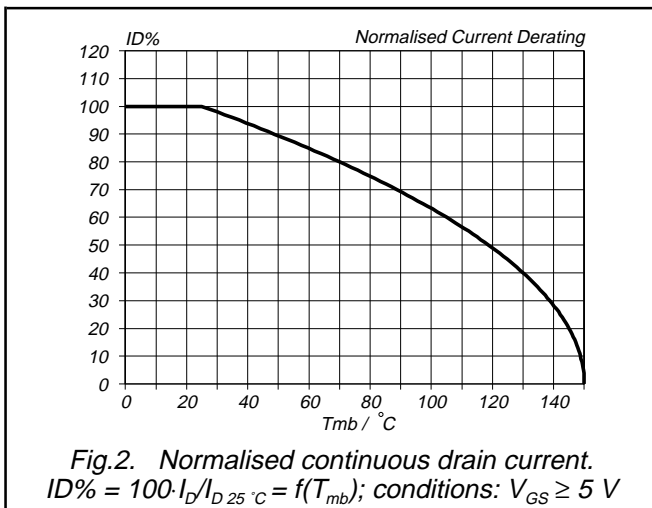
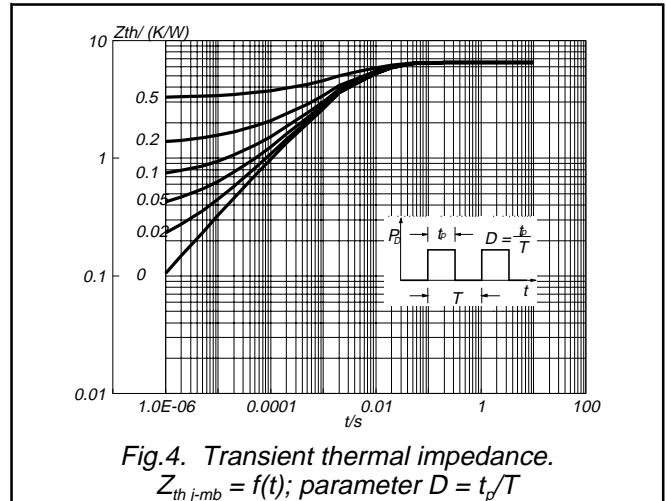
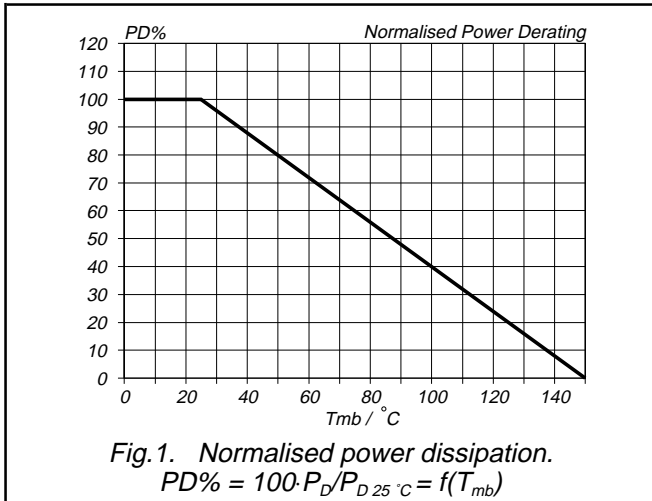
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current		-	-	11.7	A
$I_{DRM}$	Pulsed reverse drain current		-	-	47	A
$V_{SD}$	Diode forward voltage	$I_F = 11.7\text{ A}; V_{GS} = 0\text{ V}$	-	0.95	1.2	V
$t_{rr}$	Reverse recovery time	$I_F = 11.7\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	32	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = -10\text{ V}; V_R = 30\text{ V}$	-	0.12	-	$\mu\text{C}$

**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 10\text{ A}; V_{DD} \leq 25\text{ V};$ $V_{GS} = 5\text{ V}; R_{GS} = 50\ \Omega; T_{mb} = 25^\circ\text{C}$	-	-	30	mJ

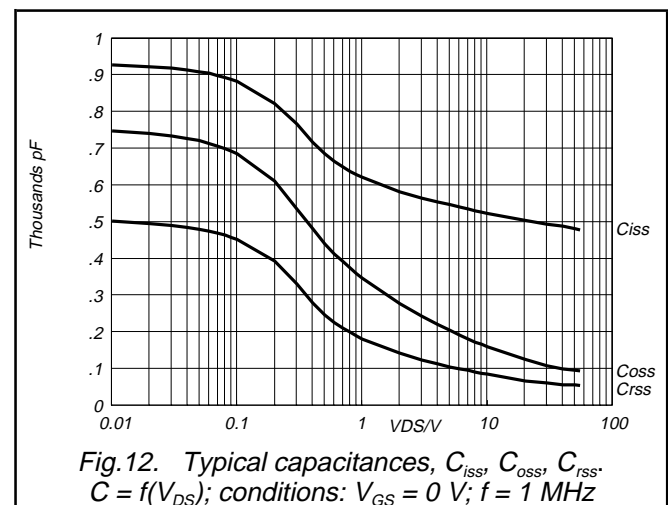
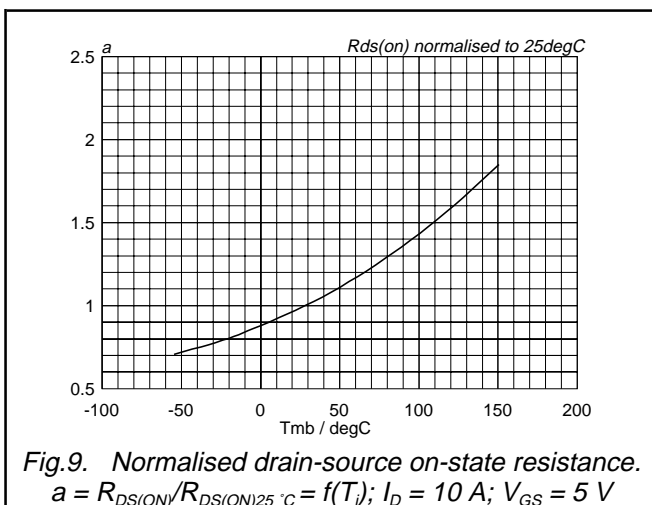
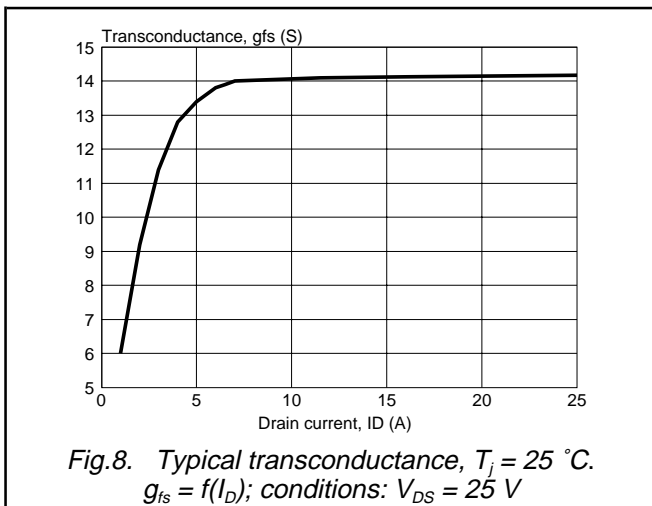
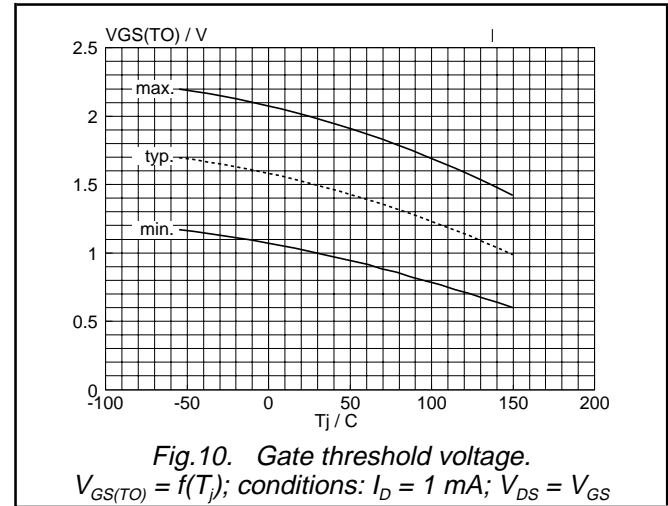
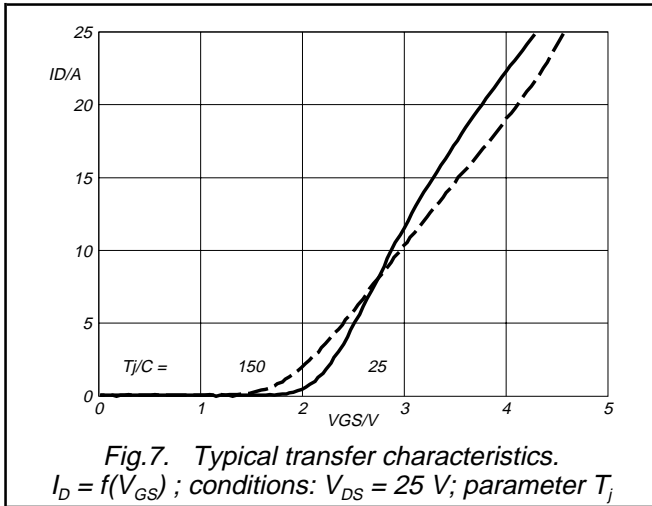
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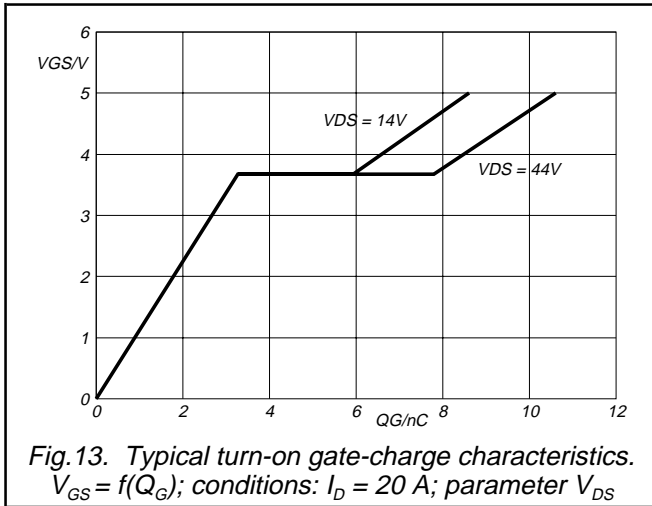


Fig. 13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$ ; conditions:  $I_D = 20 A$ ; parameter  $V_{DS}$

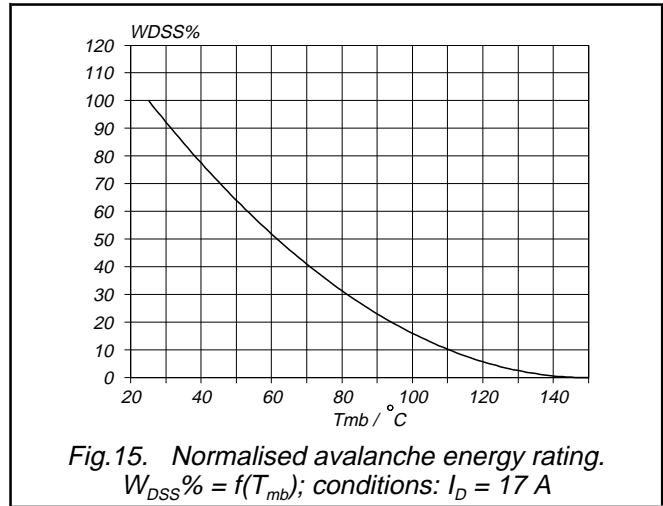


Fig. 15. Normalised avalanche energy rating.  
 $W_{DSS}\% = f(T_{mb})$ ; conditions:  $I_D = 17 A$

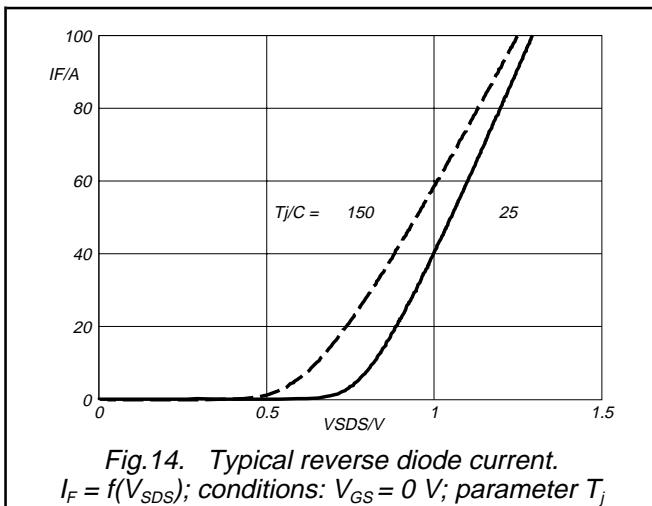


Fig. 14. Typical reverse diode current.  
 $I_F = f(V_{SDS})$ ; conditions:  $V_{GS} = 0 V$ ; parameter  $T_j$

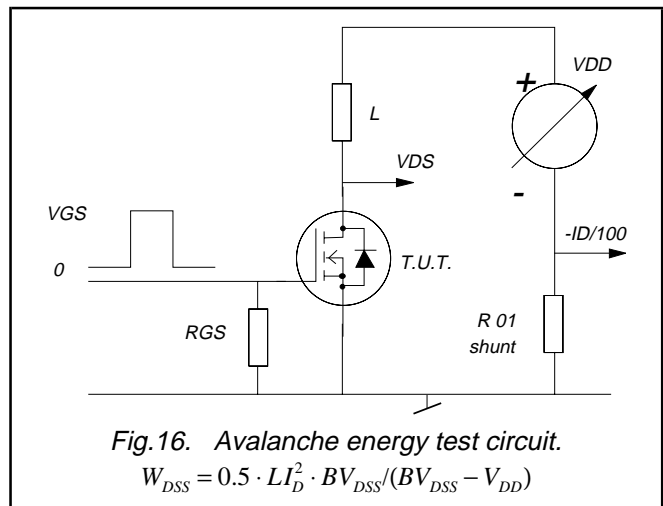


Fig. 16. Avalanche energy test circuit.  
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

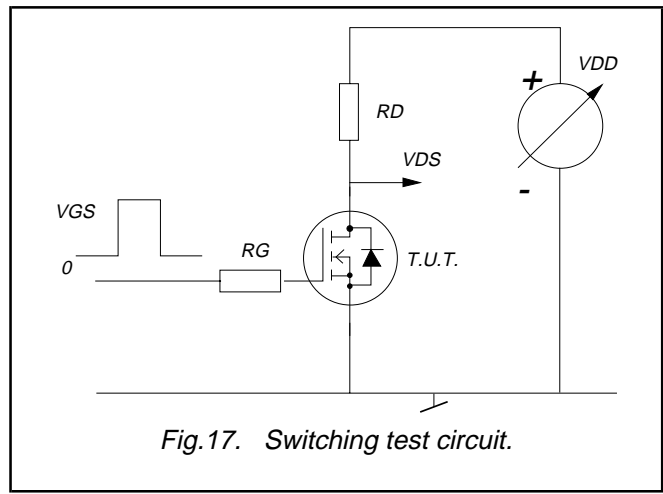
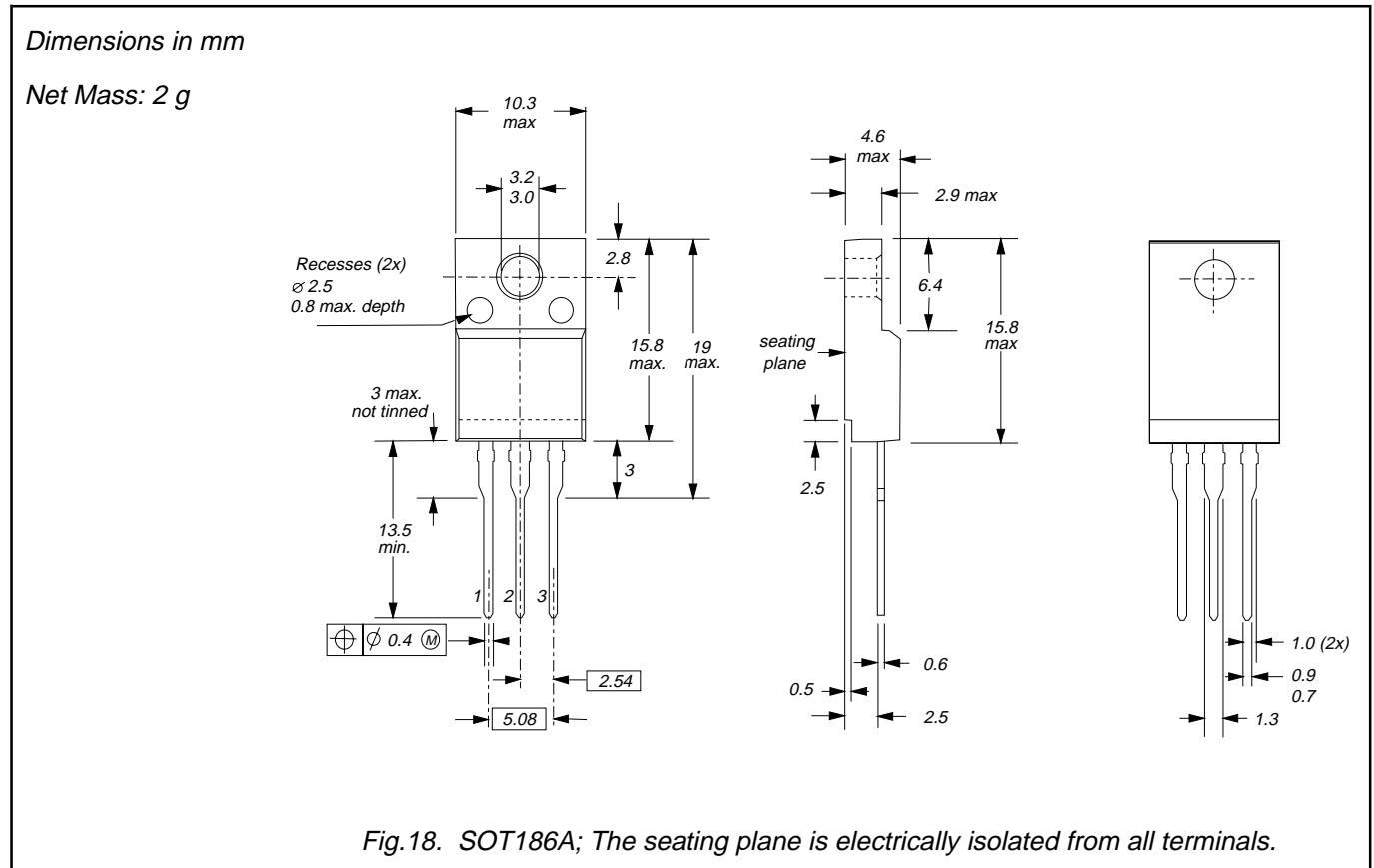


Fig. 17. Switching test circuit.

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**MECHANICAL DATA**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
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