DATA SHEET

PDIUSBD12
USB interface device with parallel bus

Product specification
Supersedes data of 1998 Sep 24

1999 Jan 08

Philips
Semiconductors

PHILIPS

USB interface device with parallel bus PDIUSBD12

FEATURES

- Complies with the Universal Serial Bus specification Rev. 1.1
- High performance USB interface device with integrated SIE, FIFO memory, transceiver and voltage regulator
- Compliant with most Device Class specifications
- High-speed (2 Mbytes/s) parallel interface to any external microcontroller/microprocessor
- Fully autonomous DMA operation
- Integrated 320 bytes of multi-configuration FIFO memory
- Double buffering scheme for main endpoint increases throughput and eases real time data transfer
- 1MByte/s data transfer rate achievable in Bulk mode, 1Mbit/s data transfer rate achievable in Isochronous mode
- Bus-powered capability with very good EMI performance
- Controllable LazyClock output during suspend
- Software controllable connection to the USB bus (SoftConnect™)
- Good USB connection indicator that blinks with traffic (GoodLink™)
- Programmable clock frequency output
- Complies with the ACPI, OnNOW, and USB power management requirements
- Internal power-on reset and low voltage reset circuit
- Available in SO28 and TSSOP28 pin packages
- Full industrial grade operation from –40 to +85°C
- Higher than 8kV in-circuit ESD protection lowers cost of extra components
- Full-scan design with high fault coverage (>99%) ensures high quality
- Operation with dual voltages:
  3.3 ± 0.3V or extended 5V supply range of 3.6 – 5.5V
- Multiple interrupt modes to facilitate both bulk and isochronous transfers

DESCRIPTION

The PDIUSBD12 is a cost and feature-optimized USB device. It is normally used in microcontroller-based systems and communicates with the system microcontroller over the high speed general-purpose parallel interface. It also supports local DMA transfer.

This modular approach to implementing a USB interface allows the designer to choose the optimum system microcontroller from the available wide variety. This flexibility cuts down the development time, risks, and costs by allowing the use of the existing architecture and minimize firmware investments. This results in the fastest way to develop the most cost-effective USB peripheral solution.

The PDIUSBD12 fully conforms to the USB specification Rev. 1.1. It is also designed to be compliant with most device class specifications: Imaging Class, Mass Storage Devices, Communication Devices, Printing Devices, and Human Interface Devices. As such, the PDIUSBD12 is ideally suited for many peripherals like Printer, Scanner, External Mass Storage (Zip Drive), Digital Still Camera, etc. It offers an immediate cost reduction for applications that currently use SCSI implementations.

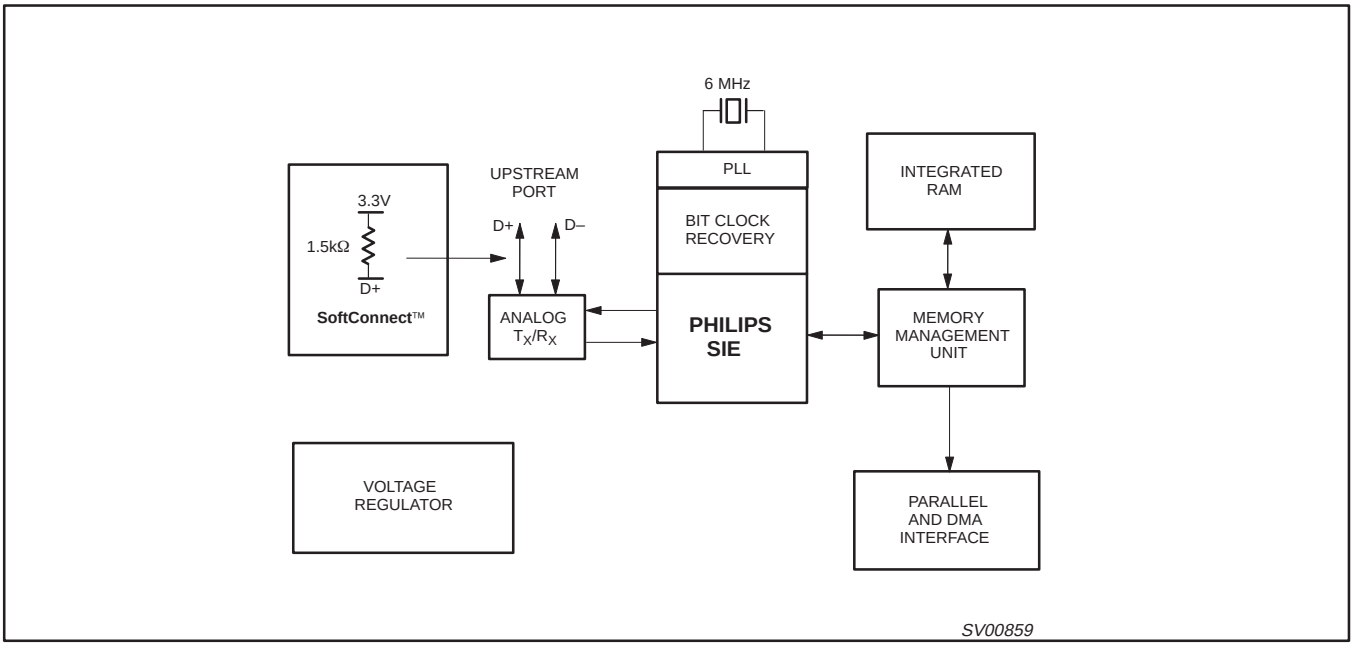
The PDIUSBD12 low suspend power consumption along with the LazyClock output allows for easy implementation of equipment that is compliant to the ACPI, OnNOW, and USB power management requirements. The low operating power allows the implementation of bus-powered peripherals.

In addition, it also incorporates features like SoftConnect™, GoodLink™, programmable clock output, low frequency crystal oscillator, and integration of termination resistors. All of these features contribute to significant cost savings in the system implementation and at the same time ease the implementation of advanced USB functionality into the peripherals.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
28-pin plastic SO	–40°C to +85°C	PDIUSBD12 D	PDIUSBD12 D	SOT136-1
28-pin plastic TSSOP	–40°C to +85°C	PDIUSBD12 PW	PDUSBD12PW DH	SOT361-1

BLOCK DIAGRAM



NOTE:
* This is a conceptual block diagram and does not include each individual signal.

Analog Transceiver
The integrated transceiver interfaces directly to the USB cables through termination resistors.

Voltage Regulator
A 3.3V regulator is integrated on-chip to supply the analog transceiver. This voltage is also provided as an output to connect to the external 1.5 kΩ pull-up resistor. Alternatively, the PDIUSBD12 provides SoftConnect™ technology with integrated 1.5 kΩ pull-up resistor.

PLL
A 6 MHz to 48 MHz clock multiplier PLL (Phase-Locked Loop) is integrated on-chip. This allows for the use of low-cost 6 MHz crystal. EMI is also minimized due to the lower frequency crystal. No external components are needed for the operation of the PLL.

Bit Clock Recovery
The bit clock recovery circuit recovers the clock from the incoming USB data stream using 4X over-sampling principle. It is able to track jitter and frequency drift specified by the USB specification.

Philips Serial Interface Engine (PSIE)
The Philips SIE implements the full USB protocol layer. It is completely hardwired for speed and needs no firmware intervention. The functions of this block include: synchronization pattern recognition, parallel/serial conversion, bit stuffing/de-stuffing, CRC checking/generation, PID verification/generation, address recognition, and handshake evaluation/generation.

SoftConnect™
The connection to the USB is accomplished by bringing D+ (for high-speed USB device) high through a 1.5 kΩ pull-up resistor. In the PDIUSBD12, the 1.5 kΩ pull-up resistor is integrated on-chip and is not connected to V_{CC} by default. The connection is established through a command sent by the external/system microcontroller. This allows the system microcontroller to complete its initialization sequence before deciding to establish connection to the USB. Re-initialization of the USB bus connection can also be performed without requiring to pull out the cable.

The PDIUSBD12 will check for USB VBUS availability before the connection can be established. VBUS sensing is provided through EOT_N pin. See the pin description for details. Sharing of VBUS sensing and EOT_N can be easily accomplished by using VBUS voltage as the pull up voltage for the normally open-drain output of the DMA controller pin.

It should be noted that the tolerance of the internal resistors is higher (25%) than that specified by the USB specification (5%). However, the overall V_{SE} voltage specification for the connection can still be met with good margin. The decision to make sure of this feature lies with the users.

SoftConnect™ is a patent pending technology from Philips Semiconductors.

GoodLink™

Good USB connection indication is provided through GoodLink™ technology. During enumeration, the LED indicator will blink ON momentarily corresponding to the enumeration traffic. When the PDIUSBD12 is successfully enumerated and configured, the LED indicator will be permanently ON. Subsequent successful (with acknowledgement) transfer to and from the PDIUSBD12 will blink OFF the LED. During suspend, the LED will be OFF.

This feature provides a user-friendly indicator on the status of the USB device, the connected hub and the USB traffic. It is a useful field diagnostics tool to isolate faulty equipment. This feature helps lower field support and hotline costs.

Memory Management Unit (MMU) and Integrated RAM

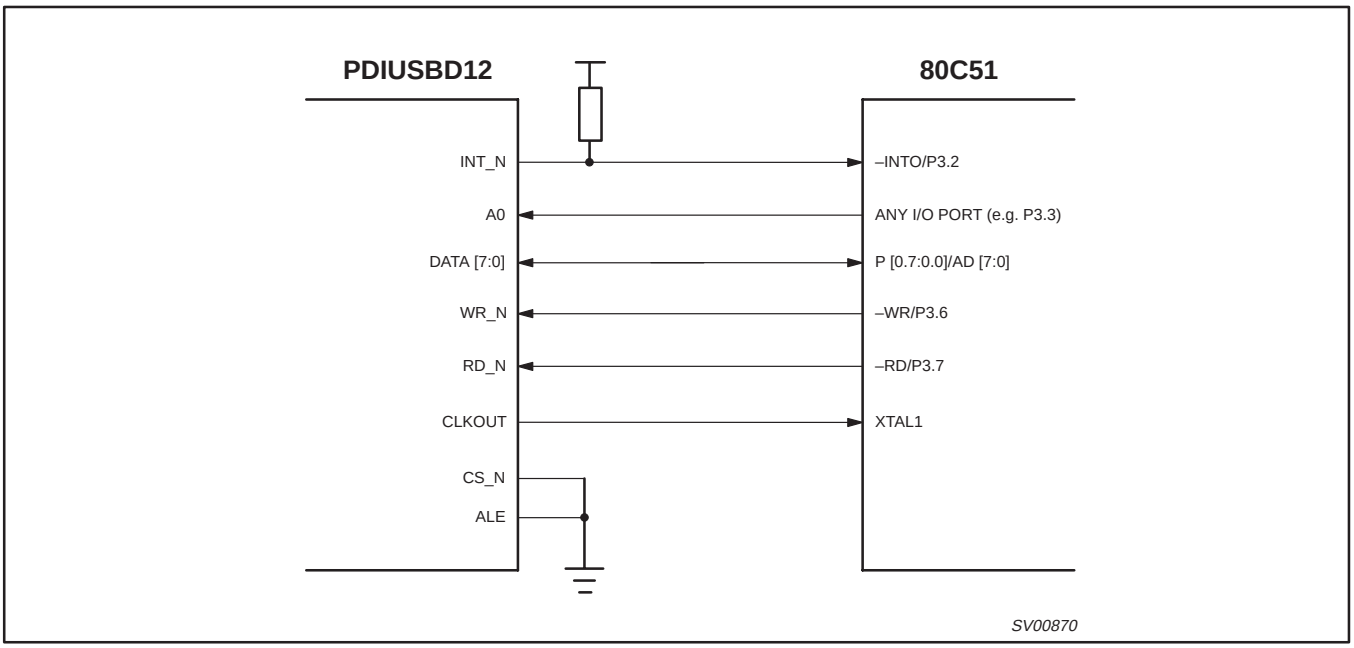
The MMU and the integrated RAM buffer the difference in speed between USB, running in bursts of 12 Mbits/s and the parallel interface to the microcontroller. This allows the microcontroller to read and write USB packets at its own speed.

Parallel and DMA Interface

A generic parallel interface is defined for ease-of-use, speed, and allows direct interfacing to major microcontrollers. To a microcontroller, the PDIUSBD12 appears as a memory device with 8-bit data bus and 1 address bit (occupying 2 locations). The PDIUSBD12 supports both multiplexed and non-multiplexed address and data bus. The PDIUSBD12 also supports DMA (Direct Memory Access) transfer which allows the main endpoint (endpoint 2) to directly transfer to and from the local shared memory. Both single cycle and burst mode DMA transfers are supported.

Example of parallel interface to a dedicated 80C51

In this example, the ALE is permanently tied LOW to signify a separate address and data bus configuration. The A0 pin of the PDIUSBD12 connects to any of the 80C51 I/O port. This port controls command or data phase to the PDIUSBD12. The multiplexed address and data bus of the 80C51 can now be connected directly to the data bus of the PDIUSBD12. The address phase will simply be ignored by the PDIUSBD12. The crystal input of the 80C51 can be supplied by the CLKOUT output of the PDIUSBD12.



DMA TRANSFER

Direct Memory Address (DMA) allows an efficient transfer of a block of data between the host and the local shared memory. Using a DMA controller, data transfer between the PDIUSBD12 main endpoint (endpoint 2) and the local shared memory can happen autonomously without local CPU intervention.

Preceding any DMA transfer, the local CPU receives from the host the necessary setup information and programs the DMA controller accordingly. Typically, the DMA controller is setup for demand transfer mode and the byte count register and the address counter are programmed with the right values. In this mode, transfers occur only when the PDIUSBD12 requests them and terminated when the byte count register reaches zero. After the DMA controller has been programmed, the DMA enable bit of the PDIUSBD12 is set by the local CPU to initiate the transfer.

The PDIUSBD12 can be programmed for single cycle DMA or burst mode DMA. In single cycle DMA, the DMREQ is deactivated for every single acknowledgement by the DMACK_N before being asserted again. In burst mode DMA, the DMREQ is held active for the number of bursts programmed in the device before returning inactive. This process continues until the PDIUSBD12 receives a DMA termination notice through EOT_N. This will generate an interrupt to notify the local CPU that DMA operation is completed.

For DMA read operation, the DMREQ will only be activated whenever the buffer is full signifying that the host has successfully transferred a packet to the PDIUSBD12. With the double buffering scheme, the host can start filling up the second buffer while the first buffer is being read out. This parallel processing increases effective throughput. For the case when the host does not fill up the buffer completely (less than 64 bytes or 128 bytes for single direction ISO configuration), the DMREQ will be deactivated at the last byte of the buffer regardless of the current DMA burst count. It will be asserted again on the next packet with a refreshed DMA burst count.

Similarly, for DMA write operation, the DMREQ remains active whenever the buffer is not full. When the buffer is filled up, the packet is sent over to the host on the next IN token and DMREQ will be reactivated if the transfer was successful. Also, the double buffering scheme here will improve throughput. For non-isochronous transfer (bulk and interrupt), the buffer needs to be completely filled up by the DMA write operation before the data is sent to the host. The only exception is at the end of DMA transfer when the reception of EOT_N will stop DMA write operation and the buffer content will be sent to the host on the next IN token.

For isochronous transfer, the local CPU and DMA controller has to guarantee that they are able to sink or source the maximum packet size in one USB frame (1 ms).

The assertion of DMACK_N will automatically selects the main endpoint (endpoint 2) regardless of the current selected endpoint. The DMA operation of the PDIUSBD12 can be interleaved with normal I/O access to other endpoints.

DMA operation can be terminated by resetting the DMA enable register bit or the assertion of EOT_N together with DMACK_N and either RD_N or WR_N.

PDIUSBD12 supports DMA transfer in a single address mode and it can also work in dual address mode of the DMA controller. In the single address mode, DMA transfer is done via the DREQ, DMACK_N, EOT_N, WR_N and RD_N control lines. In the dual address mode, DMREQ, DMACK_N and EOT_N are NOT used, instead CS_N, WR_N and RD_N control signals are used. The I/O mode Transfer Protocol of PDIUSBD12 needs to be followed. The source of the DMAC is accessed during the read cycle, and the destination accessed during the write cycle. Transfer needs to be done in two separate bus cycles, storing the data temporarily in the DMAC.

ENDPOINT DESCRIPTION

The PDIUSBD12 endpoints are generic enough to be used by various device classes ranging from Imaging, Printer, Mass Storage and Communication device classes. The PDIUSBD12 endpoints can be configured for 4 modes depending on the “Set Mode” command. The 4 modes are:

Mode 0 (Non-ISO Mode):	no Isochronous transfer
Mode 1 (ISO-OUT Mode):	Isochronous output only transfer
Mode 2 (ISO-IN Mode):	Isochronous input only transfer
Mode 3 (ISO-IO Mode):	Isochronous input and output transfer

MODE 0 (NON-ISO MODE):

ENDPOINT NUMBER	ENDPOINT INDEX	TRANSFER TYPE	ENDPOINT TYPE	DIRECTION	MAX. PACKET SIZE (BYTES)
0	0 1	Control Out Control In	Default	OUT IN	16 16
1	2 3	Generic Out Generic In	Generic Generic	OUT IN	16 16
2	4 5	Generic Out Generic In	Generic Generic	OUT IN	64[4] 64[4]

MODE 1 (ISO-OUT MODE):

ENDPOINT NUMBER	ENDPOINT INDEX	TRANSFER TYPE	ENDPOINT TYPE	DIRECTION	MAX. PACKET SIZE (BYTES)
0	0 1	Control Out Control In	Default	OUT IN	16 16
1	2 3	Generic Out Generic In	Generic Generic	OUT IN	16 16
2	4	Isochronous Out	Isochronous	OUT	128[4]

MODE 2 (ISO-IN MODE):

ENDPOINT NUMBER	ENDPOINT INDEX	TRANSFER TYPE	ENDPOINT TYPE	DIRECTION	MAX. PACKET SIZE (BYTES)
0	0 1	Control Out Control In	Default	OUT IN	16 16
1	2 3	Generic Out Generic In	Generic Generic	OUT IN	16 16
2	5	Isochronous In	Isochronous	IN	128[4]

MODE 3 (ISO-IO MODE):

ENDPOINT NUMBER	ENDPOINT INDEX	TRANSFER TYPE	ENDPOINT TYPE	DIRECTION	MAX. PACKET SIZE (BYTES)
0	0 1	Control Out Control In	Default	OUT IN	16 16
1	2 3	Generic Out Generic In	Generic Generic	OUT IN	16 16
2	4 5	Isochronous Out Isochronous In	Isochronous Isochronous	OUT IN	64[4] 64[4]

NOTES:
1. Generic endpoint can be used either as Bulk or Interrupt endpoint
2. The main endpoint (endpoint number 2) is double-buffered to ease synchronization with the real time applications and to increase throughput.
3. DMA access is for the main endpoint (endpoint number 2) only.
4. Denotes double buffering. The size shown is for a single buffer.

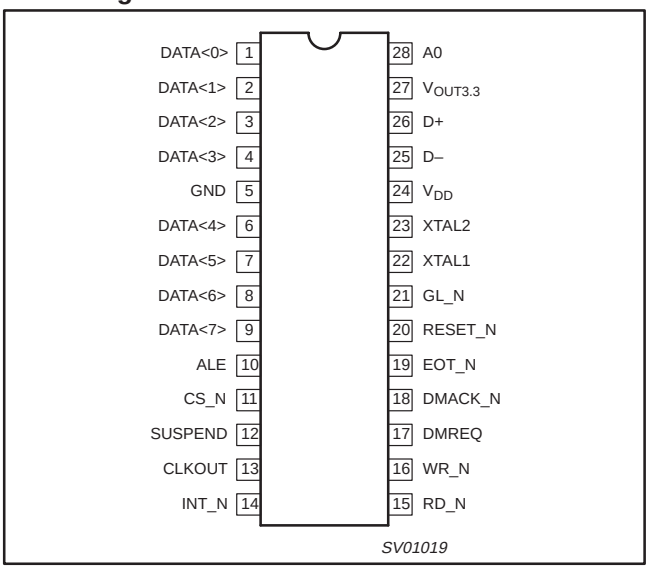
MAIN ENDPOINT

The main endpoint (endpoint number 2) is special in a few ways. It is the primary endpoint for sinking or sourcing relatively large data. As such, it implements a host of features to ease the task of transferring large data:

1. Double buffering. This allows parallel operation between USB access and local CPU access thus increasing throughput. Buffer switching is handled automatically. This results in transparent buffer operation.
2. Supports for DMA (Direct Memory Access) operation. This can be interleaved with normal I/O operation to other endpoints.
3. Automatic pointer handling during DMA operation. No local CPU intervention is necessary when ‘crossing’ the buffer boundary.
4. Configurable for either isochronous transfer or non-isochronous (bulk and interrupt) transfer.

PINNING

Pin configuration



Pin Description

PIN	SYMBOL	TYPE	DESCRIPTION
1	DATA <0>	IO2	Bit 0 of bi-directional data. Slew-rate controlled.
2	DATA <1>	IO2	Bit 1 of bi-directional data. Slew-rate controlled.
3	DATA <2>	IO2	Bit 2 of bi-directional data. Slew-rate controlled.
4	DATA <3>	IO2	Bit 3 of bi-directional data. Slew-rate controlled.
5	GND	P	Ground.
6	DATA <4>	IO2	Bit 4 of bi-directional data. Slew-rate controlled.
7	DATA <5>	IO2	Bit 5 of bi-directional data. Slew-rate controlled.
8	DATA <6>	IO2	Bit 6 of bi-directional data. Slew-rate controlled.
9	DATA <7>	IO2	Bit 7 of bi-directional data. Slew-rate controlled.
10	ALE	I	Address Latch Enable. The falling edge is used to close the latch of the address information in a multiplexed address/ data bus. Permanently tied low for separate address/ data bus configuration.
11	CS_N	I	Chip Select (Active Low).
12	SUSPEND	I,OD4	Device is in Suspend state.
13	CLKOUT	O2	Programmable Output Clock (slew-rate controlled).
14	INT_N	OD4	Interrupt (Active Low).
15	RD_N	I	Read Strobe (Active Low).
16	WR_N	I	Write Strobe (Active Low).
17	DMREQ	O4	DMA Request.
18	DMACK_N	I	DMA Acknowledge (Active Low).
19	EOT_N	I	End of DMA Transfer (Active Low). Double up as Vbus sensing. EOT_N is only valid when asserted together with DMACK_N and either RD_N or WR_N.
20	RESET_N	I	Reset (Active Low and asynchronous). Built-in Power-On-Reset circuit present on chip, so pin can be tied HIGH to V_{CC}.
21	GL_N	OD8	GoodLink LED indicator (Active Low)
22	XTAL1	I	Crystal Connection 1 (6 MHz)
23	XTAL2	O	Crystal Connection 2 (6 MHz). If external clock signal, instead of crystal, is connected to XTAL1, then XTAL2 should be floated.
24	V_{CC}	P	Voltage supply (4.0 – 5.5V). To operate the IC at 3.3V, supply 3.3V to both V_{CC} and $V_{OUT3.3}$ pins.
25	D–	A	USB D– data line
26	D+	A	USB D+ data line
27	$V_{OUT3.3}$	P	3.3V regulated output. To operate the IC at 3.3V, supply a 3.3V to both V_{CC} and $V_{OUT3.3}$ pins
28	A0	I	Address bit. A0=1 selects command instruction; A0=0 selects the data phase. This bit is a don't care in a multiplexed address and data bus configuration and should be tied high.

NOTE:

1. O2 : Output with 2 mA drive
   OD4 : Output Open Drain with 4 mA drive
   OD8 : Output Open Drain with 8 mA drive
   IO2 : Input and Output with 2 mA drive
   O4 : Output with 4mA drive

COMMAND SUMMARY

COMMAND NAME	RECIPIENT	CODING	DATA PHASE
Initialization Commands			
Set Address/Enable	Device	D0h	Write 1 byte
Set Endpoint Enable	Device	D8h	Write 1 byte
Set Mode	Device	F3h	Write 2 bytes
Set DMA	Device	FBh	Write/Read 1 byte
Data Flow Commands			
Read Interrupt Register	Device	F4h	Read 2 bytes
Select Endpoint	Control OUT	00h	Read 1 byte (optional)
	Control IN	01h	Read 1 byte (optional)
	Endpoint 1 OUT	02h	Read 1 byte (optional)
	Endpoint 1 IN	03h	Read 1 byte (optional)
	Endpoint 2 OUT	04h	Read 1 byte (optional)
	Endpoint 2 IN	05h	Read 1 byte (optional)
Read Last Transaction Status	Control OUT	40h	Read 1 byte
	Control IN	41h	Read 1 byte
	Endpoint 1 OUT	42h	Read 1 byte
	Endpoint 1 IN	43h	Read 1 byte
	Endpoint 2 OUT	44h	Read 1 byte
	Endpoint 2 IN	45h	Read 1 byte
Read Buffer	Selected Endpoint	F0h	Read n bytes
Write Buffer	Selected Endpoint	F0h	Write n bytes
Set Endpoint Status	Control OUT	40h	Write 1 byte
	Control IN	41h	Write 1 byte
	Endpoint 1 OUT	42h	Write 1 byte
	Endpoint 1 IN	43h	Write 1 byte
	Endpoint 2 OUT	44h	Write 1 byte
	Endpoint 2 IN	45h	Write 1 byte
Acknowledge Setup	Selected Endpoint	F1h	None
Clear Buffer	Selected Endpoint	F2h	None
Validate Buffer	Selected Endpoint	FAh	None
General Commands			
Send Resume		F6h	None
Read Current Frame Number		F5h	Read 1 or 2 bytes

COMMAND DESCRIPTION

Command Procedure

There are three basic types of commands: Initialization, Data Flow and General commands. Respectively, these are used to initialize the function; for data flow between the function and the host; and some general commands.

Initialization Commands

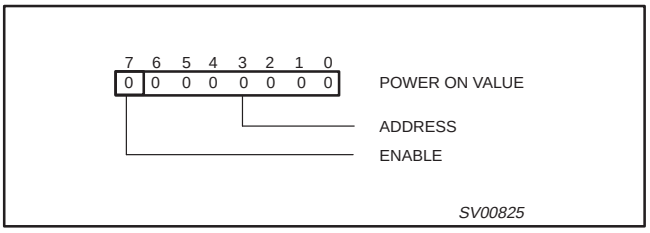
Initialization commands are used during the enumeration process of the USB network. These commands are used to enable the function endpoints. They are also used to set the USB assigned address.

Set Address / Enable

Command : D0h

Data : Write 1 byte

This command is used to set the USB assigned address and enable the function.



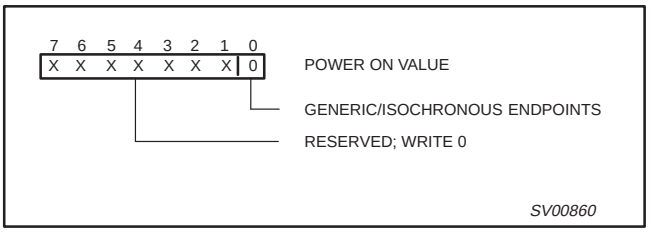
Address	The value written becomes the address.
Enable	A ‘1’ enables this function.

Set Endpoint Enable

Command : D8h

Data : Write 1 byte

The generic/Isochronous endpoints can only be enabled when the function is enabled via the Set Address/Enable command.



Generic/Isochronous Endpoint	A value of ‘1’ indicates the generic/isochronous endpoints are enabled.

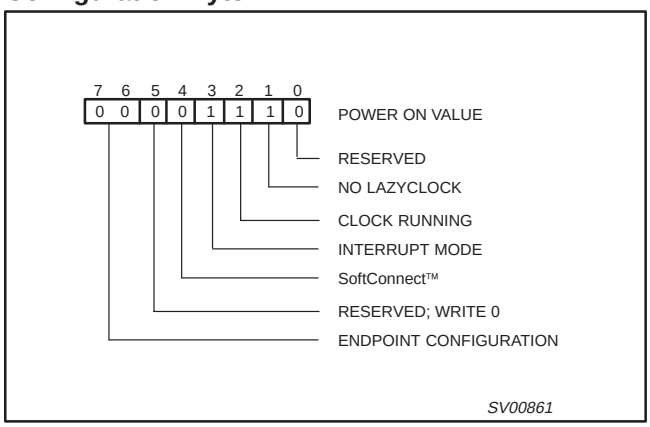
Set Mode

Command : F3h

Data : Write 2 bytes

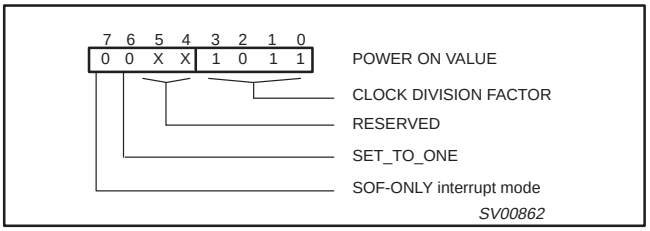
The Set Mode command is followed by two data writes. The first byte contains the configuration byte values. The second byte is the clock division factor byte.

Configuration Byte



No LazyClock	A ‘1’ indicates that CLKOUT will not switch to LazyClock. A ‘0’ indicates that the CLKOUT switches to LazyClock 1ms after the Suspend pin goes high. LazyClock frequency is 30 kHz ± 40%. The programmed value will not be changed by a bus reset.
Clock Running	A ‘1’ indicates that the internal clocks and PLL are always running even during Suspend state. A ‘0’ indicates that the internal clock, crystal oscillator and PLL are stopped whenever not needed. To meet the strict Suspend current requirement, this bit needs to be set to ‘0’. The programmed value will not be changed by a bus reset.
Interrupt Mode	A ‘1’ indicates that all errors and “NAKing” are reported and will generate an interrupt. A ‘0’ indicates that only OK is reported. The programmed value will not be changed by a bus reset.
SoftConnect™	A ‘1’ indicates that the upstream pull-up resistor will be connected if VBUS is available. A ‘0’ means that the upstream resistor will not be connected. The programmed value will not be changed by a bus reset.
Endpoint configuration	These two bits set the endpoint configurations as follows: Mode 0 (Non-ISO Mode) Mode 1 (ISO-OUT Mode) Mode 2 (ISO-IN Mode) Mode 3 (ISO-IO Mode) See Endpoint Description for more details.

Clock Division Factor Byte



Clock Division Factor — The value indicates clock division factor for CLKOUT. The output frequency is 48 MHz/(N+1) where N is the Clock Division Factor. The reset value is 11. This will produce the output frequency of 4 MHz which can then be programmed up (or down) by the user. The minimum value is one giving the range of frequency from 4 to 24 MHz. The minimum value of N is ZERO giving a maximum frequency of 48 MHz. The maximum value of N is ELEVEN giving a minimum frequency of 4 MHz. The PDIUSBD12 design ensures no glitching during frequency change. The programmed value will not be changed by a bus reset.

SET_TO_ONE — This bit needs to be set to 1 prior to any DMA read or DMA write operation. This bit should always be set to 1 after power. It is zero after power–on reset.

SOF-ONLY interrupt mode — Setting this bit to 1 will cause the interrupt line to be interrupted due to Start of Frame clock (SOF) ONLY, regardless of the setting of pin-interrupt mode, bit 5 of setDMA.

Set DMA

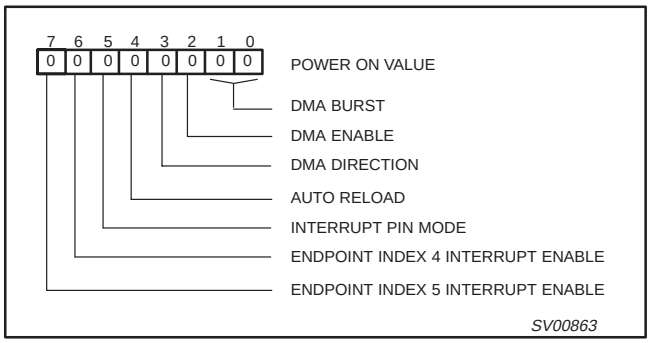
Command : FBh

Data : Read/Write 1 byte

The set DMA command is followed by one data write/read to/from the DMA configuration register.

DMA Configuration register

During DMA operation, the two-byte buffer header (status and byte length information) is not transferred to/from the local CPU. This allows DMA data to be continuous and not interleaved by chunks of these headers. For DMA read operation, the header will be skipped by the PDIUSBD12. See Read Buffer command. For DMA write operation, the header will be automatically added by the PDIUSBD12. This provides for a clean and simple DMA data transfer.



DMA Burst — Selects the burst length for DMA operation:

00	Single cycle DMA
01	Burst (4 cycle) DMA
10	Burst (8 cycle) DMA
11	Burst (16 cycle) DMA

DMA Enable — Writing a ‘1’ to this bit will start DMA operation through the assertion of DMREQ. The main endpoint buffer needs to be full (for DMA Read) or empty (for DMA Write) before DMREQ will be asserted. In a single cycle DMA mode, the DMREQ is deactivated upon receiving DMACK_N. In burst mode DMA, the DMREQ is deactivated after the number of burst is exhausted. It is then asserted again for the next burst. This process continues until EOT_N is asserted together with DMACK_N and either RD_N or WR_N which will reset this bit to ‘0’ and terminate the DMA operation. The DMA operation can also be terminated by writing a ‘0’ to this bit.

DMA Direction — This bit determines the direction of data flow during a DMA transfer. A ‘1’ means external shared memory to PDIUSBD12 (DMA Write); a ‘0’ means PDIUSBD12 to the external shared memory (DMA Read).

Auto Reload — When this bit is set to ‘1’, the DMA operation will automatically restart.

Interrupt Pin Mode — A ‘0’ signifies a normal interrupt pin mode where interrupt is generated as a logical OR of all the bits in the interrupt registers. A ‘1’ signifies that the interrupt will occur when Start of Frame clock (SOF) is seen on the upstream USB bus. The other normal interrupts are still active.

Endpoint Index 4 Interrupt Enable — A ‘1’ allows for interrupt to be generated whenever the endpoint buffer contains a valid packet. Normally turned off for DMA operation to reduce unnecessary CPU servicing.

Endpoint Index 5 Interrupt Enable — A ‘1’ allows for interrupt to be generated whenever the endpoint buffer is validated (see the Validate Buffer command). Normally turned off for DMA operation to reduce unnecessary CPU servicing.

INTERRUPT MODES

Bit 7 of Clock Division Factor SOF_ONLY interrupt mode	Bit 5 of SetDMA INTERRUPT_PIN mode	Types of Interrupt
0	0	Normal Interrupt[1]
0	1	Normal Interrupt + SOF[1]
1	X	SOF interrupt ONLY

NOTE:
1. Normal Interrupt: Normal interrupts from Interrupt Register :

Data Flow Commands

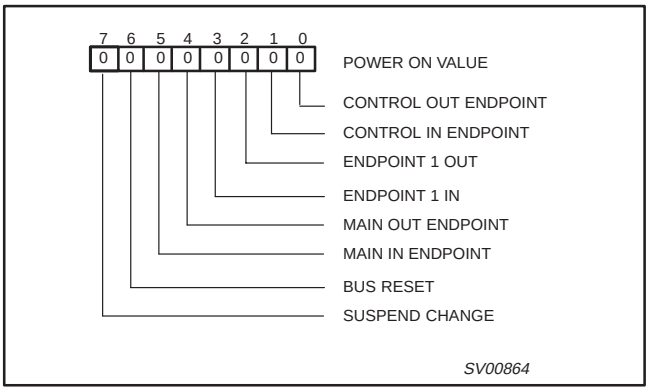
Data flow commands are used to manage the data transmission between the USB endpoints and the external microcontroller. Much of the data flow is initiated via an interrupt to the microcontroller. The microcontroller utilizes these commands to access and determine whether the endpoint FIFOs have valid data.

Read Interrupt Register

Command : F4h

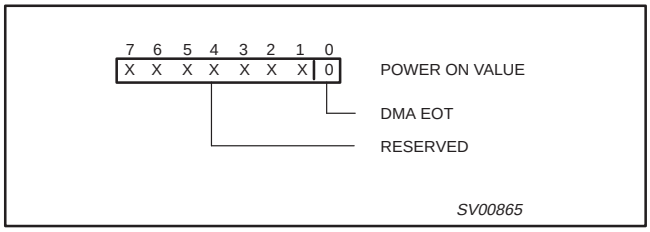
Data : Read 2 bytes

Interrupt Register Byte 1



Interrupt Register Byte 2

This command indicates the origin of an interrupt. The endpoint interrupt bits (bits 0 to 5) are cleared by reading the endpoint last transaction status register through Read Last Transaction Status command. The other bits are cleared after reading the interrupt registers.



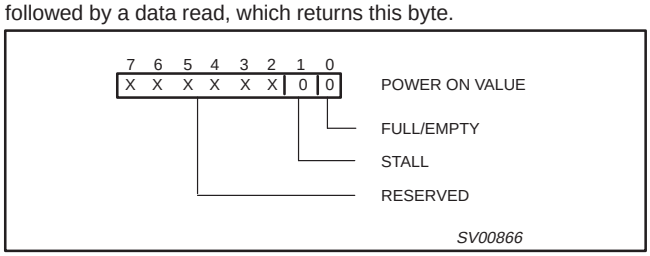
Bus Reset	After a bus reset an interrupt will be generated this bit will be ‘1’. A bus reset is identical to a hardware reset through the RESET_N pin with the exception that a bus reset generates an interrupt notification and the device is enabled at default address 0.
Suspend Change	When the PDIUSBD12 did not receive 3 SOFs, it will go into suspend state and the Suspend Change bit will be high. Any change to the suspend or awake state will set this bit high and generate an interrupt.
DMA EOT	This bit signifies that DMA operation is completed.

Select Endpoint

Command : 00-05h

Data : Optional Read 1 byte

The Select Endpoint command initializes an internal pointer to the start of the Selected buffer. Optionally, this command can be followed by a data read, which returns this byte.



Full/Empty	A ‘1’ indicates the buffer is full, ‘0’ indicates an empty buffer.
Stall	A ‘1’ indicates the selected endpoint is in the stall state.

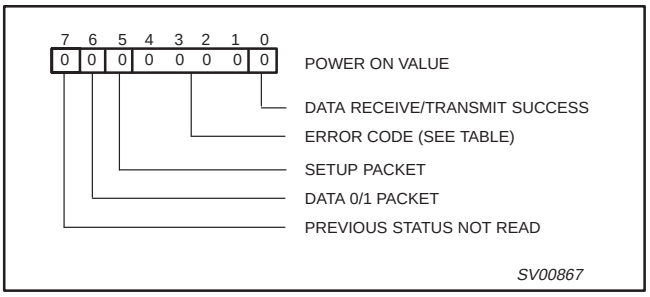
Read Last Transaction Status Register

Command : 40–45h

Data : Read 1 byte

The Read Last Transaction Status command is followed by one data read that returns the status of the last transaction of the endpoint. This command also resets the corresponding interrupt flag in the interrupt register, and clears the status, indicating that it was read.

This command is useful for debugging purposes. Since it keeps track of every transaction, the status information is overwritten for each new transaction.



Data Receive/Transmit Success	A ‘1’ indicates data has been received or transmitted successfully.
Error Code	See Table below, Error Codes.
Setup Packet	A ‘1’ indicates the last successful received packet had a SETUP token (this will always read ‘0’ for IN buffers).
Data 0/1 Packet	A ‘1’ indicates the last successful received or sent packet had a DATA1 PID.
Previous Status not Read	A ‘1’ indicates a second event occurred before the previous status was read.

ERROR CODES

ERROR CODE	RESULT
0000	No Error
0001	PID encoding Error; bits 7–4 are not the inversion of bits 3–0
0010	PID unknown; encoding is valid, but PID does not exist
0011	Unexpected packet; packet is not of the type expected (= token, data or acknowledge), or SETUP token to a non-control endpoint
0100	Token CRC Error
0101	Data CRC Error
0110	Time Out Error
0111	Never happens
1000	Unexpected End-of-packet
1001	Sent or received NAK
1010	Sent Stall, a token was received, but the endpoint was stalled
1011	Overflow Error, the received packet was longer than the available buffer space
1101	Bitstuff Error
1111	Wrong DATA PID; the received DATA PID was not the expected one

Read Buffer

Command : F0h

Data : Read multiple bytes (max 130)

The Read Buffer command is followed by a number of data reads, which return the contents of the selected endpoint data buffer. After each read, the internal buffer pointer is incremented by 1.

The buffer pointer is not reset to the buffer start by the Read Buffer command. This means that reading or writing a buffer can be interrupted by any other command (except for Select Endpoint).

The data in the buffer are organized as follows:

byte 0: Reserved: can have any value

byte 1: Number/length of data bytes

byte 2: Data byte 1

byte 3: Data byte 2

. . . . . .

The first two bytes will be skipped in the DMA read operation. Thus, the first read will get Data Byte 1, the second read will get Data Byte 2, etc. The PDIUSBD12 can determine the last byte of this packet through the EOP termination of the USB packet.

Write Buffer

Command : F0h

Data : Write multiple bytes (max 130)

The Write Buffer command is followed by a number of data writes, which load the endpoints buffer. The data must be organized in the same way as described in the Read Buffer command. The first byte (reserved) should always be '0'.
During DMA write operation, the first two bytes will be bypassed. Thus, the first write will write into Data Byte 1, the second write will write into Data Byte 2, etc. For non-isochronous transfer (bulk or interrupt), the buffer should be completely filled before the data is sent to the host and a switch to the next buffer occurs. The exception is at the end of DMA transfer indicated by activation of EOT_N, when the current buffer content (completely full or not) will be sent to the host.

WARNING:
There is no protection against writing or reading over a buffer's boundary or against writing into an OUT buffer or reading from an IN buffer. Any of these actions could cause an incorrect operation. Data in an OUT buffer are only meaningful after a successful transaction. The exception is during DMA operation on the main endpoint (endpoint 2); in which case the pointer is automatically pointed to the second buffer after reaching the boundary (double buffering scheme).

Clear Buffer

Command : F2h

Data : None

When a packet is received completely, an internal endpoint buffer full flag is set. All subsequent packets will be refused by returning a NAK. When the microcontroller has read the data, it should free the buffer by the Clear Buffer command. When the buffer is cleared, new packets will be accepted.

Validate Buffer

Command : FAh

Data : None

When the microprocessor has written data into an IN buffer, it should set the buffer full flag by the Validate Buffer command. This indicates that the data in the buffer are valid and can be sent to the host when the next IN token is received.

Set Endpoint Status

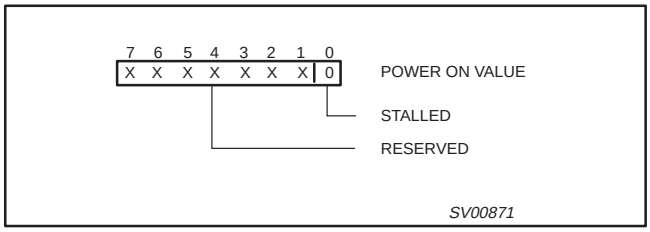
Command : 40–45h

Data : Write 1 byte

A stalled control endpoint is automatically unstalled when it receives a SETUP token, regardless of the content of the packet. If the endpoint should stay in its stalled state, the microcontroller can re-stall it.

When a stalled endpoint is unstalled (either by the Set Endpoint Status command or by receiving a SETUP token), it is also re-initialized. This flushes the buffer and if it is an OUT buffer it waits for a DATA 0 PID, if it is an IN buffer it writes a DATA 0 PID.

Even when unstalled, writing Set Endpoint Status to '0' initializes the endpoint.



Stalled A '1' indicates the endpoint is stalled.

Acknowledge Setup

Command : F1h

Data : None

The arrival of a SETUP packet flushes the IN buffer and disables the Validate Buffer and Clear Buffer commands for both IN and OUT endpoints.

The microcontroller needs to re-enable these commands by the Acknowledge Setup command. This ensures that the last SETUP packet stays in the buffer and no packet can be sent back to the host until the microcontroller has acknowledged explicitly that it has seen the SETUP packet.

The microcontroller must send the Acknowledge Setup command to both the IN and OUT endpoints.

GENERAL COMMANDS

Send Resume

Command : F6h

Data : None

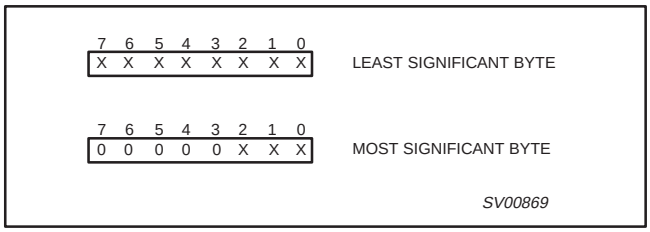
Sends an upstream resume signal for 10 ms. This command is normally issued when the device is in suspend. The RESUME command is not followed by a data read or write.

Read Current Frame Number

Command : F5h

Data : Read One or Two Bytes

This command is followed by one or two data reads and returns the frame number of the last successfully received SOF. The frame number is returned Least Significant Byte first.



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{CC1}	DC supply voltage (Main mode)	Apply V_{CC1} to V_{CC} pin only	3.6	5.5	V
V_{CC2}	DC supply voltage (Alternate mode)	Apply V_{CC2} to both V_{CC} and $V_{out3.3}$ pins	3.0	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input voltage range for I/O		0	5.5	V
$V_{AI/O}$	DC input voltage range for analog I/O		0	3.6	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	–40	85	°C

DC CHARACTERISTICS (Digital pins)

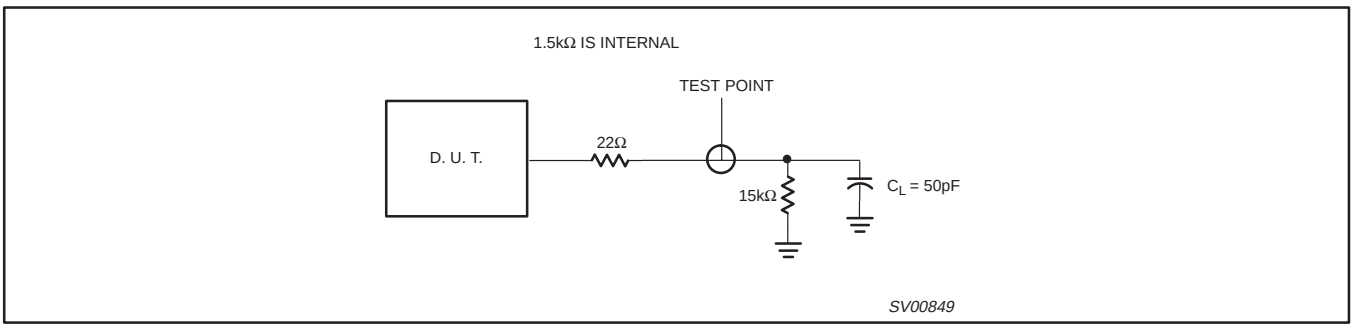
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Levels						
V_{IL}	LOW level input voltage				0.8	V
VIH	HIGH level input voltage		2.0			V
V_{HYS}	Hysteresis voltage	ST (Schmitt Trigger) pins	0.4		0.7	V
Output Levels						
V_{OL}	LOW level output voltage	I_{OL} = rated drive I_{OL} = 20 µA			0.4 0.1	V V
V_{OH}	HIGH level output voltage	I_{OH} = rated drive I_{OH} = 20 µA	2.4 V_{CC} – 0.1			V V
Leakage Current						
I_{OZ}	OFF state current	OD (Open Drain) pins			±5	µA
I_L	Input leakage current				±5	µA
I_S	Suspend current	Oscillator stopped and inputs to GND/V_{CC}			15	µA
I_O	Operating current			15		mA

DC CHARACTERISTICS (AI/O pins)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Leakage Current					
I_{LO}	Hi-Z state data line leakage	0V < V_{IN} < 3.3V		±10	µA
Input Levels					
V_{DI}	Differential input sensitivity	|(D+) – (D–)|	0.2		V
V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	2.5	V
V_{SE}	Single-ended receiver threshold		0.8	2.0	V
Output Levels					
V_{OL}	Static output LOW	R_L of 1.5kΩ to 3.6V		0.3	V
V_{OH}	Static output HIGH	R_L of 15kΩ to GND	2.8	3.6	V
Capacitance					
C_{IN}	Transceiver capacitance	Pin to GND		20	pF
Output Resistance					
Z_{DRV}[1]	Driver output resistance	Steady state drive	29	44	Ω
Pull-up Resistance					
Z_{PU}	Pull-up resistance	SoftConnect™ = ON	1.1	1.9	kΩ

NOTE:
1. Includes external resistors of 18 Ω ± 1% each on D+ and D–.

LOAD FOR D+/D–



AC CHARACTERISTICS (AI/O pins, FULL speed)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Driver characteristics		C_L = 50pF; R_{pu} = 1.5kΩ on D+ to V_{CC}			
	Transition Time:				
t_r	Rise time	Between 10% and 90%	4	20	ns
t_f	Fall time		4	20	ns
t_{RFM}	Rise/fall time matching	(t_r/t_f)	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V
Driver Timings					
t_{EOPT}	Source EOP width	Figure 1	160	175	ns
t_{DEOP}	Differential data to EOP transition skew	Figure 1	–2	5	ns
Receiver Timings:					
	Receiver Data Jitter Tolerance	Characterized but not implemented as production test. Guaranteed by design.			
t_{JR1}	To next transition		–18.5	18.5	ns
t_{JR2}	For paired transitions		–9	9	ns
	EOP Width at Receiver				
t_{EOPR1}	Must reject as EOP	Figure 1	40		ns
t_{EOPR2}	Must accept		82		ns

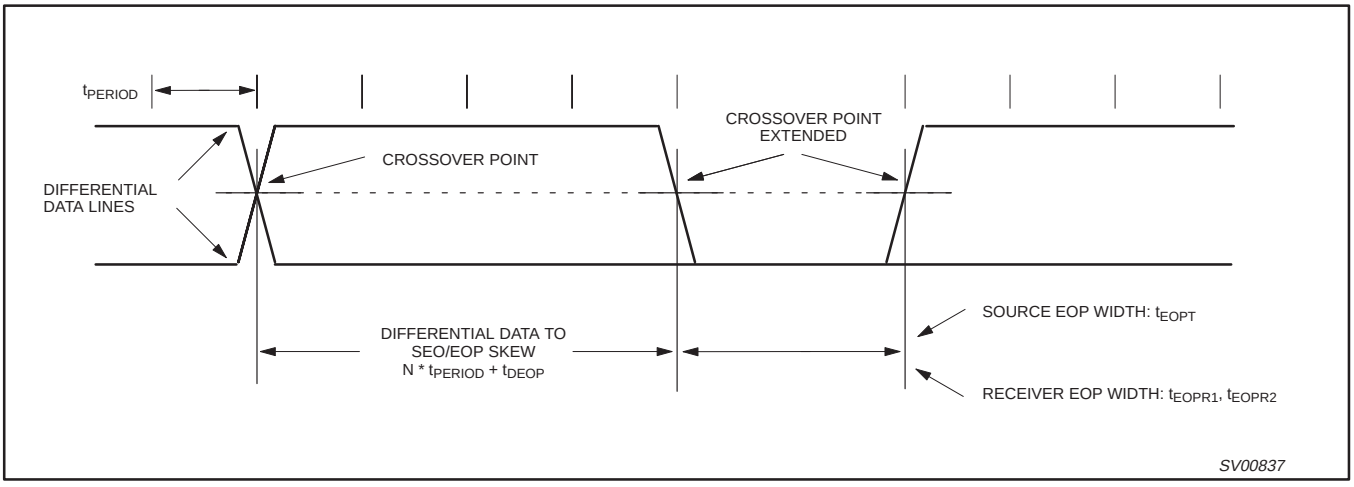


Figure 1. Differential data to EOP transition skew and EOP width

AC CHARACTERISTICS (Parallel Interface)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ALE Timings					
t_{LH}	ALE High pulse width		20		ns
t_{AVLL}	Address Valid to ALE Low time		10		ns
t_{LLAX}	ALE Low to Address transition time			10	ns
Write Timings					
t_{CLWL}	CS_N (DMACK_N) Low to WR_N Low time		0[1]		ns
t_{WHCH}	WR_N High to CS_N (DMACK_N) High time		5		ns
t_{AVWL}	A0 Valid to WR_N Low time		0[1]		ns
			130[2]		ns
t_{WHAX}	WR_N High to A0 transition time		5		ns
t_{WL}	WR_N Low pulse width		20		ns
t_{WDSU}	Write Data Setup time		30		ns
t_{WDH}	Write Data Hold time		10		ns
t_{WC}	Write Cycle time		500		ns
Read Timings					
t_{CLRL}	CS_N (DMACK_N) Low to RD_N Low time		0[1]		ns
			130[2]		ns
t_{RHCH}	RD_N High to CS_N (DMACK_N) High time		5		ns
t_{AVRL}	A0 Valid to RD_N Low time		0[1]		ns
t_{RL}	RD_N Low pulse width		20		ns
t_{RLDD}	RD_N Low to Data Driven time			20	ns
t_{RHDZ}	RD_N High to Data Hi–Z time			20	ns
t_{RC}	Read Cycle time		500		ns

NOTES:
1. Can be negative.
2. For DMA access only on the Modulo 64th byte and the Second Last (EOT-1) byte.

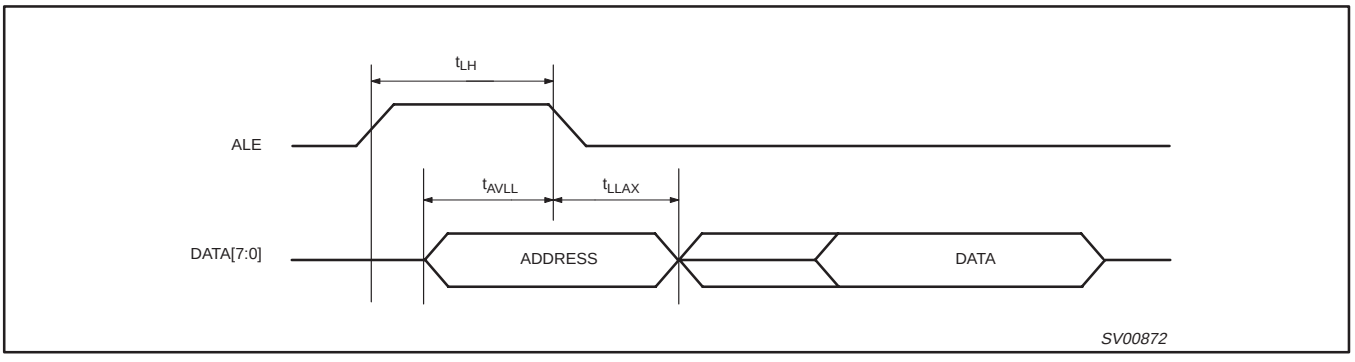


Figure 2. ALE Timing

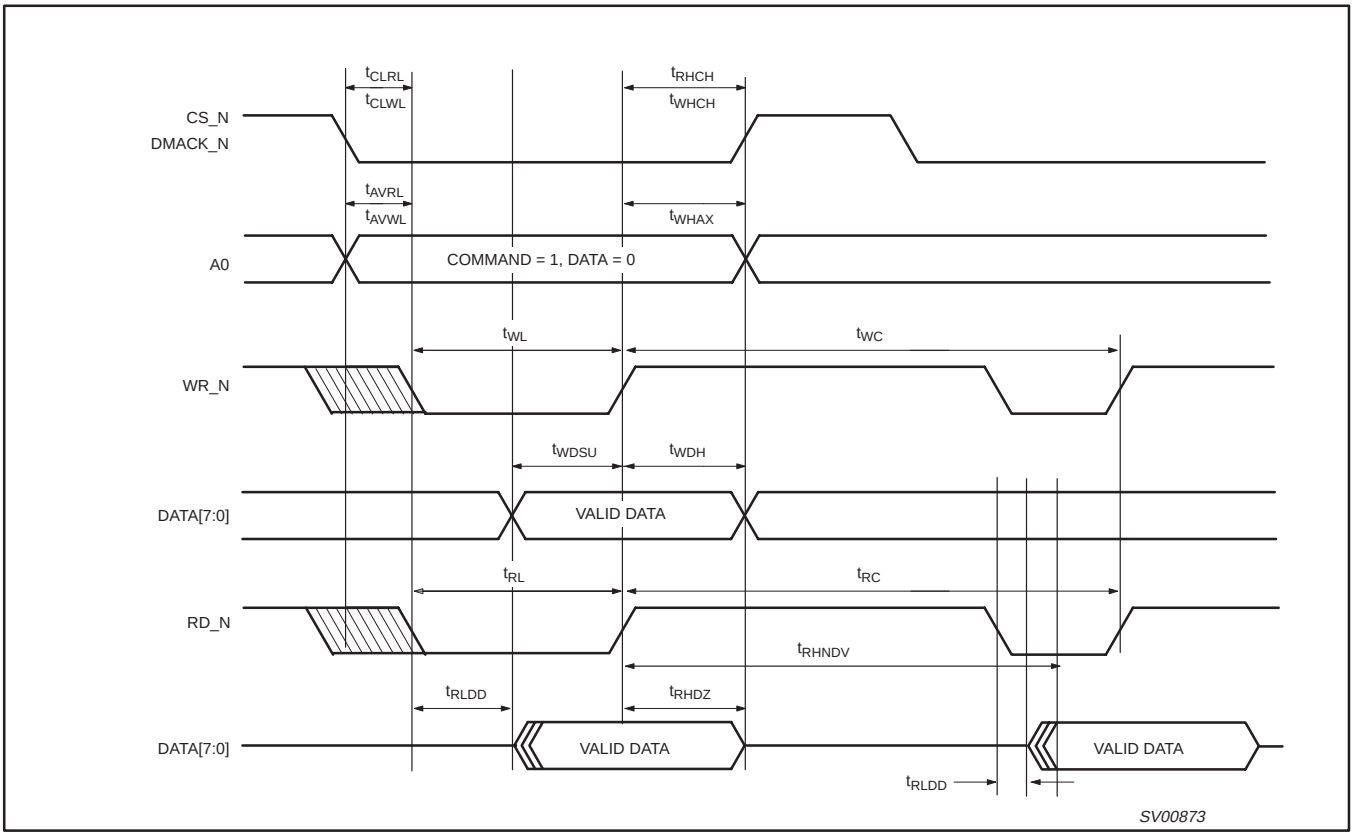
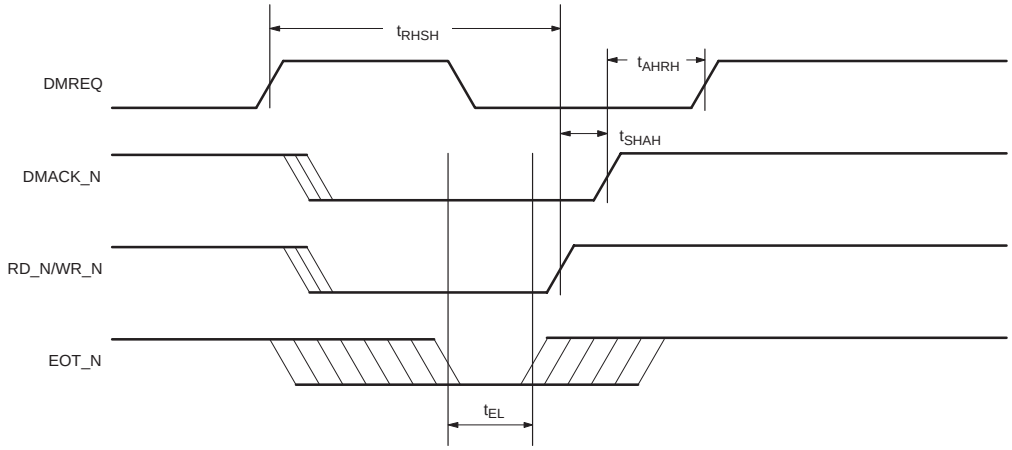


Figure 3. Parallel Interface TIming (I/O and DMA)

AC CHARACTERISTICS (DMA)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Single-cycle DMA Timings					
t_{AHRH}	DMACK_N High to DMREQ High time			330	ns
t_{SHAH}	RD_N/WR_N High to DMACK_N High time		130		ns
t_{RHSH}	DMREQ High to RD_N/WR_N High time		120		ns
t_{EL}	EOT_N Low Pulse Width (Simultaneous DMACK_N, RD_N/WR_N and EOT_N low time)		10		ns
Burst DMA Timings					
t_{SLRL}	RD_N/WR_N Low to DMREQ Low time			40	ns
t_{RHNDV}	RD_N (only) High to next data valid			420	ns
EOT Timings					
t_{ELRL}	EOT_N Low to DMREQ Low time			40	ns



NOTES:
EOT_N is considered valid when DMACK_N, RD_N/WR_N and EOT_N are all LOW.
t_{ALRL} timing starts from the DMACK_N or RD_N/RW_N depending which goes LOW later.

Figure 4. Single-cycle DMA Timing

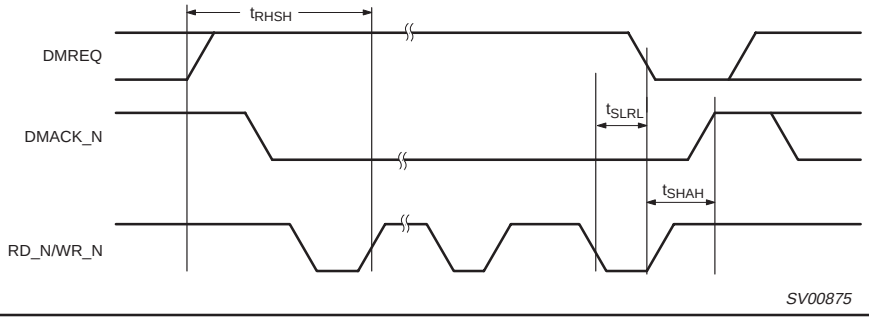


Figure 5. Burst DMA Timing

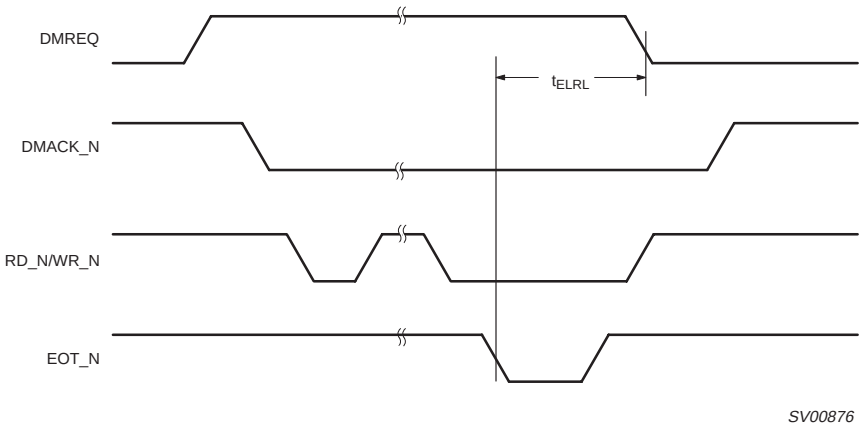
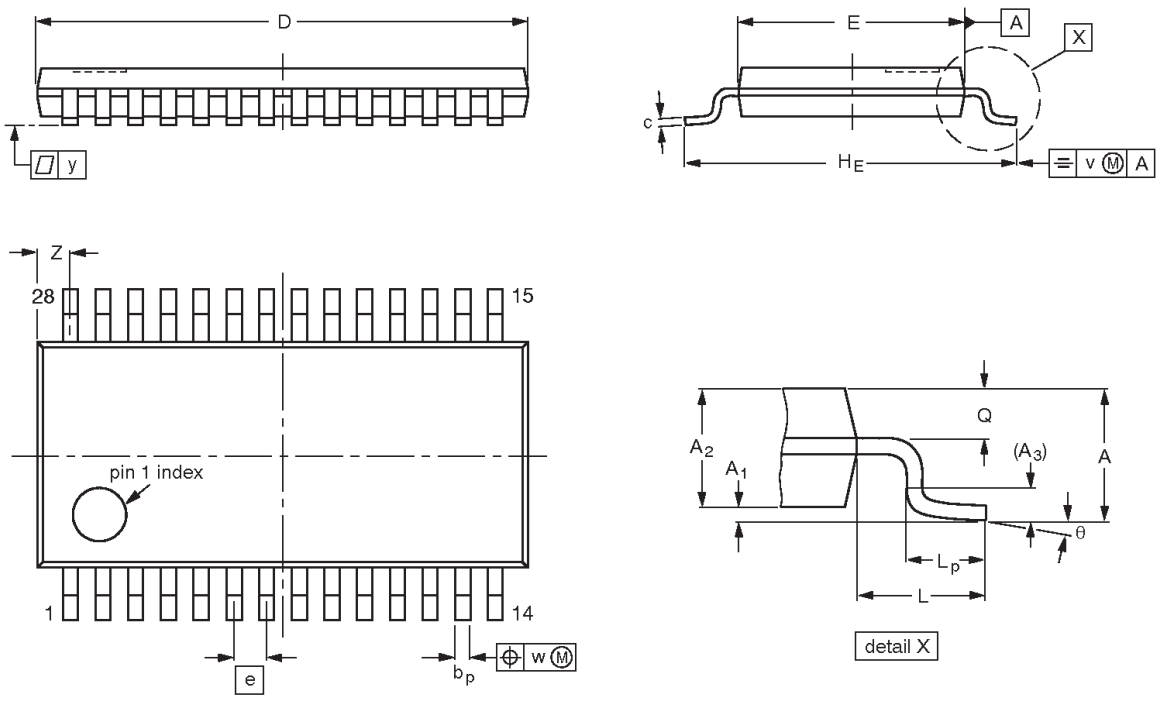
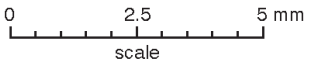


Figure 6. DMA Terminated by EOT

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm SOT361-1





DIMENSIONS (mm are the original dimensions)

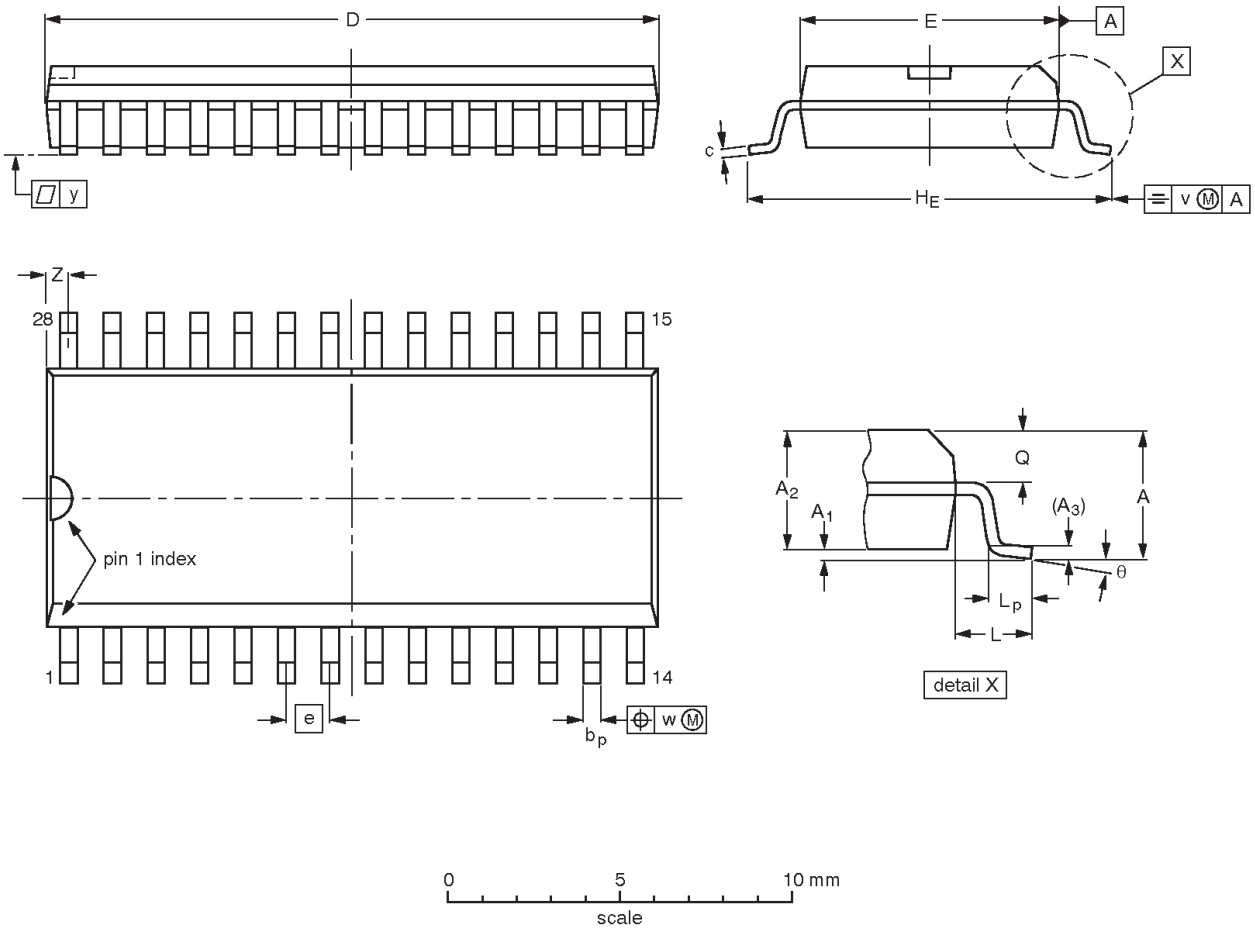
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT361-1		MO-153AE				~~93-06-16~~ 95-02-04

SO28: plastic small outline package; 28 leads; body width 7.5mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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