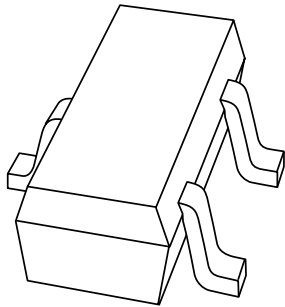


DATA SHEET



PDTA123JE

PNP resistor-equipped transistor

Product specification
Supersedes data of 1997 Dec 15

1998 Nov 25

PNP resistor-equipped transistor

PDTA123JE

FEATURES

- Built-in bias resistors R1 and R2 (typ. 2.2 kΩ and 47 kΩ respectively)
- Simplification of circuit design
- Reduces number of components and board space.

APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of external resistors.

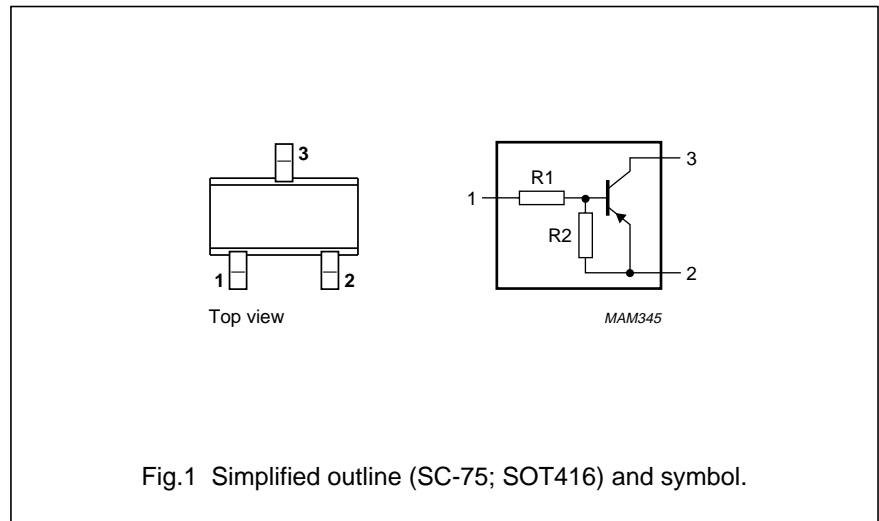


Fig.1 Simplified outline (SC-75; SOT416) and symbol.

DESCRIPTION

PNP resistor-equipped transistor in a SC-75 (SOT416) plastic package. NPN complement: PDTA123JE.

PINNING

| PIN | DESCRIPTION |
|-----|--------------------|
| 1 | base/input |
| 2 | emitter/ground (+) |
| 3 | collector/output |

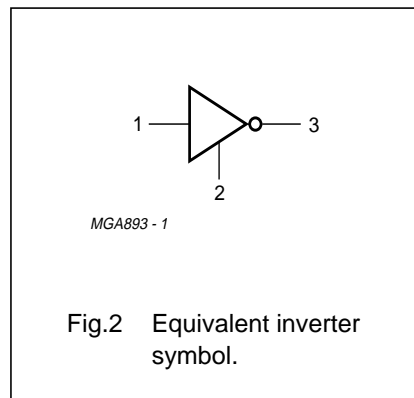


Fig.2 Equivalent inverter symbol.

MARKING

| TYPE NUMBER | MARKING CODE |
|-------------|--------------|
| PDTA123JE | 27 |

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------|---------------------------|---|------|------|------|------|
| V_{CEO} | collector-emitter voltage | open base | – | – | –50 | V |
| I_O | output current (DC) | | – | – | –100 | mA |
| I_{CM} | peak collector current | | – | – | –100 | mA |
| P_{tot} | total power dissipation | $T_{amb} \leq 25\text{ }^\circ\text{C}$ | – | – | 150 | mW |
| h_{FE} | DC current gain | $I_C = -10\text{ mA}; V_{CE} = -5\text{ V}$ | 100 | – | – | |
| R1 | input resistor | | 1.54 | 2.2 | 2.86 | kΩ |
| $\frac{R2}{R1}$ | resistor ratio | | 17 | 21 | 26 | |

PNP resistor-equipped transistor

PDTA123JE

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|-------------------------------|--------------------------------------|------|------|------|
| V_{CBO} | collector-base voltage | open emitter | – | –50 | V |
| V_{CEO} | collector-emitter voltage | open base | – | –50 | V |
| V_{EBO} | emitter-base voltage | open collector | – | –10 | V |
| V_i | input voltage | | | | |
| | positive | | – | +5 | V |
| | negative | | – | –12 | V |
| I_O | output current (DC) | | – | –100 | mA |
| I_{CM} | peak collector current | | – | –100 | mA |
| P_{tot} | total power dissipation | $T_{amb} \leq 25\text{ °C}$; note 1 | – | 150 | mW |
| T_{stg} | storage temperature | | –65 | +150 | °C |
| T_j | junction temperature | | – | 150 | °C |
| T_{amb} | operating ambient temperature | | –65 | +150 | °C |

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---------------|---|------------|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient | note 1 | 833 | K/W |

Note

1. Transistor mounted on an FR4 printed-circuit board.

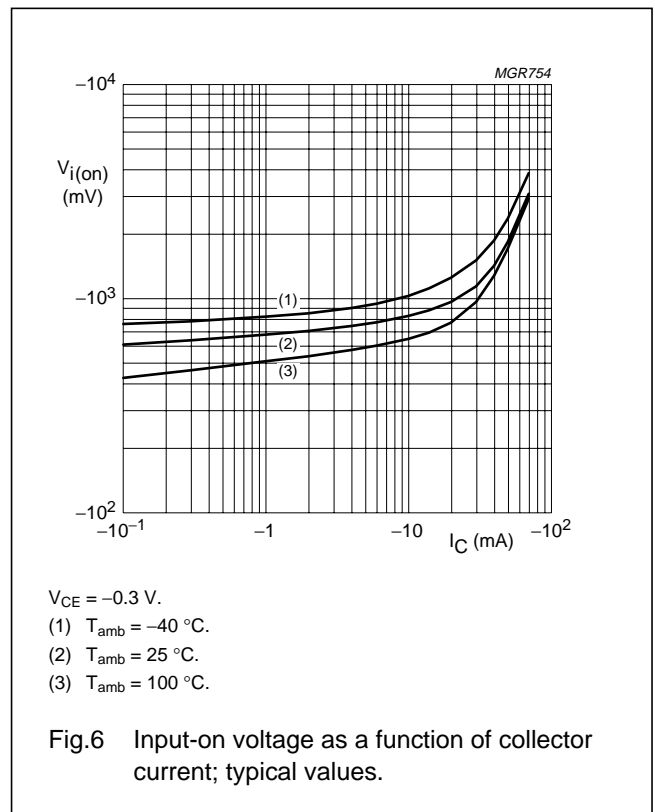
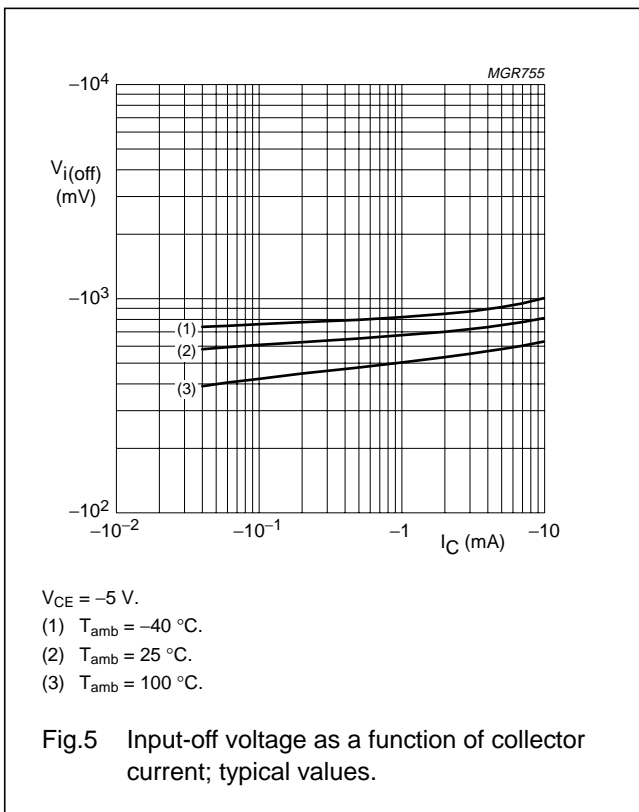
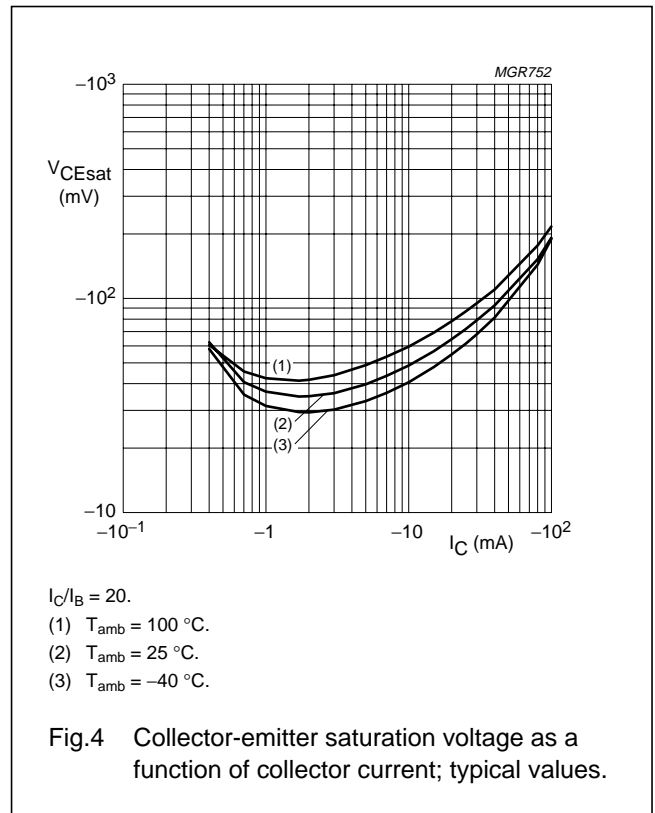
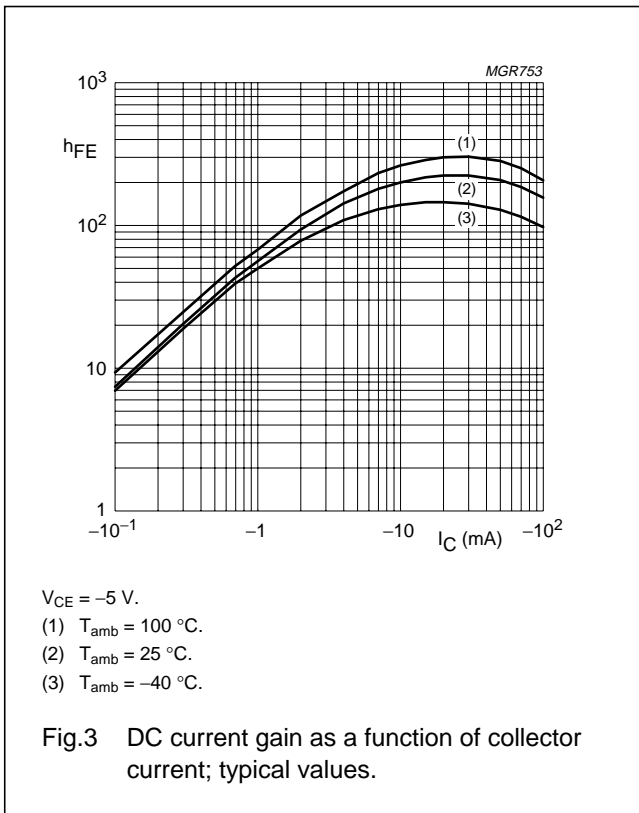
CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|--|------|------|------|---------------|
| I_{CBO} | collector cut-off current | $I_E = 0$; $V_{CB} = -50\text{ V}$ | – | – | –100 | nA |
| I_{CEO} | collector cut-off current | $I_B = 0$; $V_{CE} = -30\text{ V}$ | – | – | –1 | μA |
| | | $I_B = 0$; $V_{CE} = -30\text{ V}$; $T_j = 150\text{ °C}$ | – | – | –50 | μA |
| I_{EBO} | emitter cut-off current | $I_C = 0$; $V_{EB} = -5\text{ V}$ | – | – | –180 | μA |
| h_{FE} | DC current gain | $I_C = -10\text{ mA}$; $V_{CE} = -5\text{ V}$ | 100 | – | – | |
| V_{CEsat} | collector-emitter saturation voltage | $I_C = -5\text{ mA}$; $I_B = -0.25\text{ mA}$ | – | – | –100 | mV |
| $V_{i(off)}$ | input-off voltage | $I_C = -100\text{ }\mu\text{A}$; $V_{CE} = -5\text{ V}$ | – | –600 | –500 | mV |
| $V_{i(on)}$ | input-on voltage | $I_C = -5\text{ mA}$; $V_{CE} = -300\text{ mV}$ | –1.1 | –1.1 | – | V |
| R1 | input resistor | | 1.54 | 2.2 | 2.86 | k Ω |
| $\frac{R2}{R1}$ | resistor ratio | | 17 | 21 | 26 | |
| C_c | collector capacitance | $I_E = I_B = 0$; $V_{CB} = -10\text{ V}$; $f = 1\text{ MHz}$ | – | – | 3 | pF |

PNP resistor-equipped transistor

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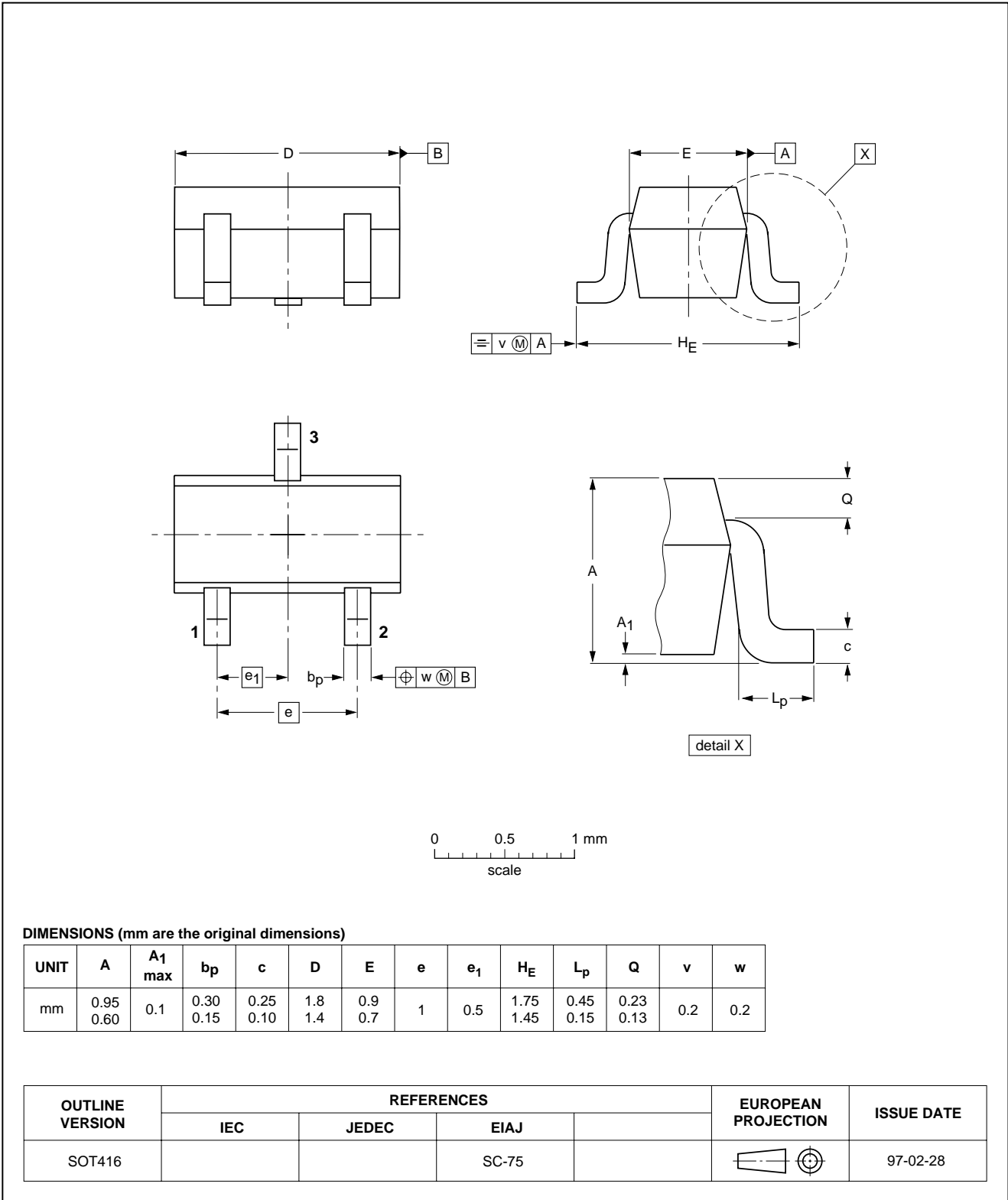
PNP resistor-equipped transistor

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PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT416



PNP resistor-equipped transistor

PDTA123JE

DEFINITIONS

| Data Sheet Status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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PNP resistor-equipped transistor

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Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

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France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS, Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

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Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399

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Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

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Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919

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