

# DATA SHEET

## **PHC2300**

Complementary enhancement  
mode MOS transistors

Product specification  
Supersedes data of 1997 Jun 19  
File under Discrete Semiconductors, SC13b

1997 Oct 24

# Complementary enhancement mode MOS transistors

PHC2300

**FEATURES**

- High-speed switching
- No secondary breakdown.

**APPLICATIONS**

- Universal line interface in telephone sets
- Relay, high-speed and line transformer drivers.

**DESCRIPTION**

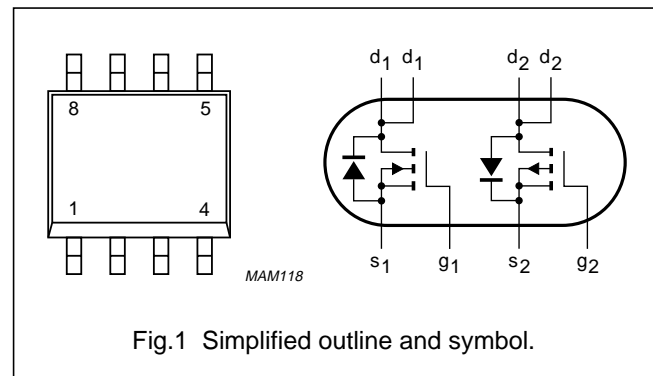
One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

**PINNING - SOT96-1 (SO8)**

PIN	SYMBOL	DESCRIPTION
1	s <sub>1</sub>	source 1
2	g <sub>1</sub>	gate 1
3	s <sub>2</sub>	source 2
4	g <sub>2</sub>	gate 2
5	d <sub>2</sub>	drain 2
6	d <sub>2</sub>	drain 2
7	d <sub>1</sub>	drain 1
8	d <sub>1</sub>	drain 1

**CAUTION**

The device is supplied in an antistatic package.  
The gate-source input must be protected against static discharge during transport or handling.



**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per FET</b>					
V <sub>DS</sub>	drain-source voltage (DC) N-channel P-channel		–	300 –300	V V
V <sub>GS</sub>	gate-source voltage (DC)		–	±20	V
V <sub>GSth</sub>	gate-source threshold voltage N-channel P-channel	V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = 1 mA V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = –1 mA	0.8 –0.8	2 –2	V V
I <sub>D</sub>	drain current (DC) N-channel P-channel	T <sub>s</sub> = 80 °C	–	340 –235	mA mA
R <sub>DSon</sub>	drain-source on-state resistance N-channel P-channel	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 170 mA V <sub>GS</sub> = –10 V; I <sub>D</sub> = –115 mA	–	8 17	Ω Ω
P <sub>tot</sub>	total power dissipation	T <sub>s</sub> = 80 °C	–	1.6	W

# Complementary enhancement mode MOS transistors

PHC2300

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

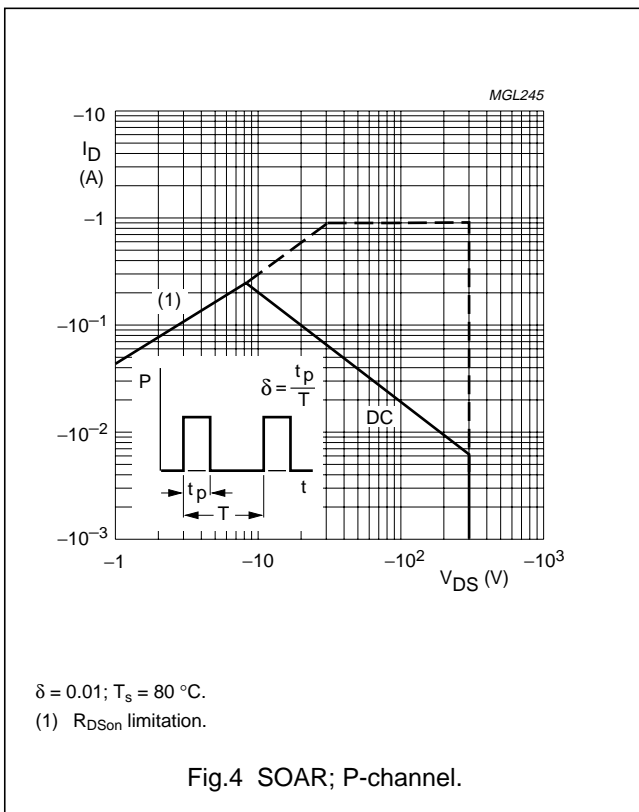
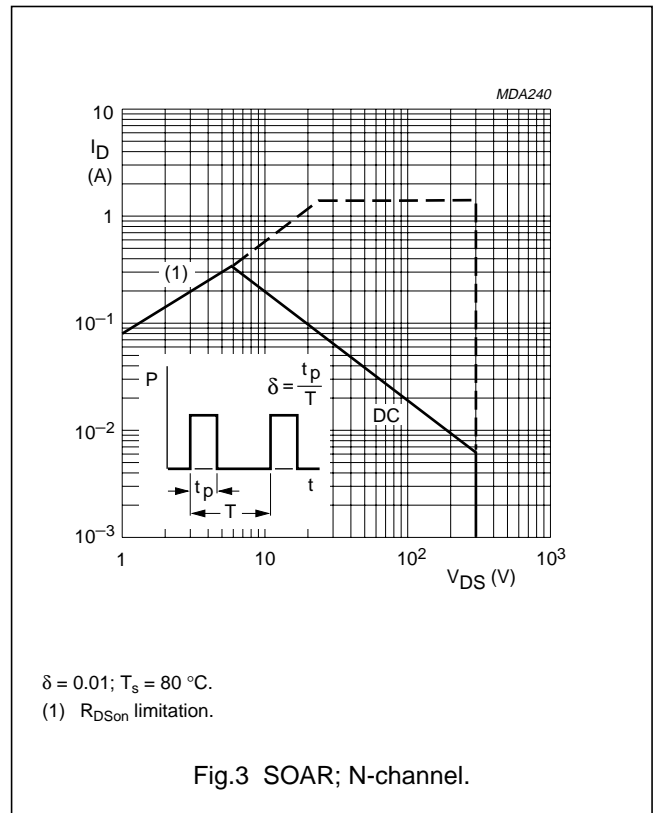
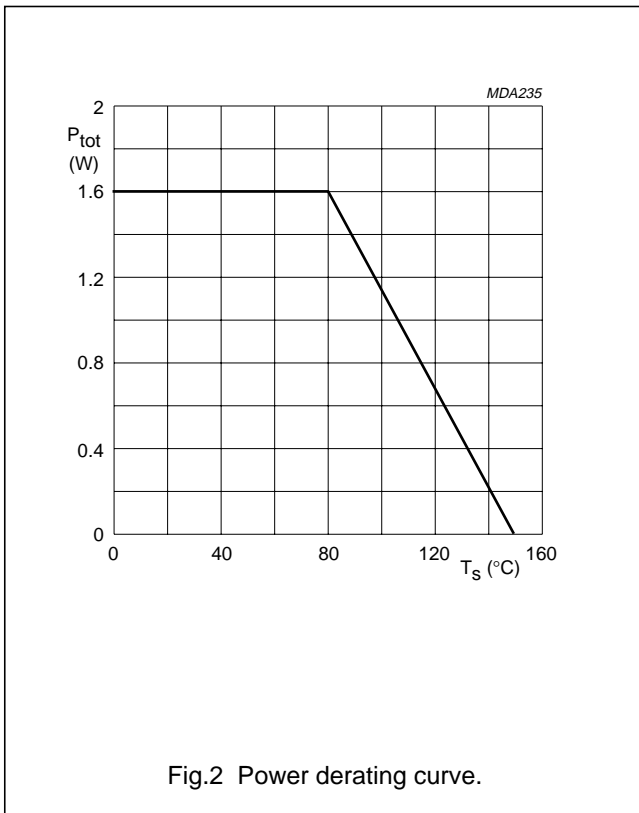
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per FET</b>					
V <sub>DS</sub>	drain-source voltage (DC)				
	N-channel		–	300	V
	P-channel		–	–300	V
V <sub>GS</sub>	gate-source voltage (DC)		–	±20	V
I <sub>D</sub>	drain current (DC)	T <sub>s</sub> = 80 °C; note 1			
	N-channel		–	340	mA
	P-channel		–	–235	mA
I <sub>DM</sub>	peak drain current	note 2			
	N-channel		–	1.4	A
	P-channel		–	–0.9	A
P <sub>tot</sub>	total power dissipation	T <sub>s</sub> = 80 °C; note 3	–	1.6	W
		T <sub>amb</sub> = 25 °C; note 4	–	1.8	W
		T <sub>amb</sub> = 25 °C; note 5	–	0.9	W
		T <sub>amb</sub> = 25 °C; note 6	–	1.2	W
T <sub>stg</sub>	storage temperature		–55	+150	°C
T <sub>j</sub>	operating junction temperature		–55	+150	°C

## Notes

1. T<sub>s</sub> is the temperature at the soldering point of the drain leads.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. (So both devices may be loaded up to 1.6 W at the same time).
4. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an R<sub>th a-tp</sub> (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an R<sub>th a-tp</sub> (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on a printed-circuit board with an R<sub>th a-tp</sub> (ambient to tie-point) of 90 K/W.

Complementary enhancement mode  
MOS transistors

PHC2300

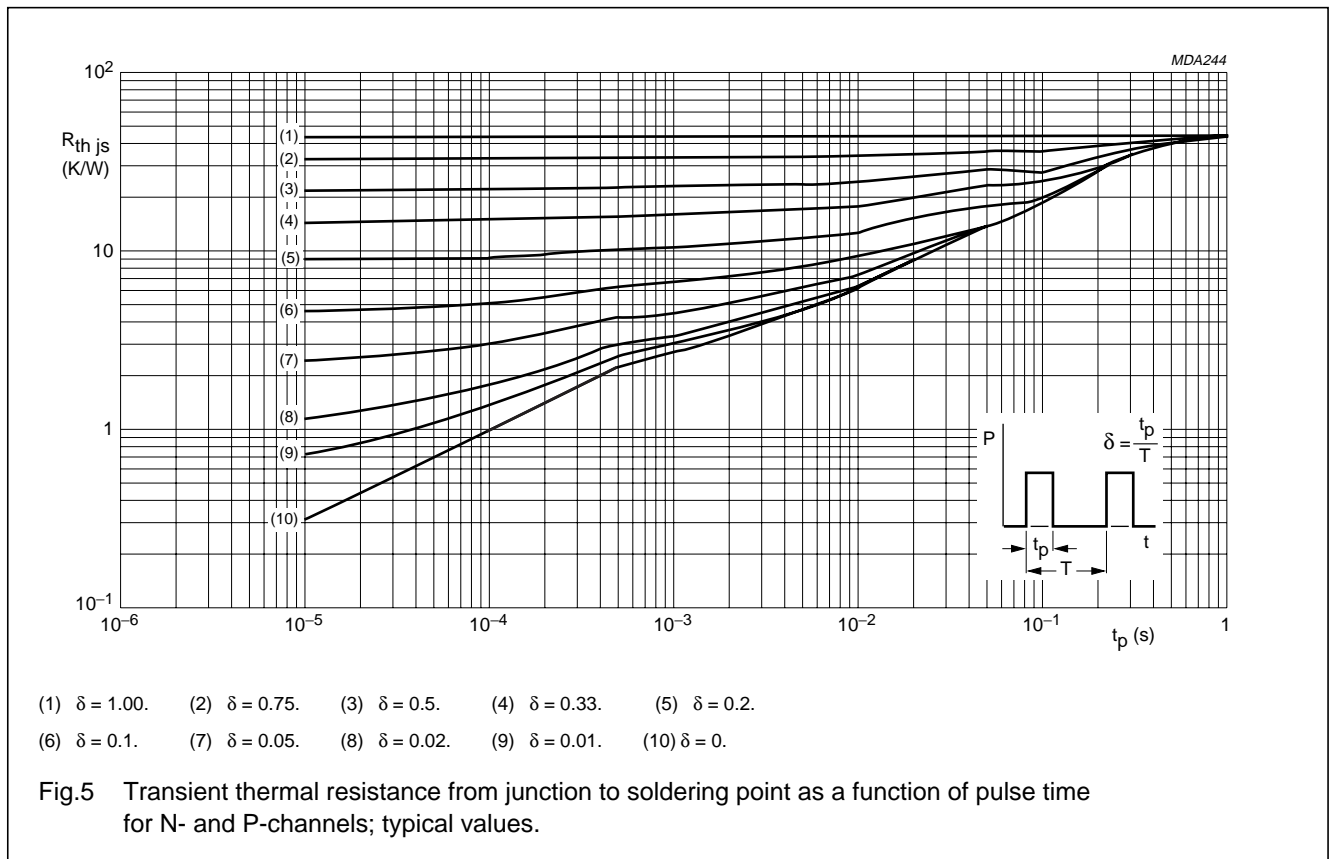


# Complementary enhancement mode MOS transistors

PHC2300

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	43	K/W



## CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per FET</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	$V_{GS} = 0; I_D = 10\ \mu\text{A}$	300	–	–	V
	P-channel	$V_{GS} = 0; I_D = -10\ \mu\text{A}$	-300	–	–	V
$V_{GSth}$	gate-source threshold voltage					
	N-channel	$V_{GS} = V_{DS}; I_D = 1\ \text{mA}$	0.8	–	2	V
	P-channel	$V_{GS} = V_{DS}; I_D = -1\ \text{mA}$	-0.8	–	-2	V
$I_{DSS}$	drain-source leakage current					
	N-channel	$V_{GS} = 0; V_{DS} = 240\ \text{V}$	–	–	100	nA
	P-channel	$V_{GS} = 0; V_{DS} = -240\ \text{V}$	–	–	-100	nA

## Complementary enhancement mode MOS transistors

PHC2300

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0$				
	N-channel		–	–	$\pm 100$	nA
	P-channel		–	–	$\pm 100$	nA
$R_{DSon}$	drain-source on-state resistance					
	N-channel	$V_{GS} = 10\text{ V}; I_D = 170\text{ mA}$	–	–	8	$\Omega$
	P-channel	$V_{GS} = -10\text{ V}; I_D = -115\text{ mA}$	–	–	17	$\Omega$
$C_{iss}$	input capacitance					
	N-channel	$V_{GS} = 0; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	–	57	–	pF
	P-channel	$V_{GS} = 0; V_{DS} = -50\text{ V}; f = 1\text{ MHz}$	–	45	–	pF
$C_{oss}$	output capacitance					
	N-channel	$V_{GS} = 0; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	–	15	–	pF
	P-channel	$V_{GS} = 0; V_{DS} = -50\text{ V}; f = 1\text{ MHz}$	–	15	–	pF
$C_{rss}$	reverse transfer capacitance					
	N-channel	$V_{GS} = 0; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	–	2.6	–	pF
	P-channel	$V_{GS} = 0; V_{DS} = -50\text{ V}; f = 1\text{ MHz}$	–	3	–	pF
$Q_G$	total gate charge					
	N-channel	$V_{GS} = 10\text{ V}; V_{DS} = 50\text{ V}; I_D = 170\text{ mA}$	–	2097	–	pC
	P-channel	$V_{GS} = -10\text{ V}; V_{DS} = -50\text{ V}; I_D = -115\text{ mA}$	–	2137	–	pC
$Q_{GS}$	gate-source charge					
	N-channel	$V_{GS} = 10\text{ V}; V_{DS} = 50\text{ V}; I_D = 170\text{ mA}$	–	75	–	pC
	P-channel	$V_{GS} = -10\text{ V}; V_{DS} = -50\text{ V}; I_D = -115\text{ mA}$	–	68	–	pC
$Q_{GD}$	gate-drain charge					
	N-channel	$V_{GS} = 10\text{ V}; V_{DS} = 50\text{ V}; I_D = 170\text{ mA}$	–	527	–	pC
	P-channel	$V_{GS} = -10\text{ V}; V_{DS} = -50\text{ V}; I_D = -115\text{ mA}$	–	674	–	pC
<b>Switching times</b>						
$t_{on}$	turn-on time					
	N-channel	$V_{GS} = 0\text{ to }10\text{ V}; V_{DD} = 50\text{ V}; I_D = 170\text{ mA}$	–	2.5	10	ns
	P-channel	$V_{GS} = 0\text{ to }-10\text{ V}; V_{DD} = -50\text{ V}; I_D = -115\text{ mA}$	–	4	10	ns
$t_{off}$	turn-off time					
	N-channel	$V_{GS} = 10\text{ to }0\text{ V}; V_{DD} = 50\text{ V}; I_D = 170\text{ mA}$	–	17	30	ns
	P-channel	$V_{GS} = -10\text{ to }0\text{ V}; V_{DD} = -50\text{ V}; I_D = -115\text{ mA}$	–	25	35	ns

# Complementary enhancement mode MOS transistors

PHC2300

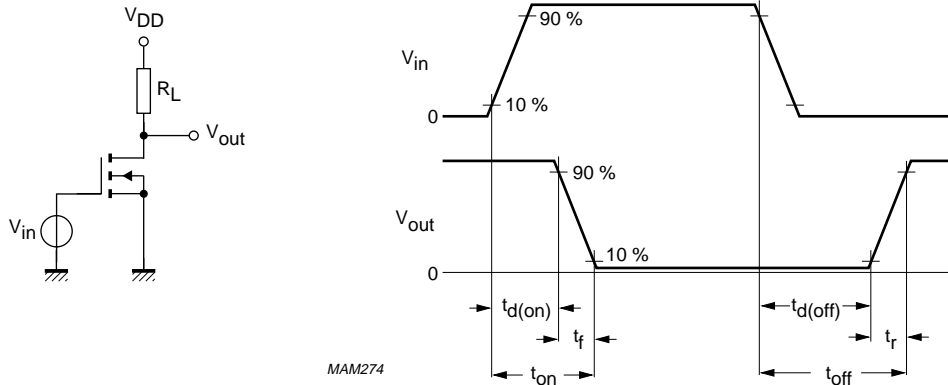


Fig.6 Switching times test circuit with input and output waveforms; N-channel.

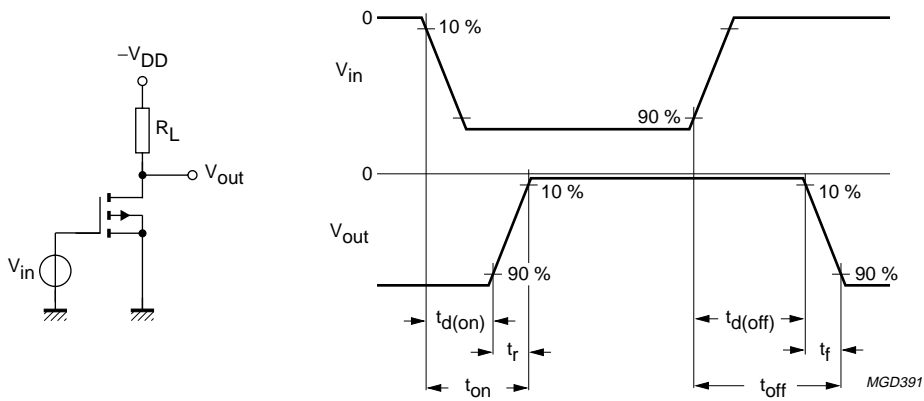
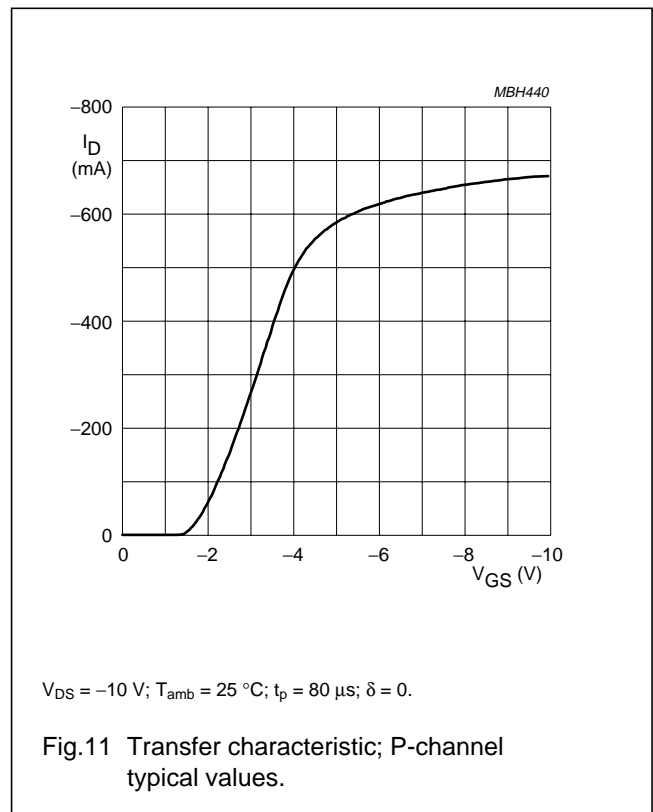
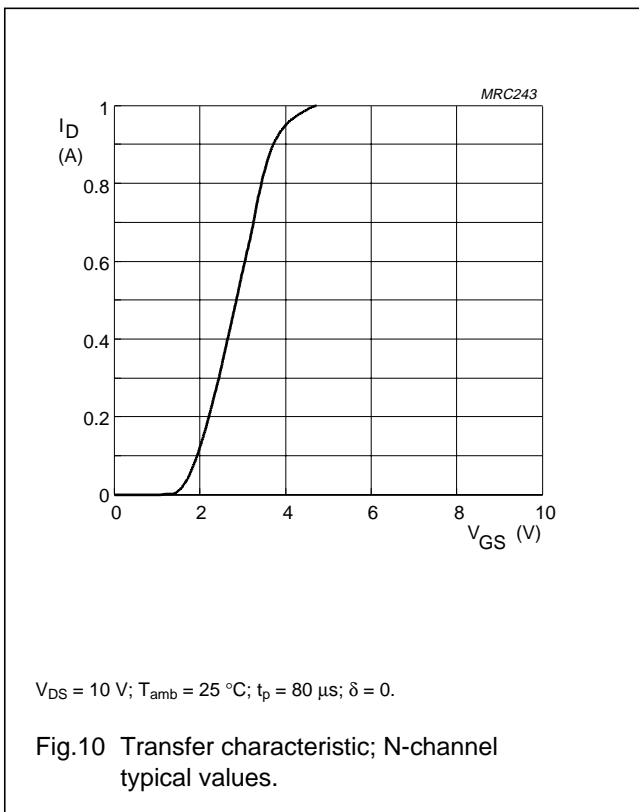
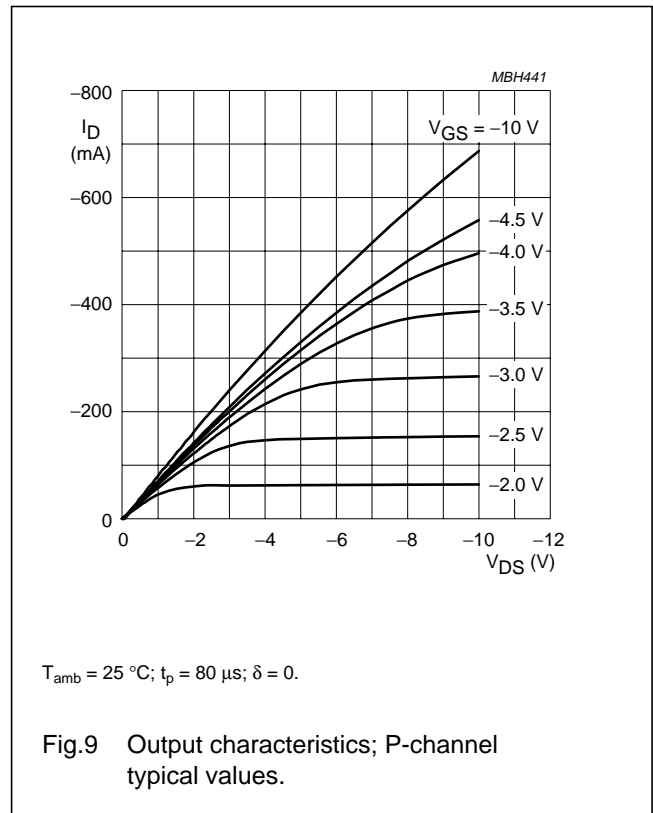
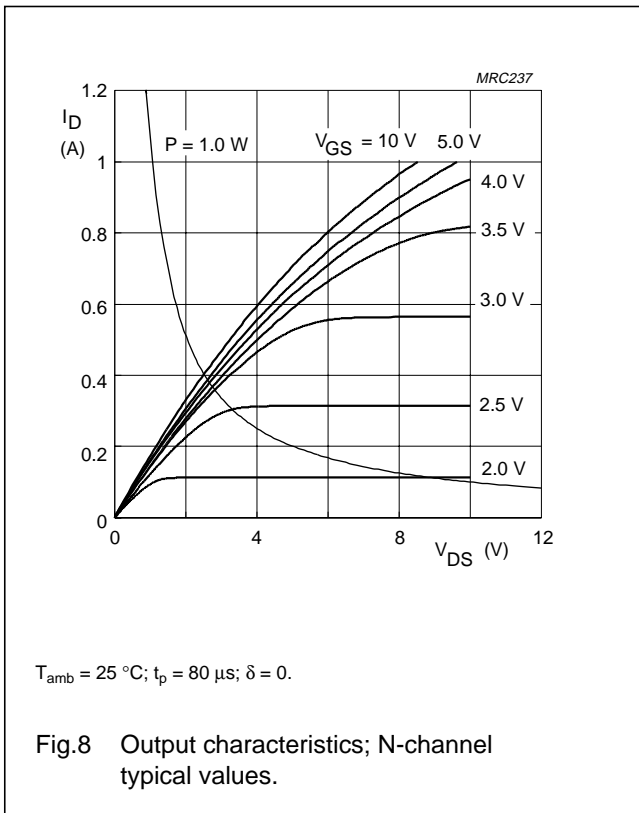


Fig.7 Switching times test circuit with input and output waveforms; P-channel.

Complementary enhancement mode  
MOS transistors

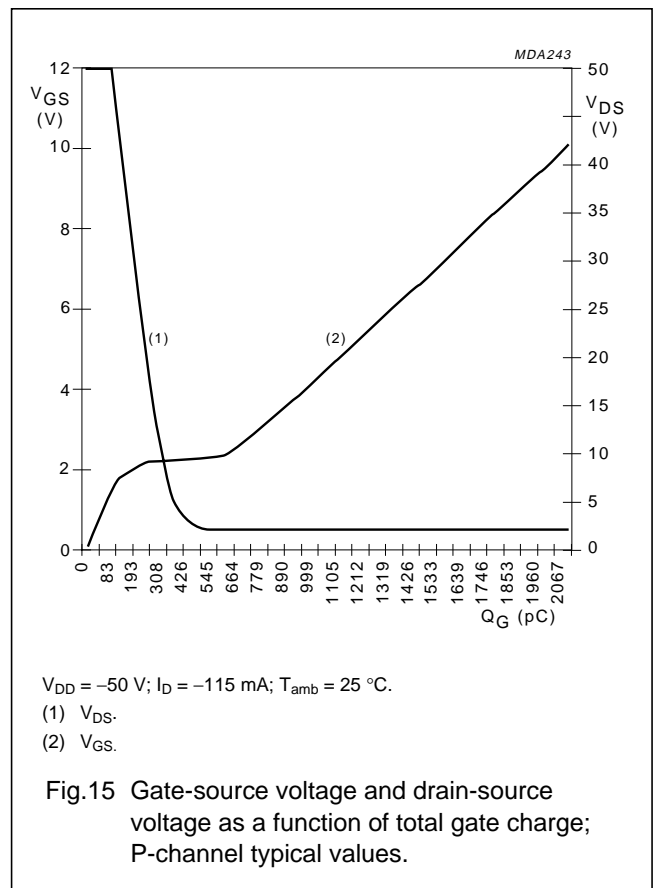
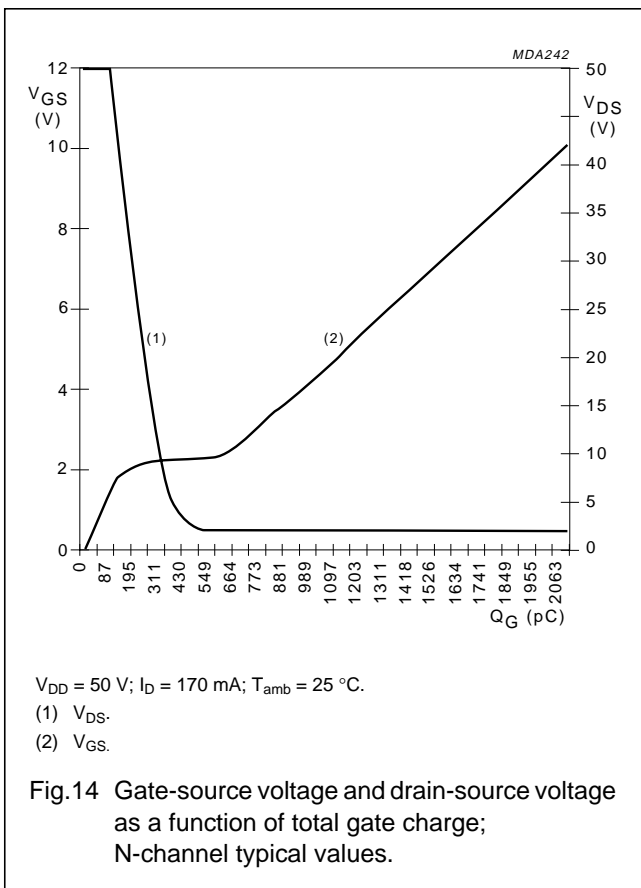
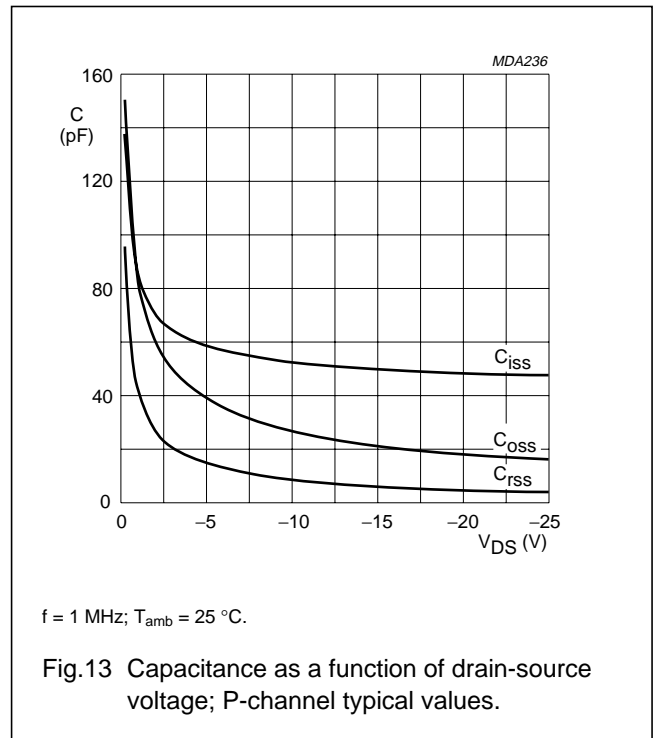
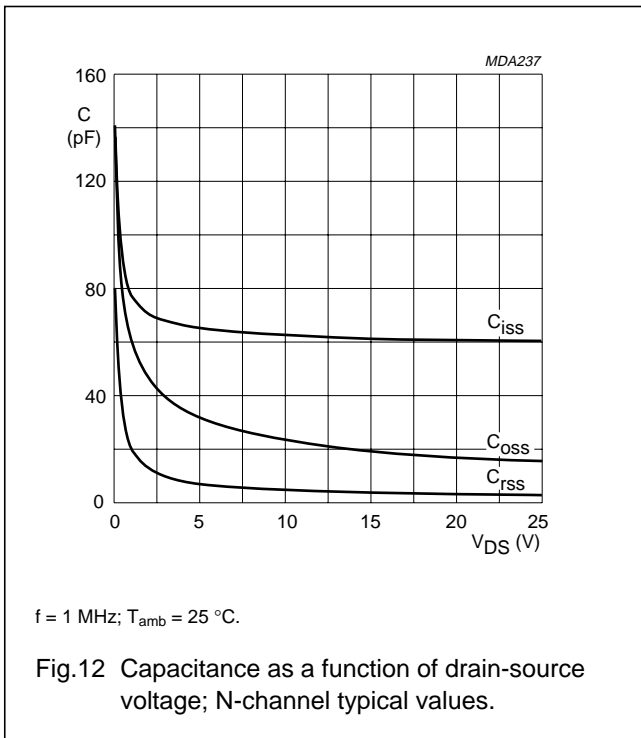
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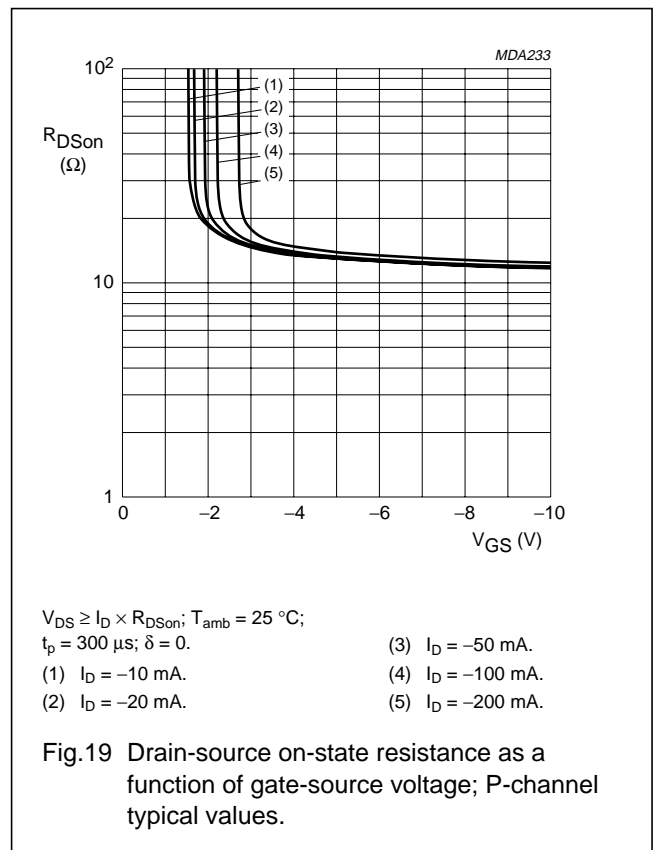
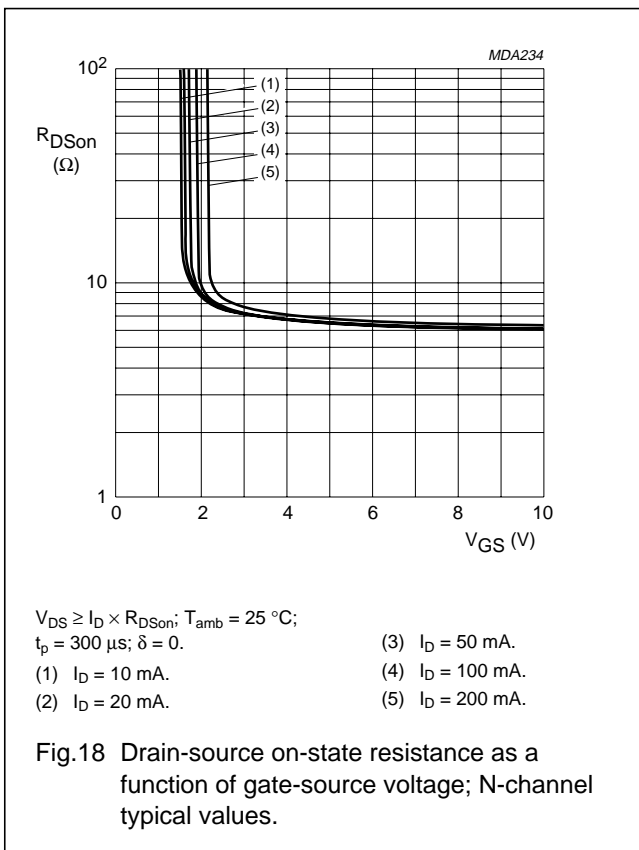
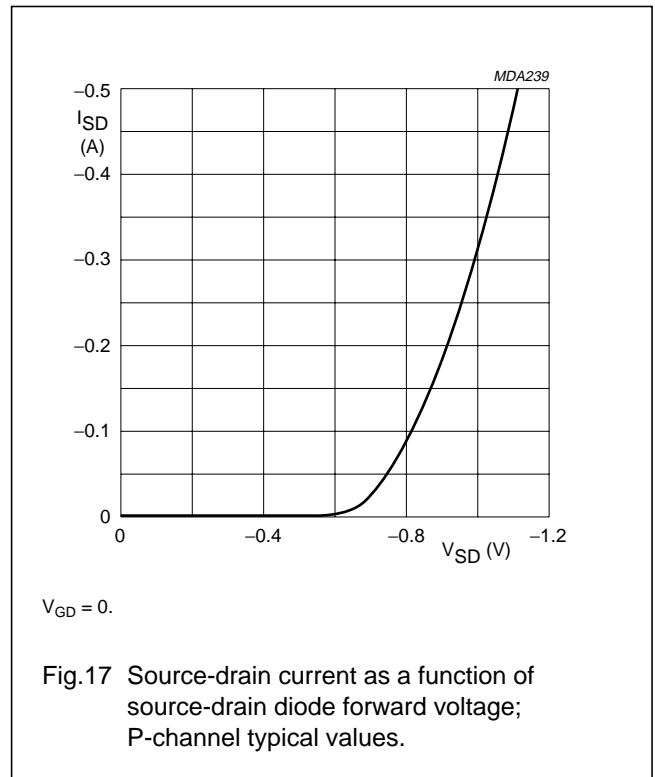
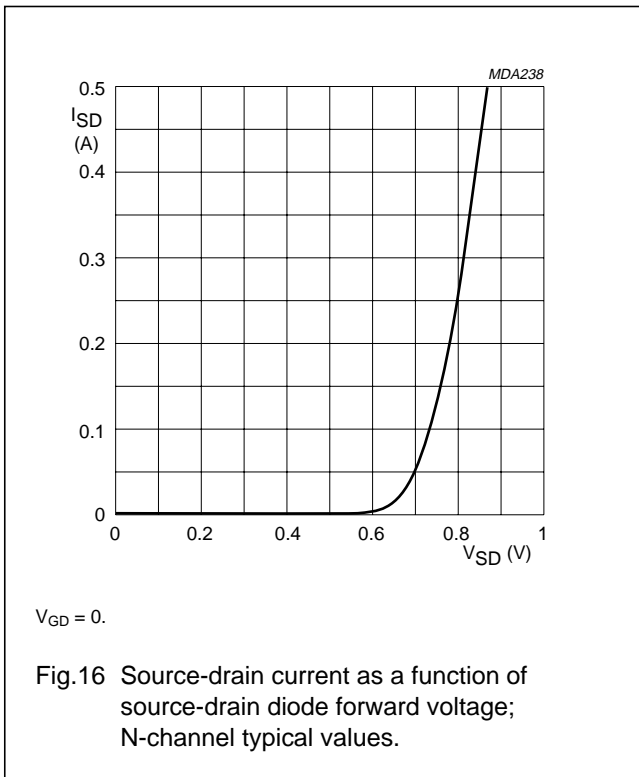
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## PHC2300



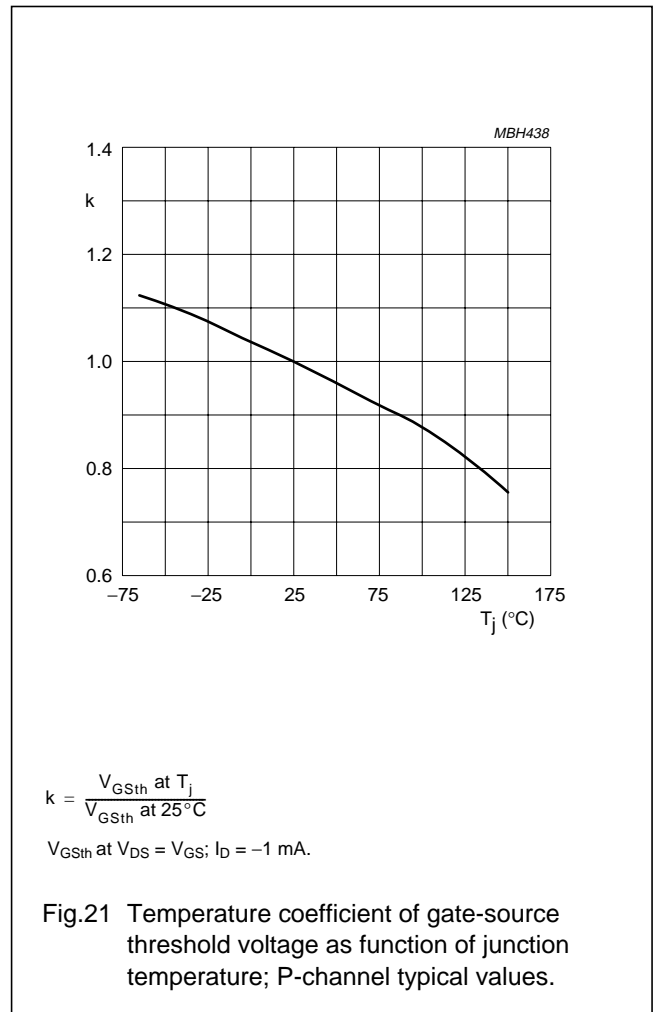
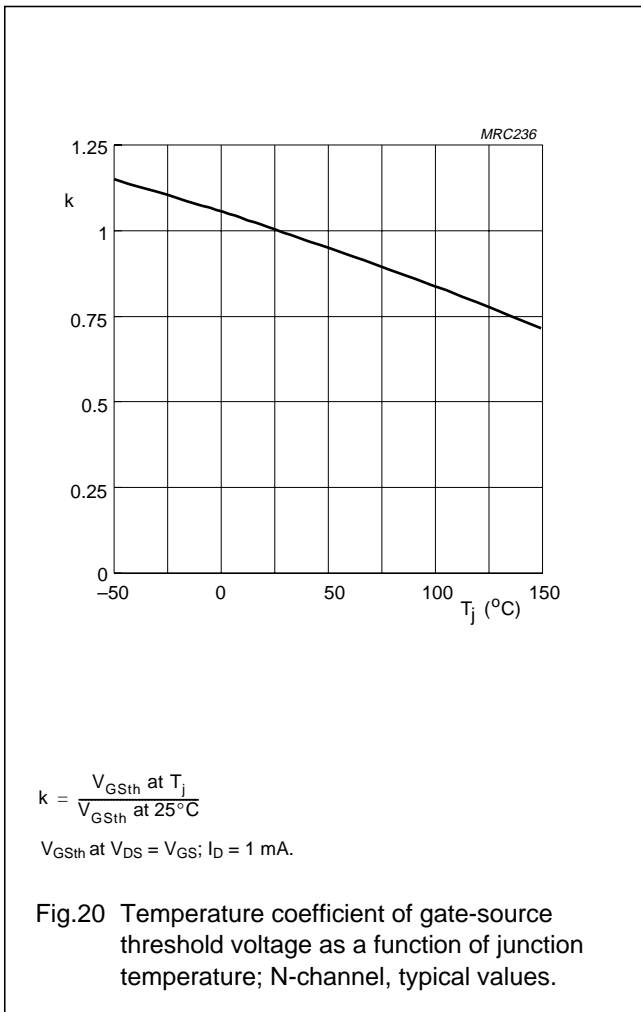
Complementary enhancement mode  
MOS transistors

PHC2300



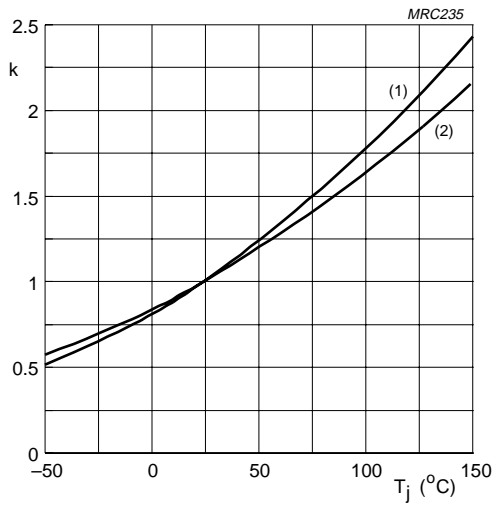
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MOS transistors

PHC2300



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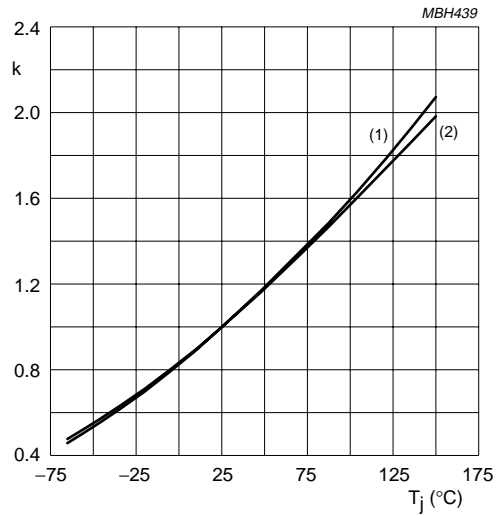
PHC2300



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

- (1)  $R_{DSon}$  at  $V_{GS} = 10\text{ V}$ ;  $I_D = 250\text{ mA}$ .
- (2)  $R_{DSon}$  at  $V_{GS} = 2.4\text{ V}$ ;  $I_D = 20\text{ mA}$ .

Fig.22 Temperature coefficient of drain-source on-resistance as a function of junction temperature; N-channel typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

- (1)  $R_{DSon}$  at  $V_{GS} = -4.5\text{ V}$ ;  $I_D = -80\text{ mA}$ .
- (2)  $R_{DSon}$  at  $V_{GS} = -2.8\text{ V}$ ;  $I_D = -50\text{ mA}$ .

Fig.23 Temperature coefficient of drain-source on-resistance as a function of junction temperature; P-channel typical values.

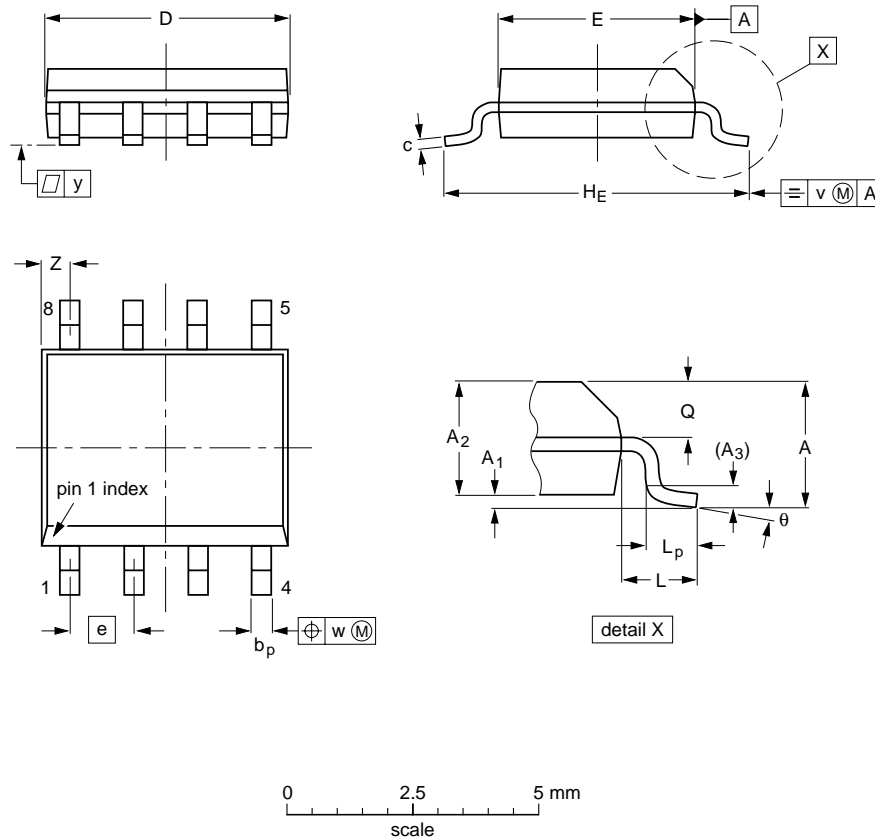
# Complementary enhancement mode MOS transistors

PHC2300

## PACKAGE OUTLINE

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				95-02-04 97-05-22

# Complementary enhancement mode MOS transistors

PHC2300

## DEFINITIONS

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,  
Fax. +43 160 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 689 211, Fax. +359 2 689 102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 0044

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580920

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** see Singapore

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,  
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 1231,  
Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 3 301 6312, Fax. +34 3 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 632 2000, Fax. +46 8 632 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2686, Fax. +41 1 481 7730

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 625 344, Fax. +381 11 635 777

**For all other countries apply to:** Philips Semiconductors, Marketing & Sales Communications,  
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

**Internet:** <http://www.semiconductors.philips.com>

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西安分公司：西安高新开发区 20 所(中国电子科技集团导航技术研究所)

西安劳动南路 88 号电子商城二楼 D23 号

TEL: 029-81022619 13072977981 FAX:029-88789382