

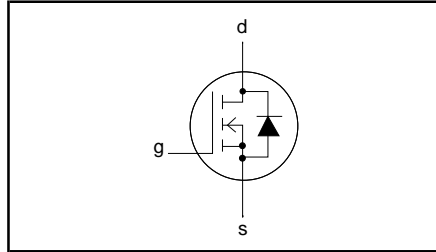
TrenchMOS™ transistor Logic level FET

PHD24N03LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 30\text{ V}$
$I_D = 24\text{ A}$
$R_{DS(ON)} \leq 56\text{ m}\Omega (V_{GS} = 5\text{ V})$
$R_{DS(ON)} \leq 50\text{ m}\Omega (V_{GS} = 10\text{ V})$

GENERAL DESCRIPTION

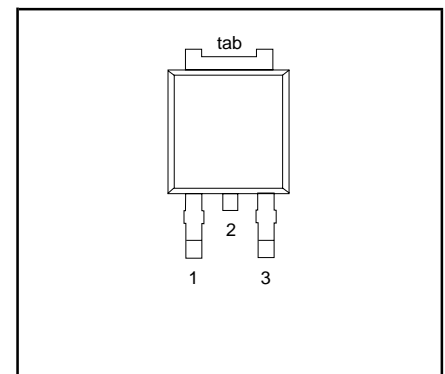
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHD24N03LT is supplied in the SOT428 (DPAK) surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

SOT428 (DPAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$	-	30	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	24	A
		$T_{mb} = 100\text{ }^\circ\text{C}$	-	20	A
I_{DM}	Pulsed drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	96	A
P_D	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	60	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\text{-}j\text{-}mb}$	Thermal resistance junction to mounting base		-	2.5	K/W
$R_{th\text{-}j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

¹ it is not possible to make connection to pin 2 of the SOT428 package.

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ELECTRICAL CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.25 mA; T _j = -55°C	30 27	- -	- -	V V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA T _j = 175°C T _j = -55°C	1.0 0.5 -	1.5 - -	2.0 - 2.3	V V V
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 10 V; I _D = 12 A V _{GS} = 5 V; I _D = 12 A T _j = 175°C	- - -	50 45 -	56 50 104	mΩ mΩ mΩ
I _{GSS}	Gate source leakage current	V _{GS} = ±5 V; V _{DS} = 0 V	-	10	100	nA
I _{DSS}	Zero gate voltage drain current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 175°C	-	0.05	10	μA
Q _{g(tot)}	Total gate charge	I _D = 24 A; V _{DD} = 15 V; V _{GS} = 5 V	-	7	-	nC
Q _{gs}	Gate-source charge		-	2.3	-	nC
Q _{gd}	Gate-drain (Miller) charge		-	5	-	nC
t _{d on}	Turn-on delay time	V _{DD} = 15 V; R _D = 0.6 Ω;	-	12	-	ns
t _r	Turn-on rise time	V _{GS} = 5 V; R _G = 10 Ω	-	50	-	ns
t _{d off}	Turn-off delay time	Resistive load	-	30	-	ns
t _f	Turn-off fall time		-	36	-	ns
L _d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L _s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C _{iss}	Input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz	-	460	-	pF
C _{oss}	Output capacitance		-	144	-	pF
C _{rss}	Feedback capacitance		-	78	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

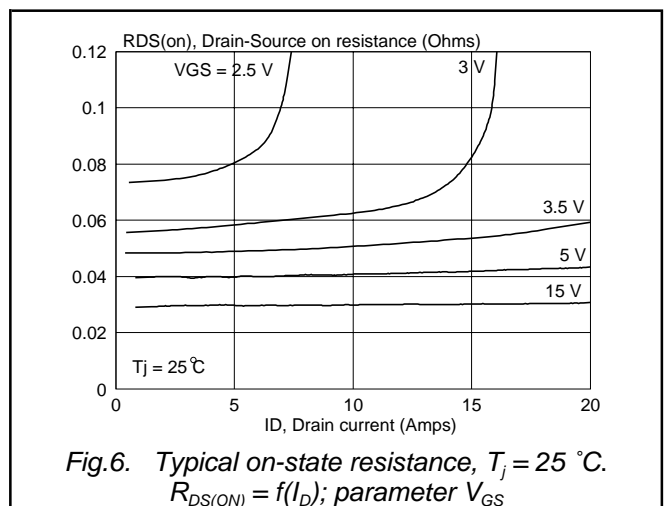
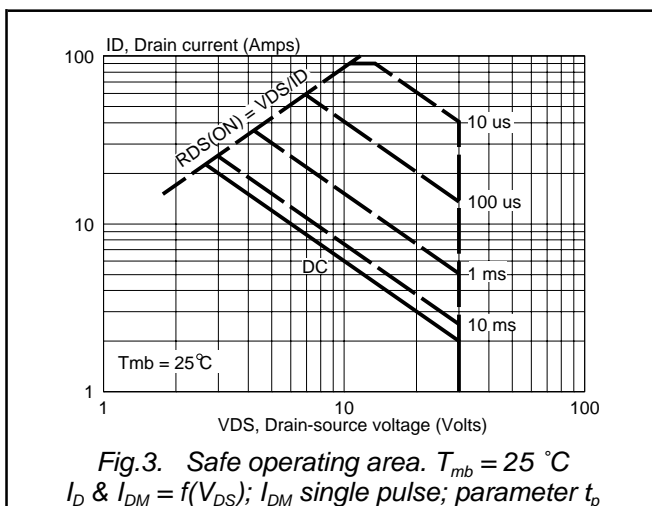
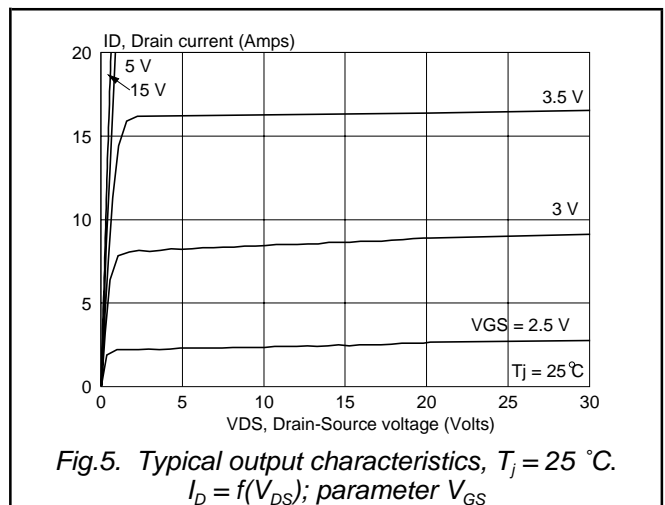
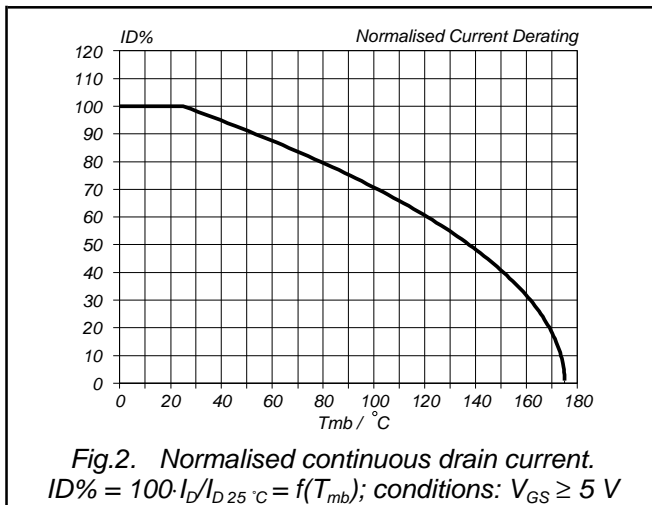
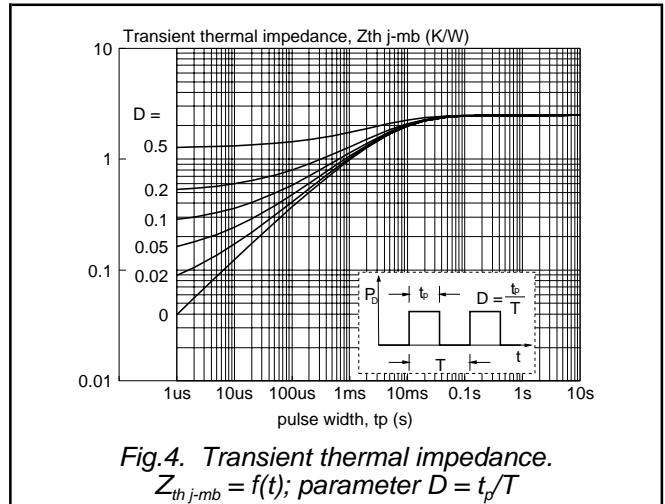
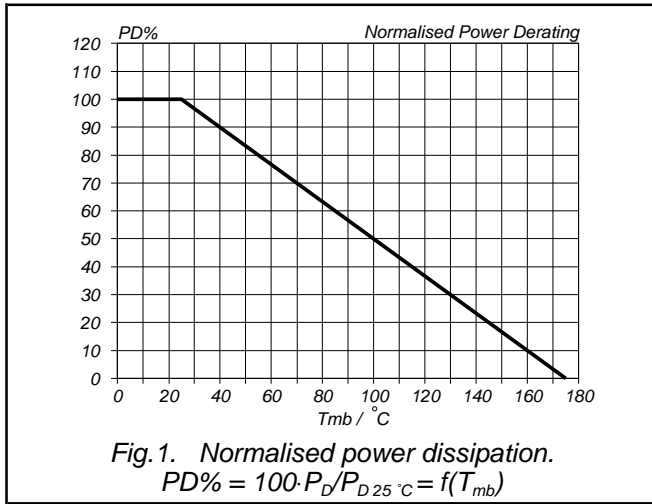
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _S	Continuous source current (body diode)		-	-	24	A
I _{SM}	Pulsed source current (body diode)		-	-	96	A
V _{SD}	Diode forward voltage	I _F = 24 A; V _{GS} = 0 V	-	1.05	1.5	V
t _{rr}	Reverse recovery time	I _F = 12 A; -di _F /dt = 100 A/μs;	-	50	-	ns
Q _{rr}	Reverse recovery charge	V _{GS} = 0 V; V _R = 30 V	-	100	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W _{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I _D = 12 A; V _{DD} ≤ 15 V; V _{GS} = 5 V; R _{GS} = 50 Ω; T _{mb} = 25 °C	-	15	mJ

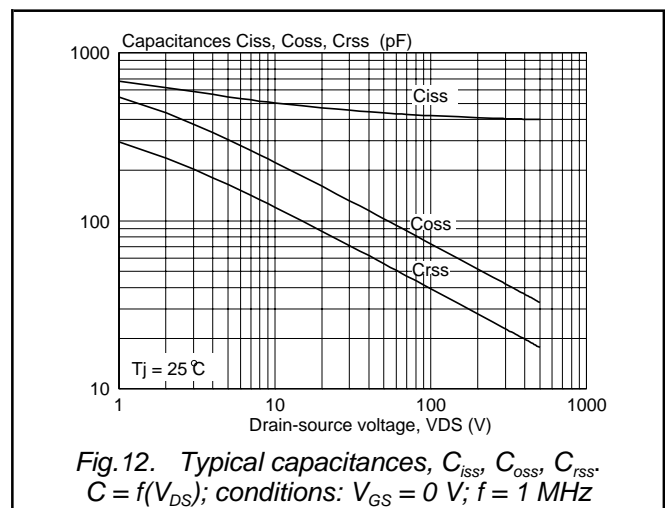
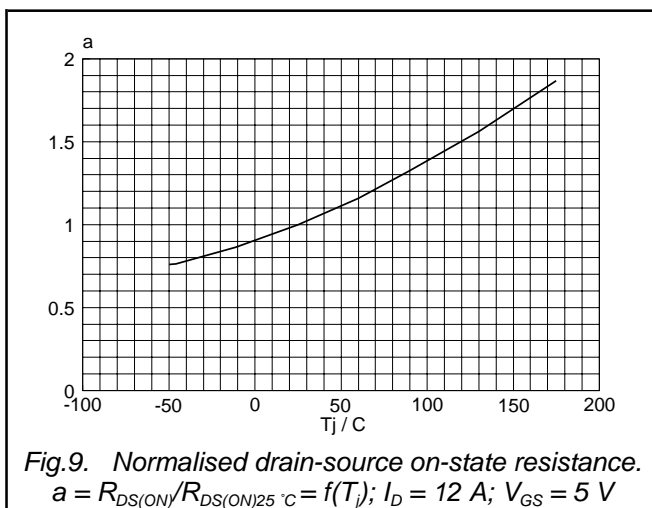
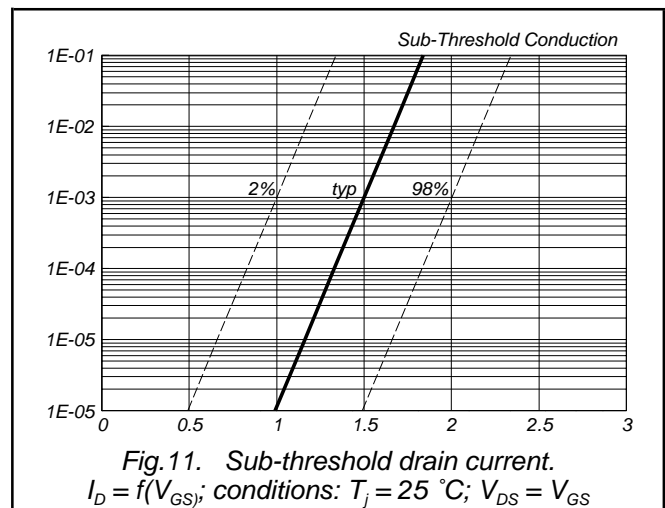
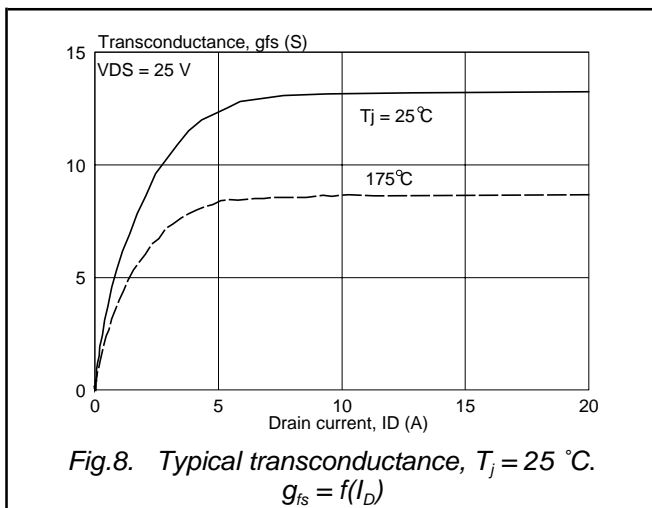
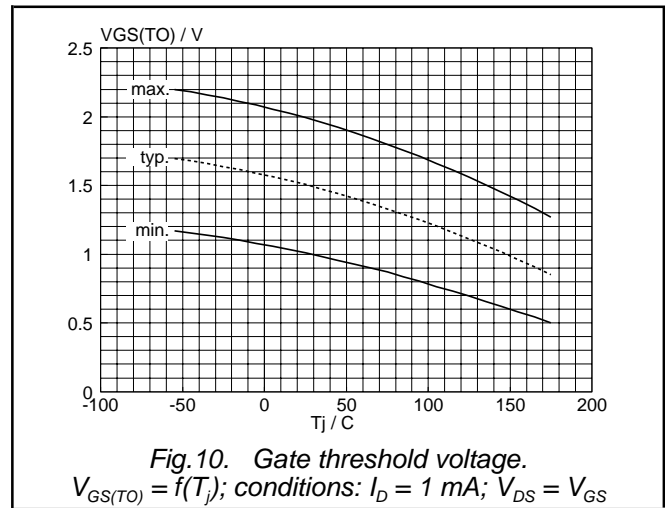
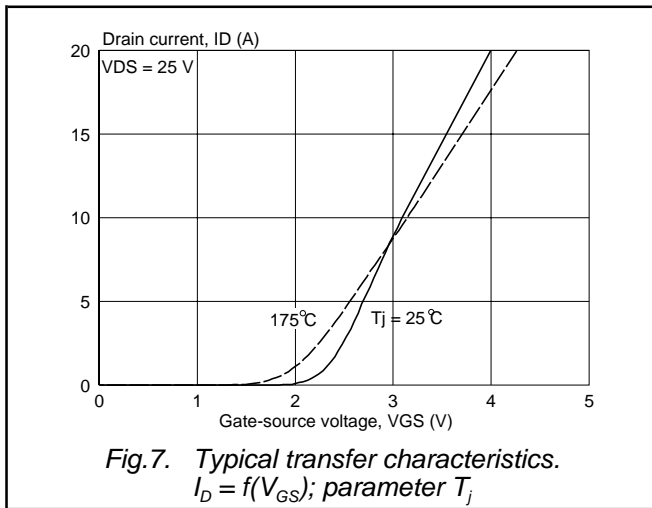
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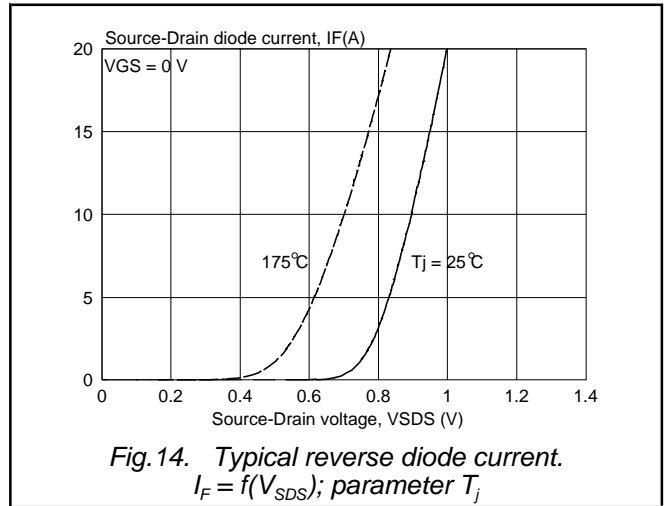
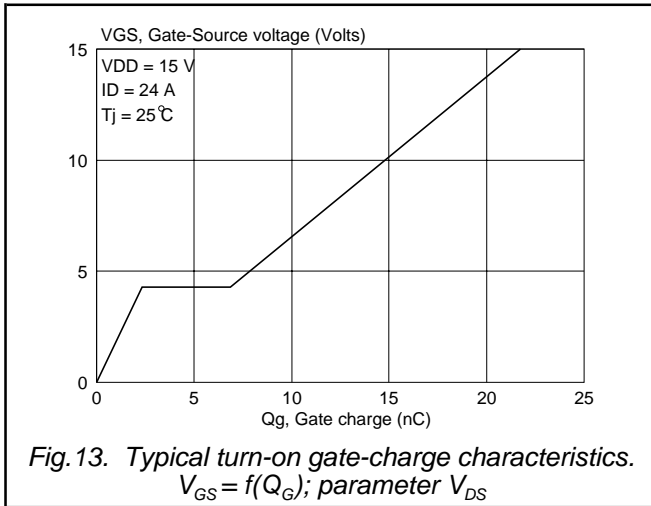
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MECHANICAL DATA

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428

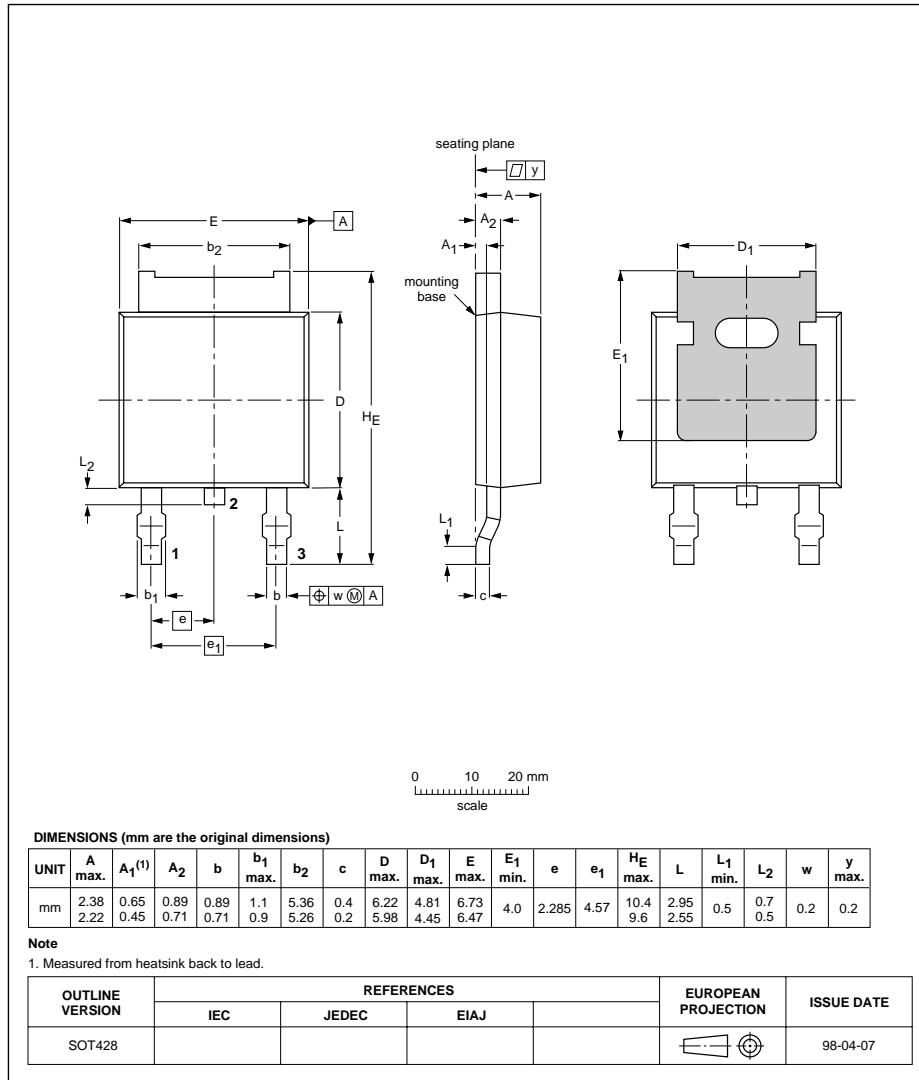


Fig. 15. SOT428 surface mounting package. Centre pin connected to mounting base.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

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MOUNTING INSTRUCTIONS

Dimensions in mm

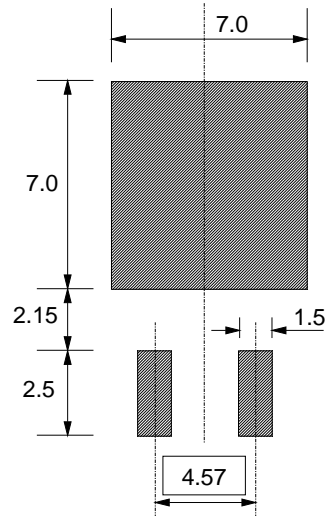


Fig.16. SOT428 : soldering pattern for surface mounting.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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