

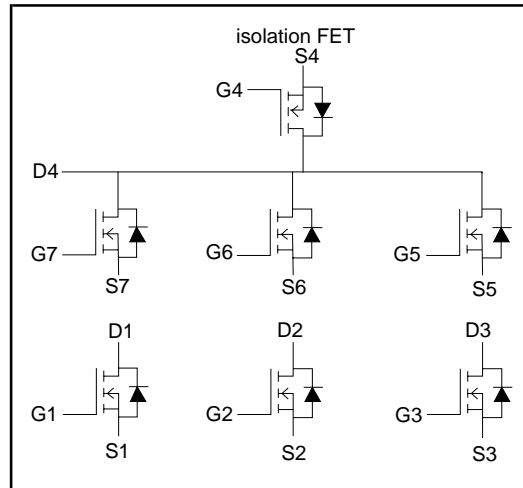
**N-channel enhancement mode
TrenchMOS transistor array**

PHN70308

FEATURES

- 30 mΩ isolation transistor
- 80 mΩ spindle transistors
- TrenchMOS technology
- Logic level compatible
- Surface mount package

SYMBOL



QUICK REFERENCE DATA

$V_{DS} = 25\text{ V}$
$I_D = 5\text{ A}$
$R_{DS(ON)} \leq 30\text{ m}\Omega$ ($V_{GS} = 10\text{ V}$; isolation FET)
$R_{DS(ON)} \leq 80\text{ m}\Omega$ ($V_{GS} = 10\text{ V}$; spindle FETs)

GENERAL DESCRIPTION

This product is used to drive high performance, three phase brushless d.c. motors in computer disk drives.

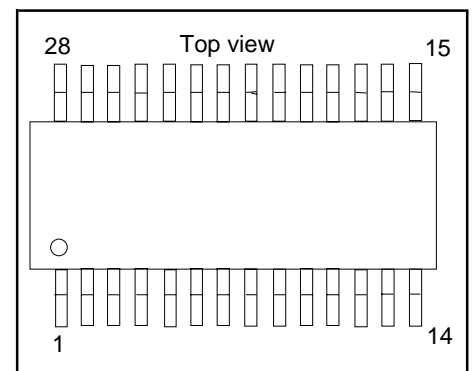
The PHN70308 contains seven, n-channel enhancement mode trenchMOS transistors in a surface mounting plastic package. Six of the transistors can be configured as a three phase bridge to drive the spindle of a disk drive motor. The remaining transistor delivers power to the three phase bridge during normal operation. In the event of a power failure occurring whilst the motor is still spinning, this transistor isolates the computer power supply from the back emf generated by the motor.

The PHN70308 is supplied in the surface mounting SOT341-1 (SSOP28) package.

PINNING

PIN	DESCRIPTION	PIN	DESCRIPTION
1,3	drain 1	16,17	source 4
2	source 1	18	gate 4
4	gate 1	20	gate 5
5,7	drain 2	21	source 5
6	source 2	23	gate 6
8	gate 2	24	source 6
9,11	drain 3	26	gate 7
10	source 3	27	source 7
12	gate 3	13-15,19,22,25,28	drain 4

SOT341-1 (SSOP28)



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LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	-	25	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Peak drain current per device (continuous operation)	$T_{sp} = 50\text{ }^\circ\text{C}^1$ spindle FETs; $\delta = 33.3\%$ isolation FET (dc)	-	5	A
I_{DM}	Peak current per device (pulse peak value)	spindle FETs isolation FET	-	20	A
P_{tot}	Power dissipation per device ²	$T_{sp} = 50\text{ }^\circ\text{C}$ spindle FETs; $\delta = 33.3\%$ isolation FET (dc)	-	1.13	W
P_{tot}	Total power dissipation in normal operation ²	$T_{sp} = 50\text{ }^\circ\text{C}$ spindle FETs; $\delta = 33.3\%$ isolation FET (dc)	-	8	W
T_{stg}, T_j	Storage & operating temperature		- 55	150	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point	isolation FET spindle FET	20 43	- -	K/W K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	device soldered to FR4 board, minimum footprint. isolation FET spindle FET	85 100	- -	K/W K/W

¹ T_{sp} is the temperature at the soldering point of the drain leads.

² In normal operation, the isolation FET conducts continuously whilst each of the spindle FETs conducts for 33.3% of the time. The dissipation in the isolation transistor is given by:-

$$P_{isolation} = I^2 \times R_{DS(ON)(isolation\ FET)}$$

The dissipation in each of the spindle transistors is given by:-

$$P_{spindle} = 0.333 \times I^2 \times R_{DS(ON)(spindle\ FET)}$$

The total dissipation under these conditions is given by:-

$$P_{tot} = P_{isolation} + 6 \times P_{spindle}$$

With the motor being driven at 5 A and assuming $T_j = 150\text{ }^\circ\text{C}$, the total dissipation is:-

$$P_{tot} = 25 \times 0.03 \times 1.7 + 0.333 \times 25 \times 0.08 \times 1.7 \times 6 = 8\text{ W}$$

Switching losses are assumed to be negligible.

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ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 10 μA	25	-	-	V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA	1.0	1.5	-	V
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 10 V; I _D = 4 A				
		spindle FET	-	60	80	mΩ
		isolation FET	-	27	30	mΩ
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 2 A				
		spindle FET	-	95	150	mΩ
		isolation FET	-	38	60	mΩ
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 10 V; I _D = 4 A; T _j = 150 °C				
		spindle FET	-	102	136	mΩ
		isolation FET	-	46	51	mΩ
I _{GSS}	Gate source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	-	10	100	nA
I _{DSS}	Zero gate voltage drain current	V _{DS} = 20 V; V _{GS} = 0 V; T _j = 150 °C	-	10	100	nA
			-	0.1	0.5	mA
Q _{g(tot)}	Total gate charge	I _D = 1 A; V _{DD} = 20 V; V _{GS} = 10 V				
		spindle FET	-	5.4	-	nC
		isolation FET	-	17.6	-	nC
Q _{gs}	Gate-source charge	spindle FET	-	0.4	-	nC
		isolation FET	-	1.4	-	nC
Q _{gd}	Gate-drain (Miller) charge	spindle FET	-	1.6	-	nC
		isolation FET	-	5.7	-	nC
t _{on}	Turn-on time	V _{DD} = 20 V; I _D = 1 A; V _{GS} = 10 V; R _G = 6 Ω; resistive load				
		spindle FET	-	5.5	10	ns
		isolation FET	-	11	20	ns
t _{off}	Turn-off time	spindle FET	-	16	25	ns
		isolation FET	-	45	60	ns
C _{iss}	Input capacitance	V _{GS} = 0 V; V _{DS} = 20 V; f = 1 MHz				
		spindle FET	-	180	-	pF
		isolation FET	-	546	-	pF
C _{oss}	Output capacitance	spindle FET	-	70	-	pF
		isolation FET	-	311	-	pF
C _{rss}	Feedback capacitance	spindle FET	-	36	-	pF
		isolation FET	-	133	-	pF

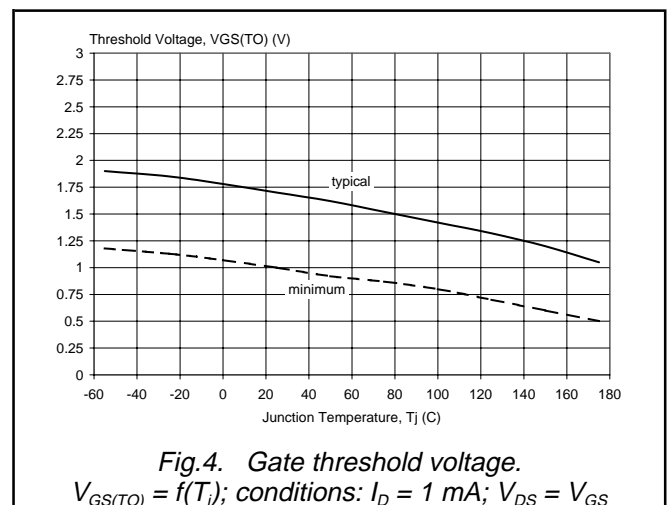
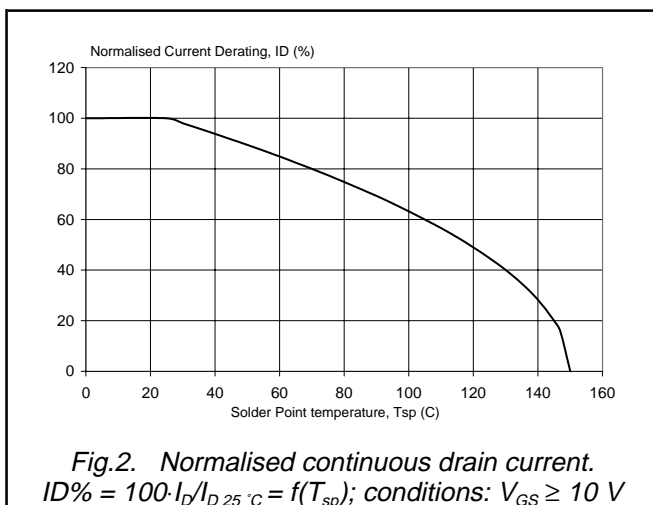
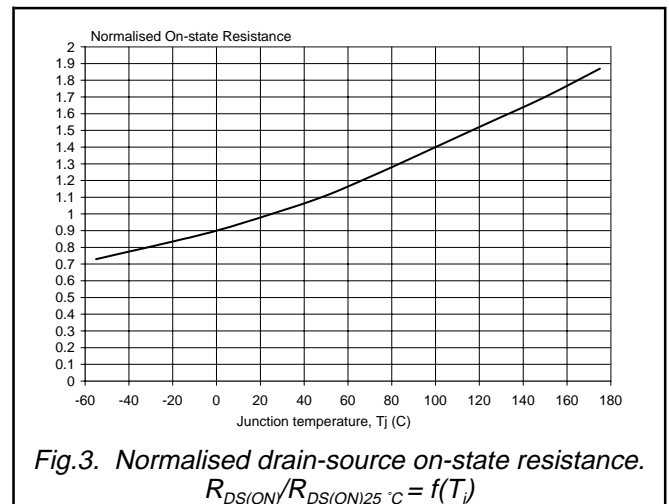
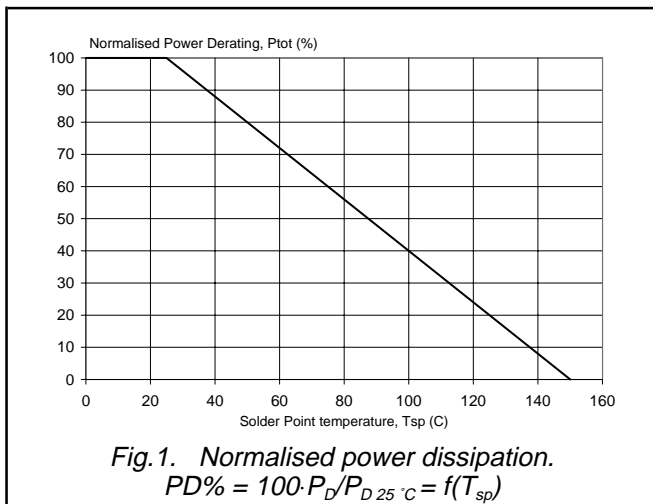
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SOURCE-DRAIN DIODE LIMITING VALUES AND CHARACTERISTICS

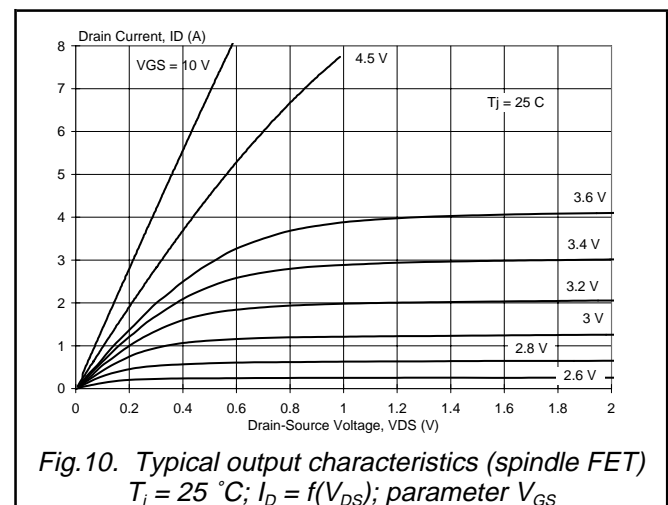
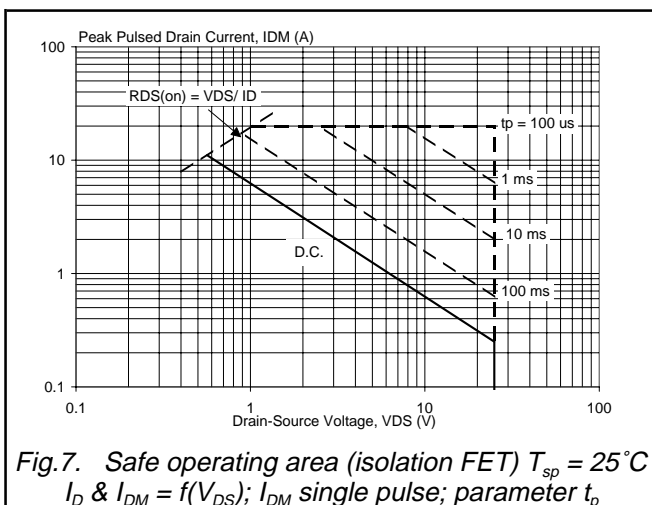
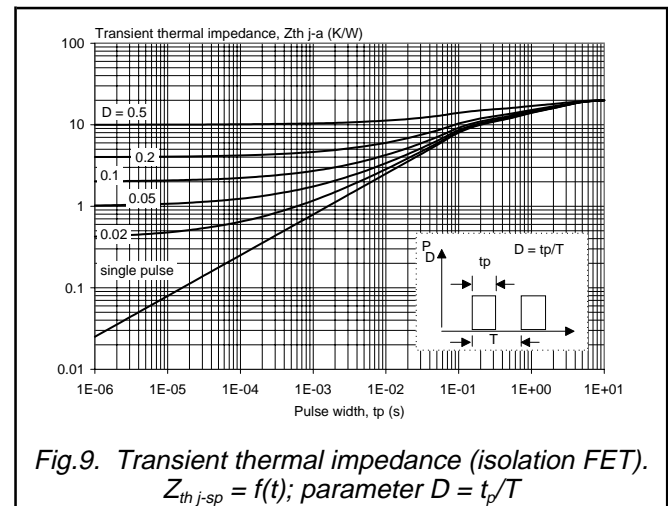
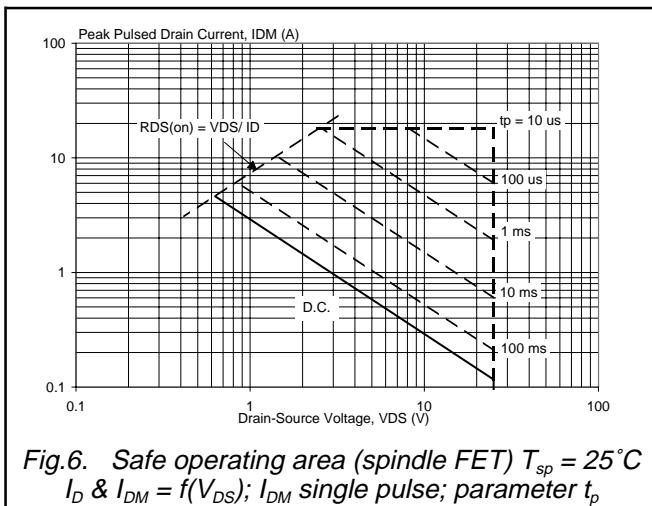
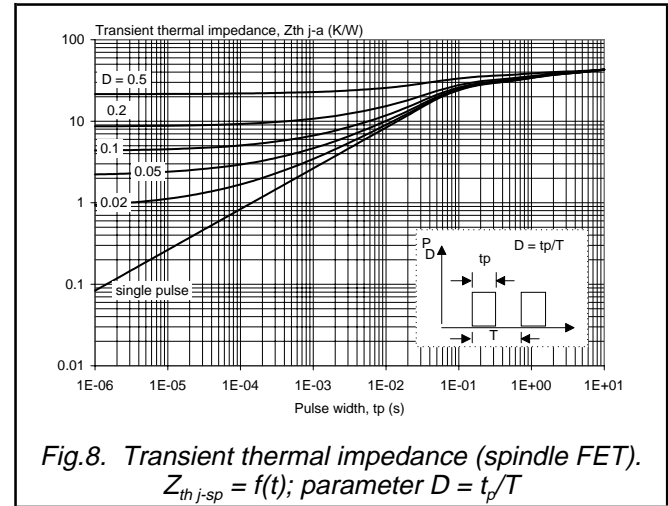
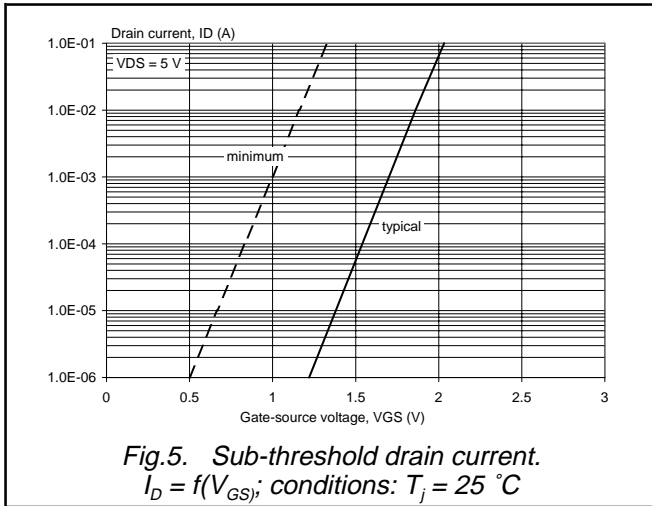
T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _F	Continuous forward diode current	T _{sp} = 50 °C spindle FET; δ = 33.3%	-	-	5	A
I _{FRM}	Repetitive peak forward diode current	isolation FET spindle FET	-	-	5 20	A A
V _F	Diode forward voltage	I _F = 1.25 A; V _{GS} = 0 V spindle FET	-	0.8	1	V
t _{rr}	Reverse recovery time	I _F = 1.25 A; -di _F /dt = 100 A/μs; V _{DS} = 25 V isolation FET	-	0.8	1	V
		spindle FET	-	20	-	ns
		isolation FET	-	25	-	ns



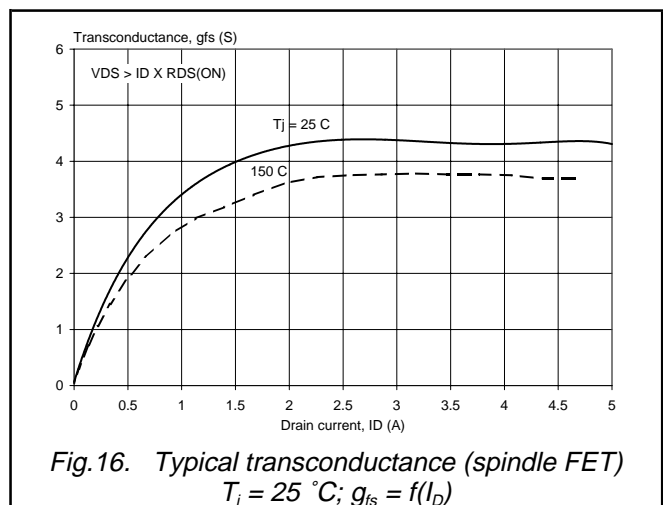
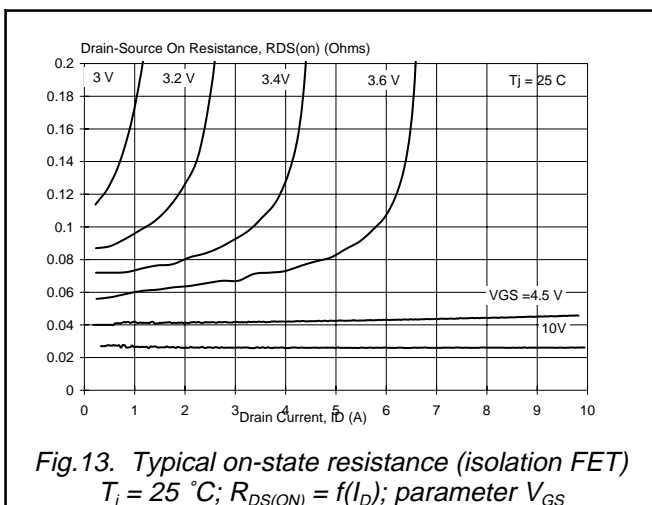
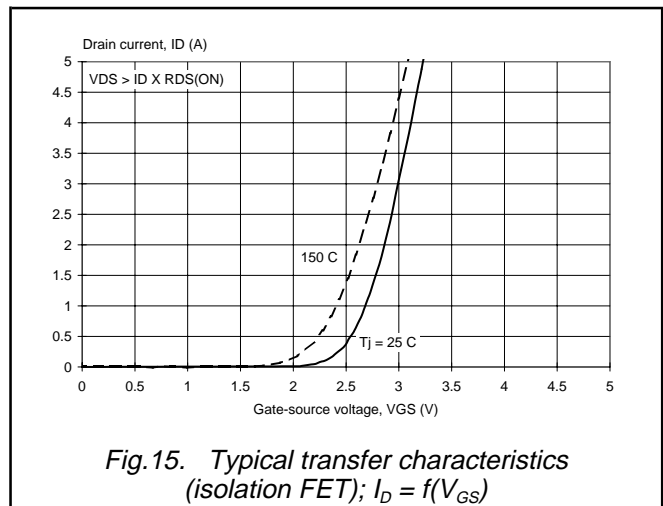
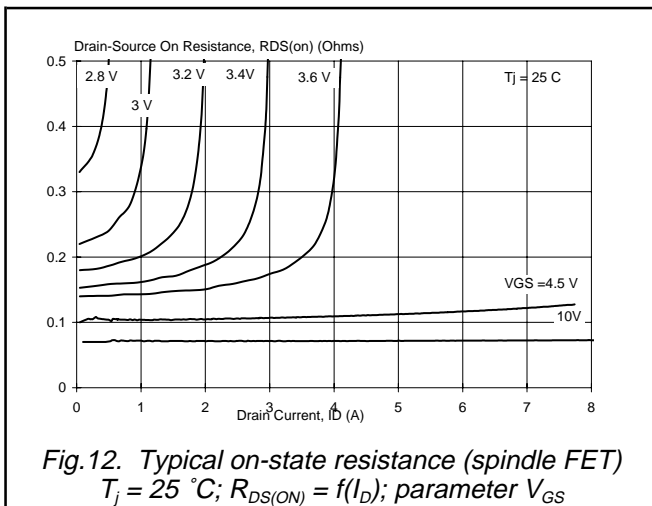
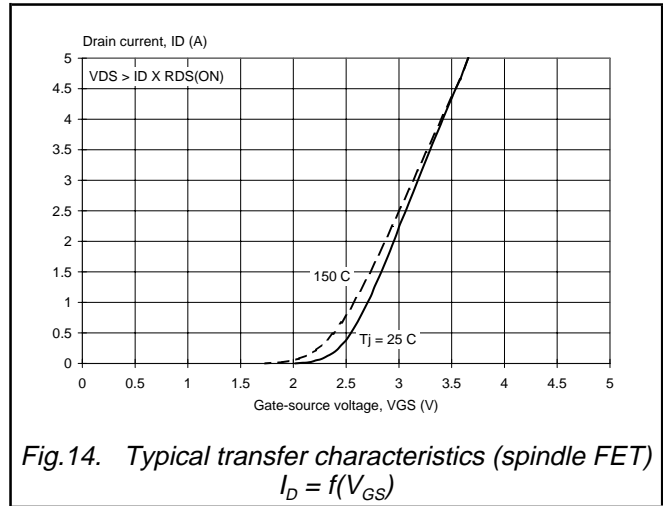
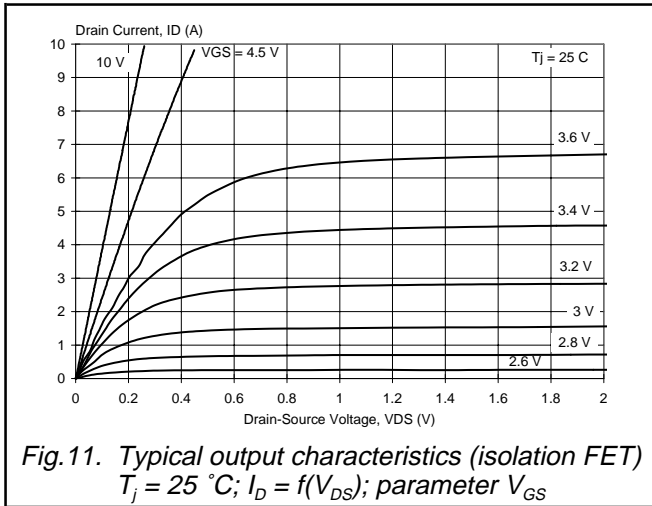
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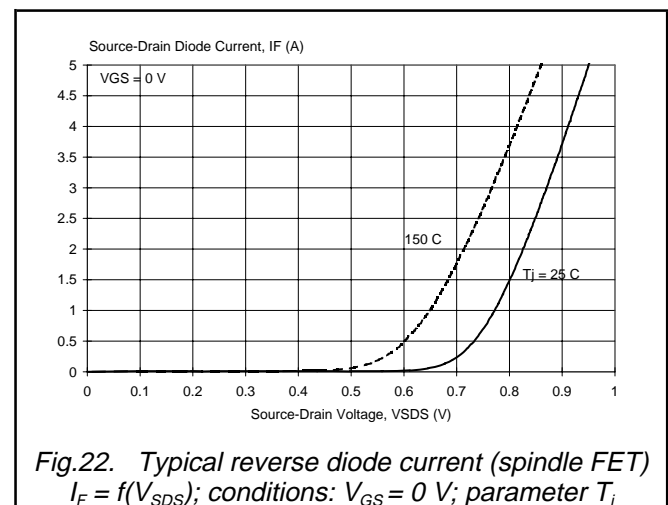
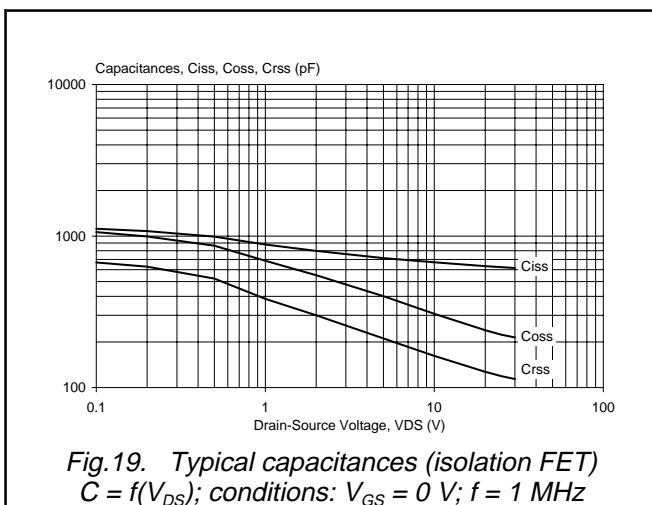
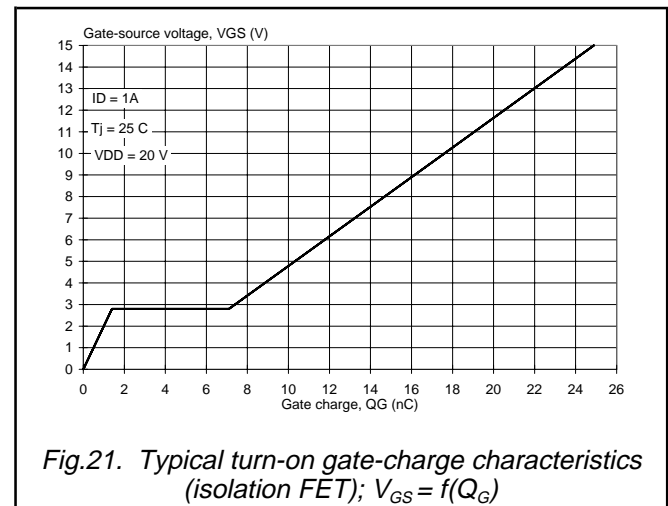
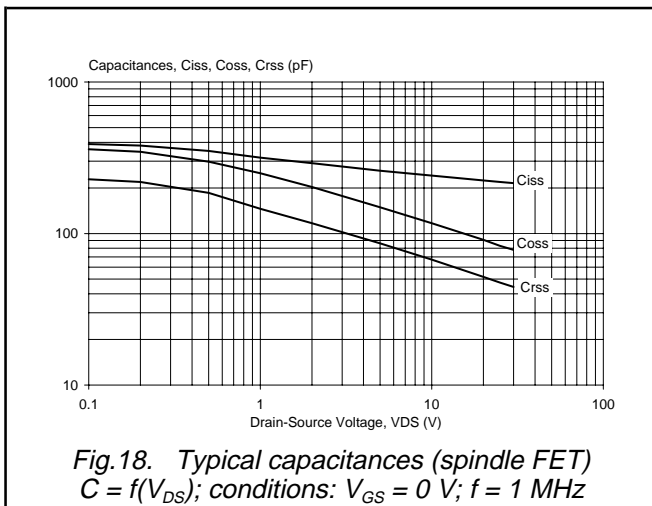
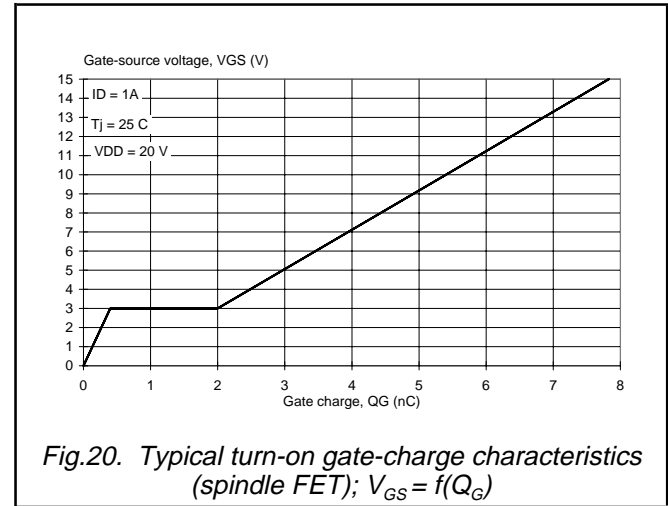
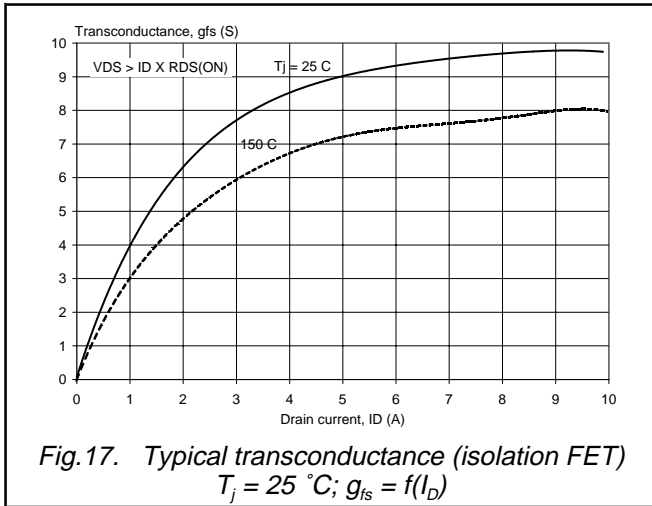
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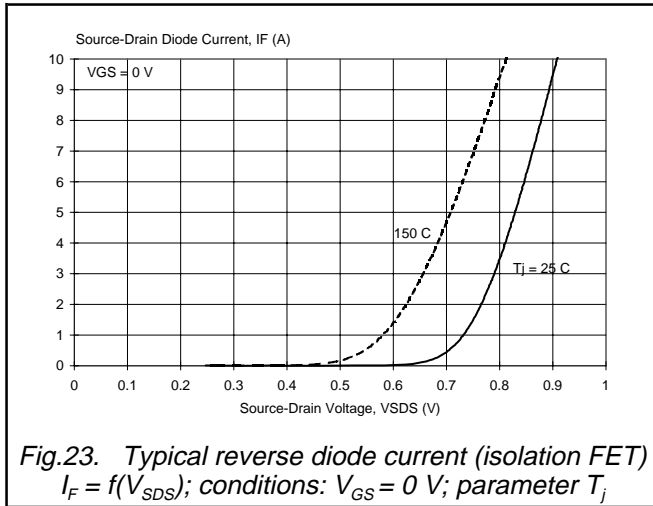
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MECHANICAL DATA

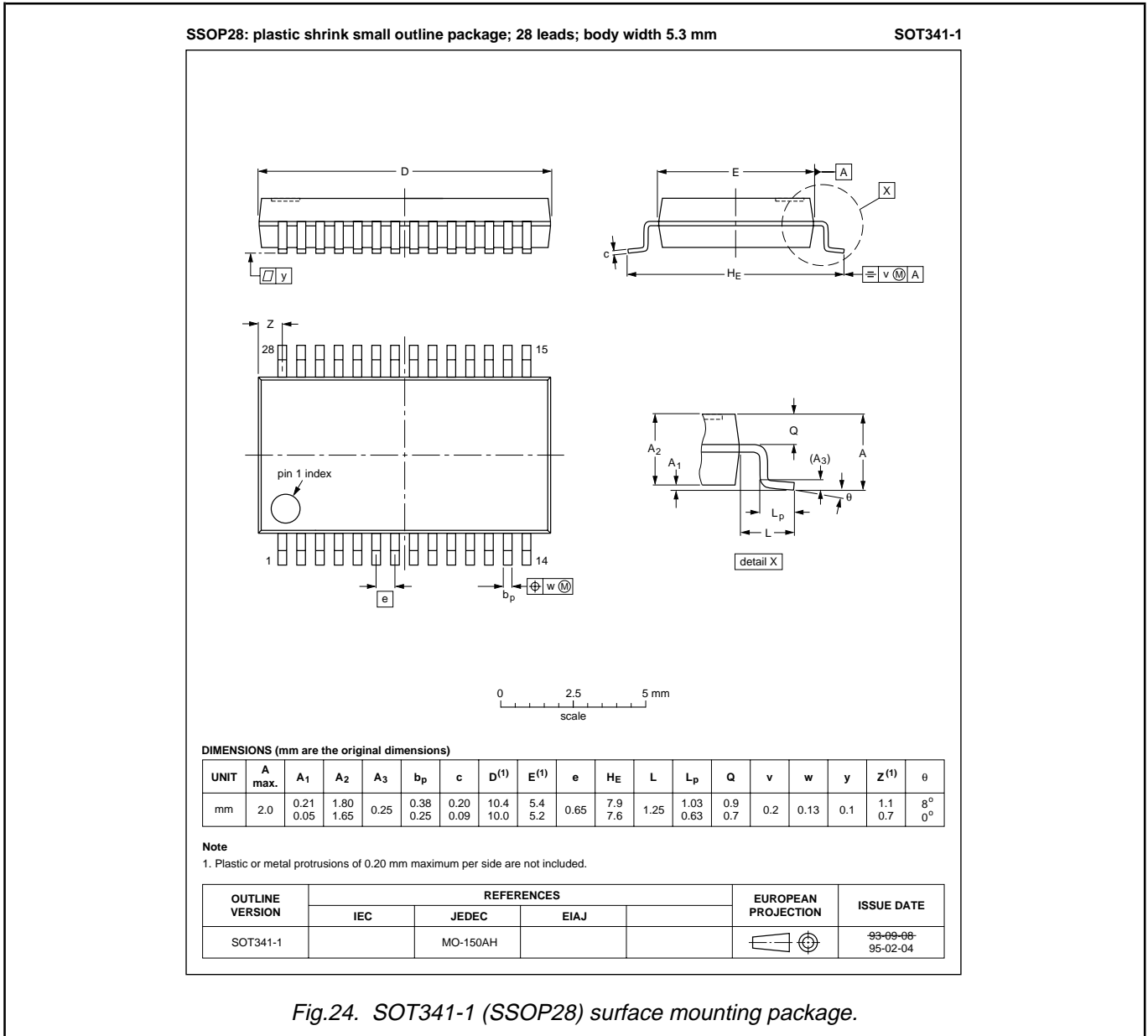


Fig.24. SOT341-1 (SSOP28) surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The leads must be protected against static discharge during transport or handling.
2. Refer to Integrated Circuit Packages, Data Handbook IC26.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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