

# DATA SHEET

## **PHN708**

**7 N-channel 80 mΩ FET array  
enhancement mode MOS  
transistors**

Product specification  
Supersedes data of 1997 Jun 19  
File under Discrete Semiconductors, SC13

1998 Mar 17

# 7 N-channel 80 mΩ FET array enhancement mode MOS transistors

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**FEATURES**

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

**APPLICATIONS**

- Driving high performance three phase brushless DC motors.

**DESCRIPTION**

Seven enhancement mode MOS transistors in a 24-pin plastic SOT340-1 (SSOP24) package. Six of the transistors are in three half-bridge configurations.

**PINNING - SOT340-1 (SSOP24)**

PIN	SYMBOL	DESCRIPTION
1 and 4	d <sub>1</sub>	drain 1
2	s <sub>1</sub>	source 1
3	g <sub>1</sub>	gate 1
5 and 8	d <sub>2</sub>	drain 2
6	s <sub>2</sub>	source 2
7	g <sub>2</sub>	gate 2
9 and 12	d <sub>3</sub>	drain 3
10	s <sub>3</sub>	source 3
11	g <sub>3</sub>	gate 3
13	g <sub>4</sub>	gate 4
14	s <sub>4</sub>	source 4
15, 17, 18, 20, 21, 23, 24	d <sub>4</sub>	drain 4
16	g <sub>5</sub>	gate 5
19	g <sub>6</sub>	gate 6
22	g <sub>7</sub>	gate 7

**CAUTION**

The device is supplied in an antistatic package.  
The gate-source input must be protected against static discharge during transport or handling.

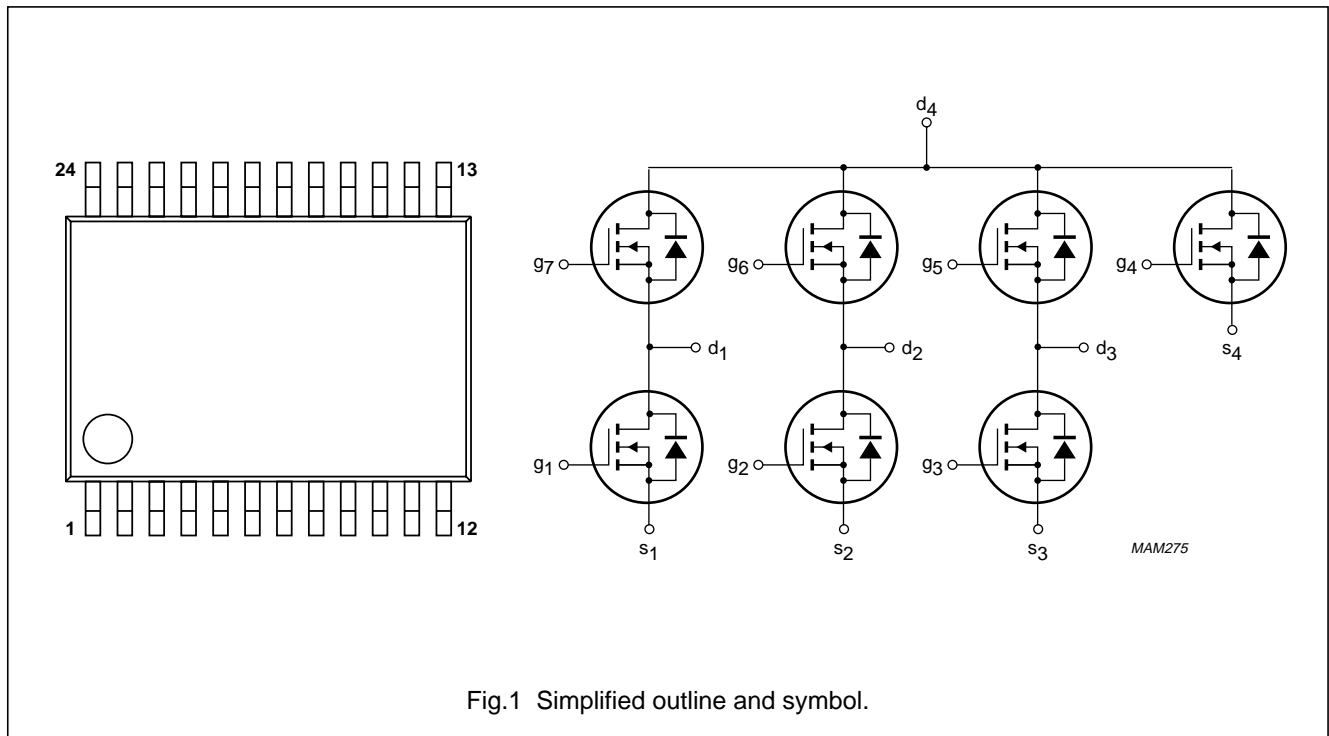


Fig.1 Simplified outline and symbol.

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**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	30	V
$V_{GS}$	gate-source voltage (DC)		–	±20	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$	1	2.8	V
$I_D$	drain current (DC)	$T_s = 80 \text{ °C}$	–	3.1	A
$R_{DSon}$	drain-source on-state resistance	$I_D = 1.5 \text{ A}; V_{GS} = 10 \text{ V}$	–	80	mΩ
$P_{tot}$	total power dissipation	$T_s = 80 \text{ °C}$	–	1.3	W

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

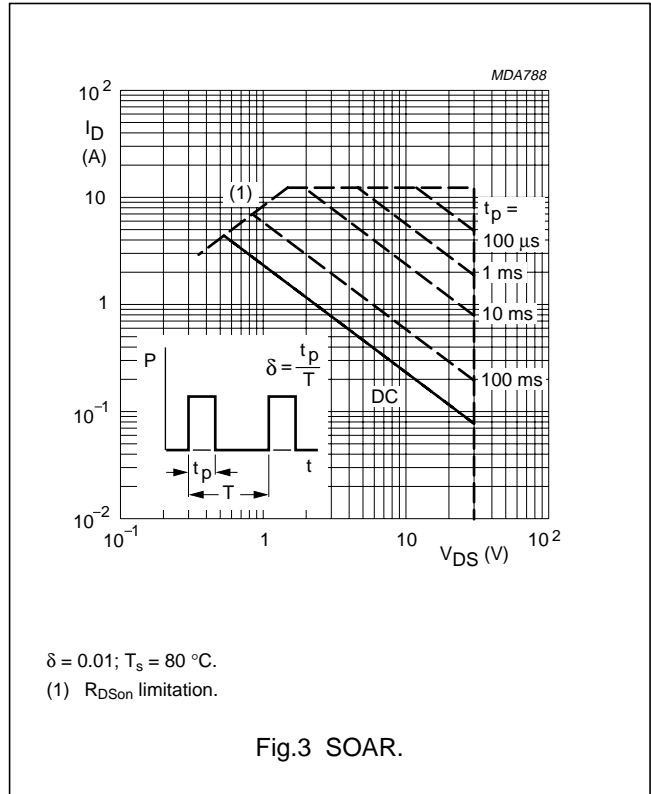
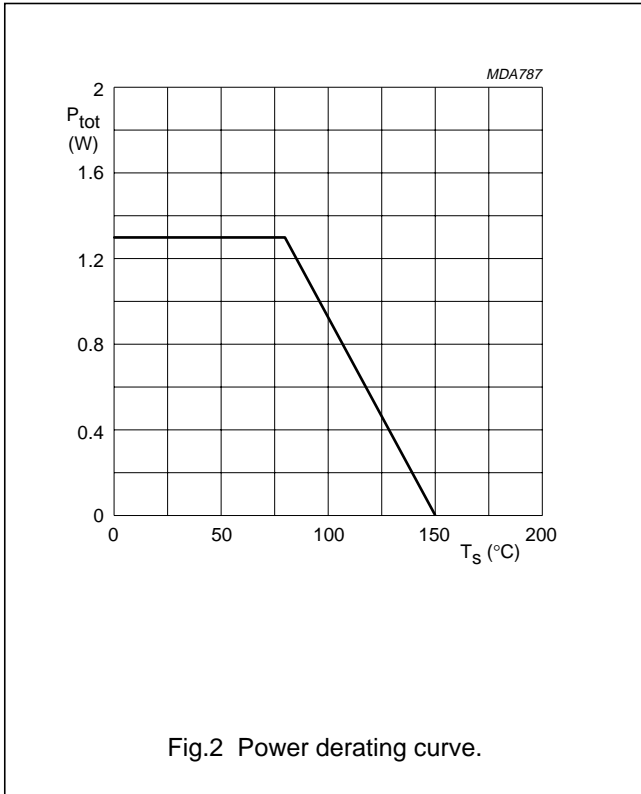
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per FET</b>					
$V_{DS}$	drain-source voltage (DC)		–	30	V
$V_{GS}$	gate-source voltage (DC)		–	±20	V
$I_D$	drain current (DC)	$T_s = 80 \text{ °C}; \text{note 1}$	–	3.1	A
$I_{DM}$	peak drain current	note 2	–	12.4	A
$P_{tot}$	total power dissipation	$T_s = 80 \text{ °C}; \text{note 3}$	–	1.3	W
		$T_s = 80 \text{ °C}; \text{note 4}$	–	1.13	W
		$T_s = 80 \text{ °C}; \text{note 5}$	–	0.92	W
		$T_s = 80 \text{ °C}; \text{note 6}$	–	0.77	W
$T_{stg}$	storage temperature		–55	+150	°C
$T_j$	operating junction temperature		–55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current (DC)	$T_s = 80 \text{ °C}$	–	1.3	A
$I_{SM}$	peak source current	note 2	–	5.2	A

**Notes**

- $T_s$  is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- When only one FET dissipates.
- When either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
- When FET four plus either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
- When all seven FETs dissipate an equal amount of power.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
<b>Per FET</b>				
$R_{th\ j-s}$	thermal resistance from junction to soldering point	note 1	53	K/W
		note 2	62	K/W
		note 3	76	K/W
		note 4	91	K/W

Notes

1. When only one FET dissipates.
2. When either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
3. When FET four plus either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
4. When all seven FETs dissipate an equal amount of power.

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**CHARACTERISTICS**T<sub>j</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per FET</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0; I <sub>D</sub> = 10 μA	30	–	–	V
V <sub>GSth</sub>	gate-source threshold voltage	V <sub>GS</sub> = V <sub>DS</sub> ; I <sub>D</sub> = 1 mA	1	–	2.8	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>GS</sub> = 0; V <sub>DS</sub> = 24 V	–	–	100	nA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = ±20 V; V <sub>DS</sub> = 0	–	–	±100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 0.75 A	–	–	130	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 1.5 A	–	–	80	mΩ
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0; V <sub>DS</sub> = 24 V; f = 1 MHz	–	180	–	pF
C <sub>oss</sub>	output capacitance	V <sub>GS</sub> = 0; V <sub>DS</sub> = 24 V; f = 1 MHz	–	70	–	pF
C <sub>rss</sub>	reverse transfer capacitance	V <sub>GS</sub> = 0; V <sub>DS</sub> = 24 V; f = 1 MHz	–	36	–	pF
Q <sub>G</sub>	total gate charge	V <sub>GS</sub> = 10 V; V <sub>DD</sub> = 15 V; I <sub>D</sub> = 1 A	–	5.4	8	nC
Q <sub>GS</sub>	gate-source charge	V <sub>DD</sub> = 15 V; I <sub>D</sub> = 1 A	–	0.4	–	nC
Q <sub>GD</sub>	gate-drain charge	V <sub>DD</sub> = 15 V; I <sub>D</sub> = 1 A	–	1.6	–	nC
<b>Switching times</b>						
t <sub>d(on)</sub>	turn-on delay time	V <sub>GS</sub> = 0 to 10 V; V <sub>DD</sub> = 20 V; I <sub>D</sub> = 1 A; R <sub>gen</sub> = 6 Ω	–	3	–	ns
t <sub>f</sub>	fall time	V <sub>GS</sub> = 0 to 10 V; V <sub>DD</sub> = 20 V; I <sub>D</sub> = 1 A; R <sub>gen</sub> = 6 Ω	–	2.5	–	ns
t <sub>on</sub>	turn-on switching time	V <sub>GS</sub> = 0 to 10 V; V <sub>DD</sub> = 20 V; I <sub>D</sub> = 1 A; R <sub>gen</sub> = 6 Ω	–	5.5	10	ns
t <sub>d(off)</sub>	turn-off delay time	V <sub>GS</sub> = 10 to 0 V; V <sub>DD</sub> = 20 V; I <sub>D</sub> = 1 A; R <sub>gen</sub> = 6 Ω	–	10	–	ns
t <sub>r</sub>	rise time	V <sub>GS</sub> = 10 to 0 V; V <sub>DD</sub> = 20 V; I <sub>D</sub> = 1 A; R <sub>gen</sub> = 6 Ω	–	6	–	ns
t <sub>off</sub>	turn-off switching time	V <sub>GS</sub> = 10 to 0 V; V <sub>DD</sub> = 20 V; I <sub>D</sub> = 1 A; R <sub>gen</sub> = 6 Ω	–	16	25	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain diode forward voltage	V <sub>GD</sub> = 0; I <sub>S</sub> = 1.25 A	–	–	1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 1.25 A; di/dt = –100 A/μs	–	25	–	ns

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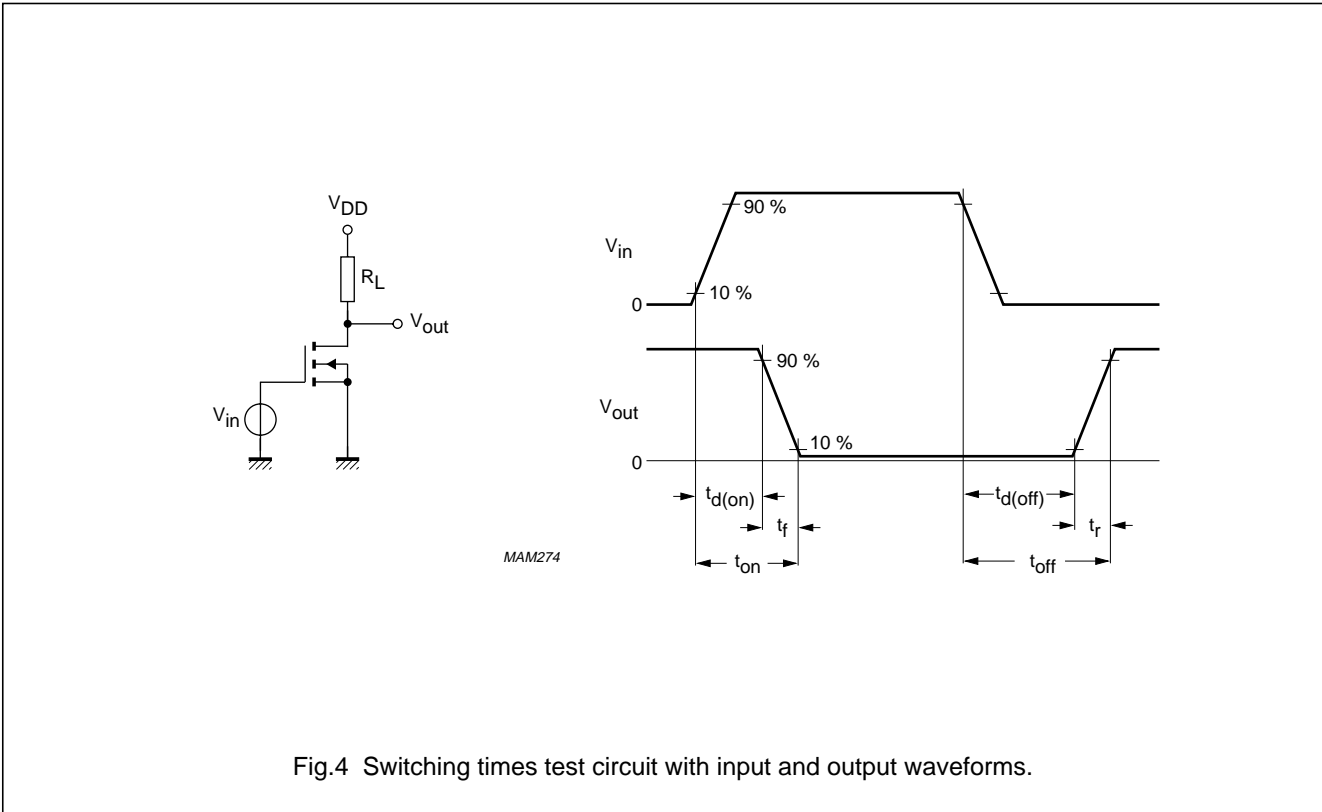


Fig.4 Switching times test circuit with input and output waveforms.

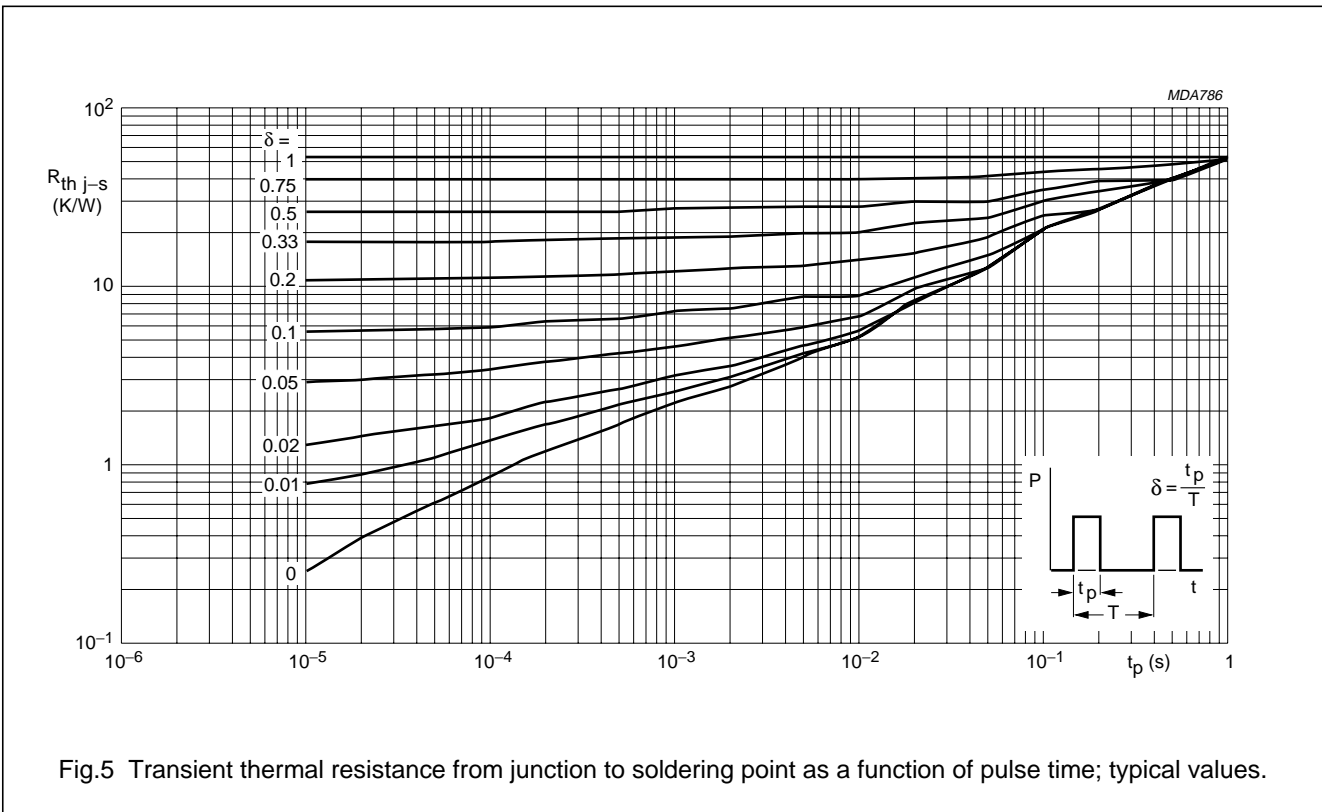
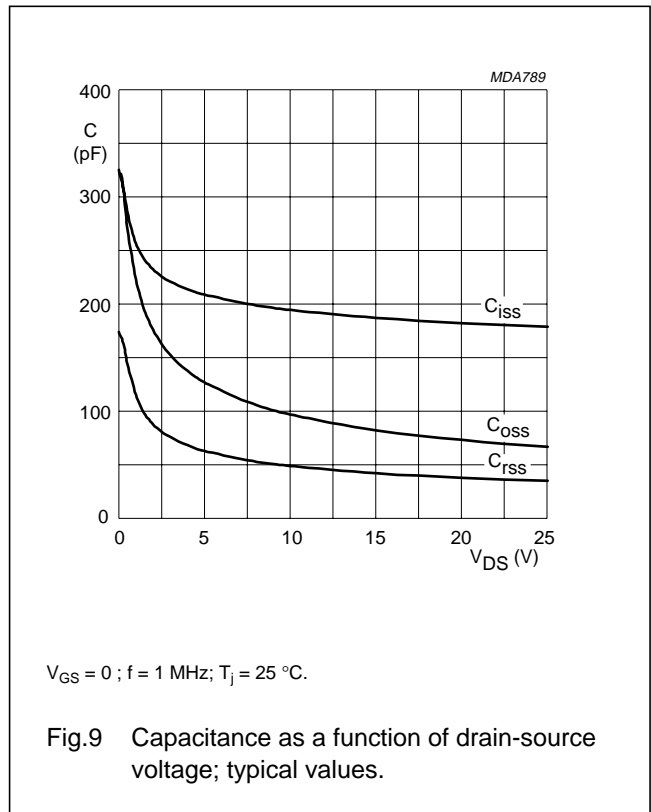
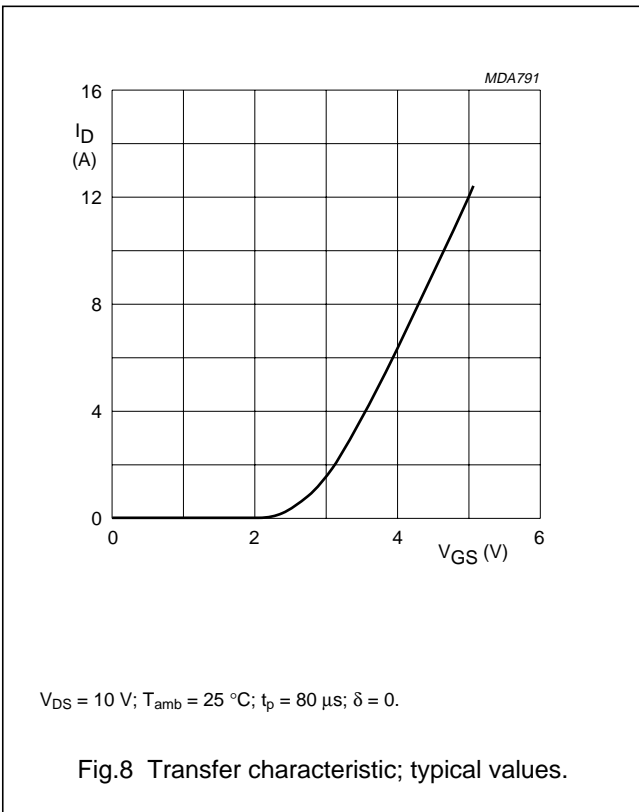
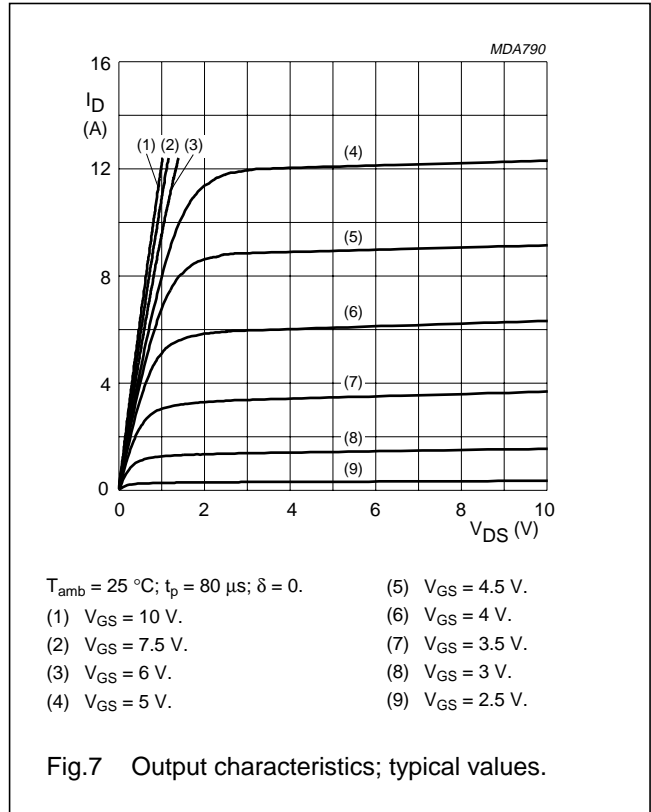
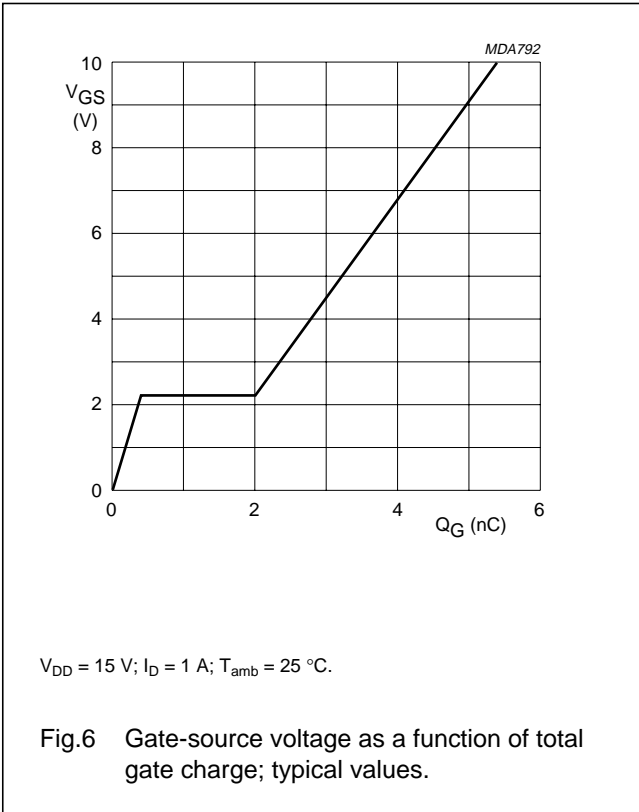


Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

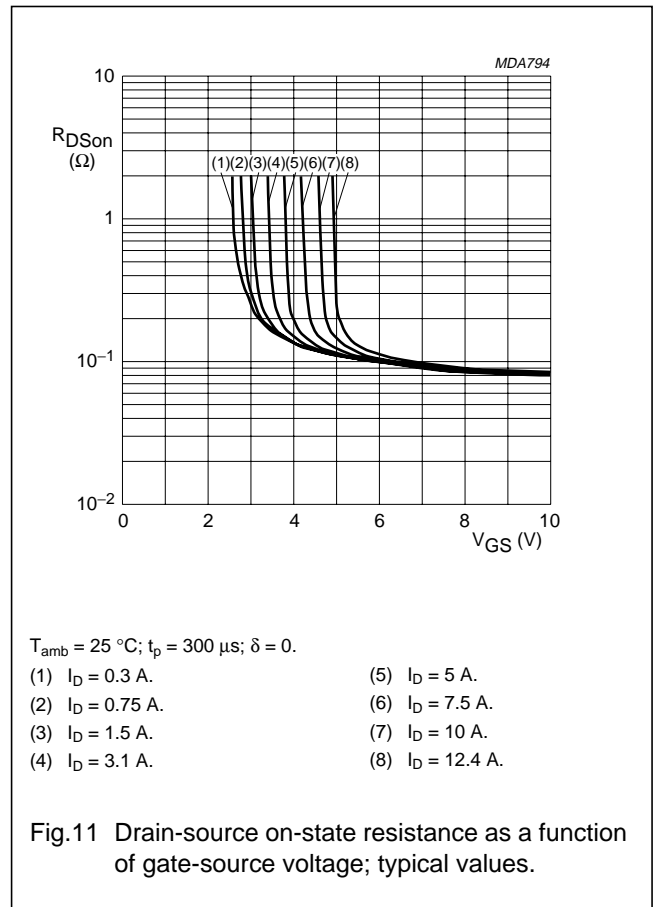
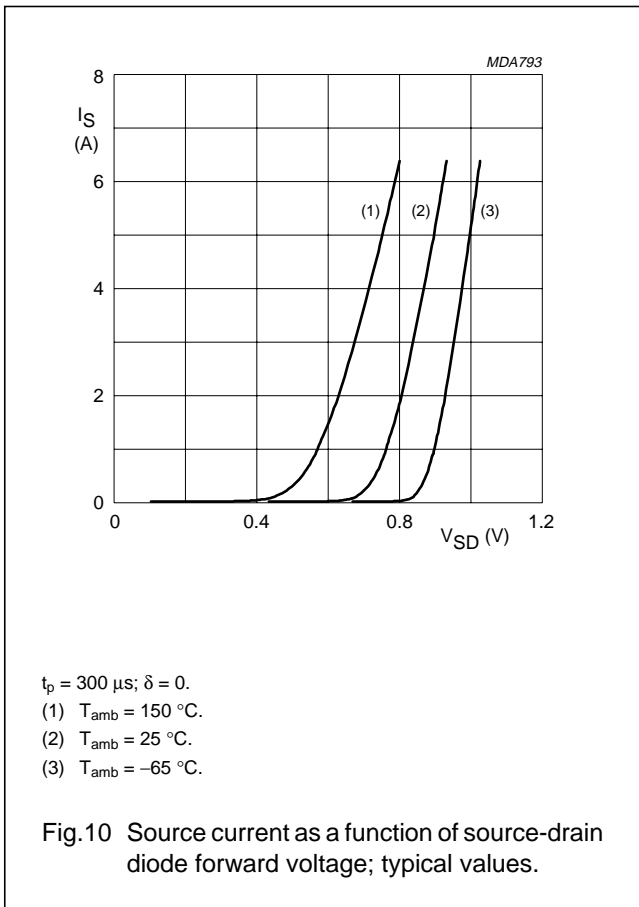
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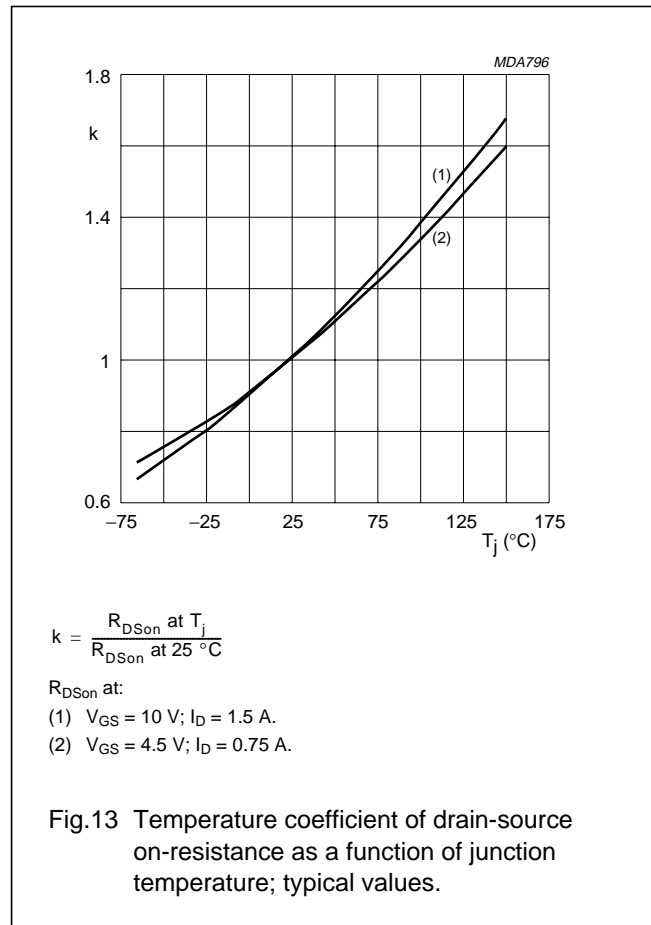
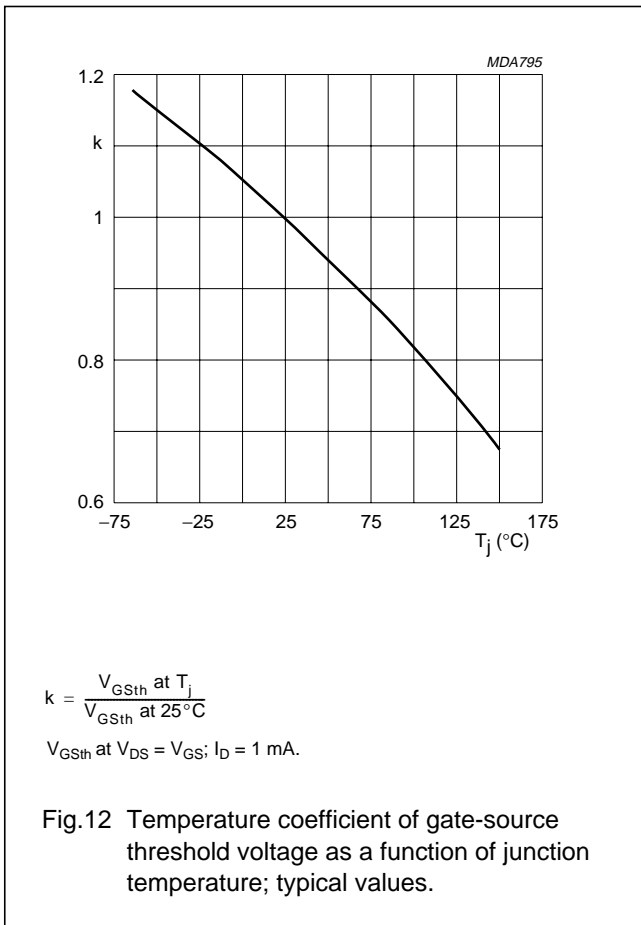
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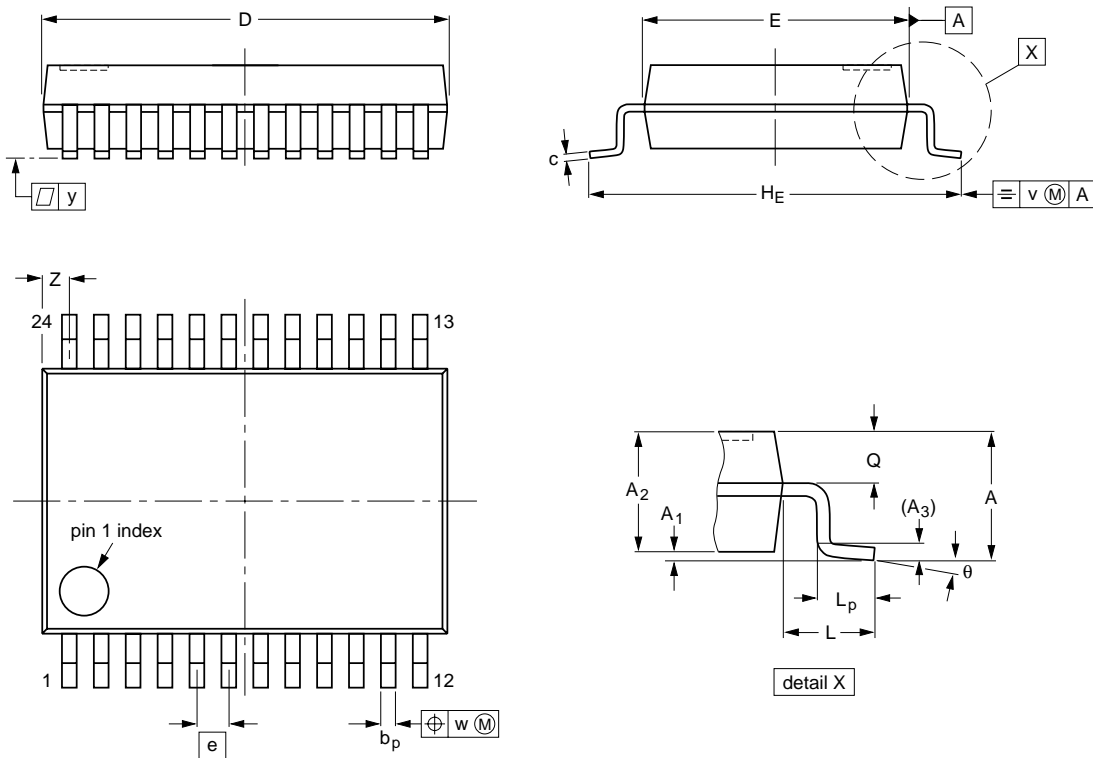
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PACKAGE OUTLINE

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

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## DEFINITIONS

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

135108/00/03/pp12

Date of release: 1998 Mar 17

Document order number: 9397 750 03274

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