

# TrenchMOS™ transistor Standard level FET

PHP37N06T

## GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in DC-DC converters and general purpose switching applications.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	55	V
$I_D$	Drain current (DC)	37	A
$P_{tot}$	Total power dissipation	100	W
$T_j$	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10\text{ V}$	35	mΩ

## PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

## PIN CONFIGURATION



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	55	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
$I_D$	Drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	37	A
$I_D$	Drain current (DC)	$T_{mb} = 100\text{ }^\circ\text{C}$	-	26	A
$I_{DM}$	Drain current (pulse peak value)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	148	A
$P_{tot}$	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	100	W
$T_{stg}, T_j$	Storage & operating temperature	-	-55	175	°C

## ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

## THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	1.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

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### STATIC CHARACTERISTICS

T<sub>j</sub> = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 0.25 mA; T <sub>j</sub> = -55 °C	55 50	- -	- -	V V
V <sub>GS(TO)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = 1 mA T <sub>j</sub> = 175 °C T <sub>j</sub> = -55 °C	2.0 1.0 -	3.0 - -	4.0 - 4.4	V V V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	0.05	10	µA
I <sub>GSS</sub>	Gate source leakage current	V <sub>GS</sub> = ±10 V; V <sub>DS</sub> = 0 V T <sub>j</sub> = 175 °C	-	0.04	1 500	µA µA
±V <sub>(BR)GSS</sub>	Gate source breakdown voltage	I <sub>G</sub> = ±1 mA; T <sub>j</sub> = 175 °C	16	-	-	V
R <sub>DS(ON)</sub>	Drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 17 A T <sub>j</sub> = 175 °C	-	28	35 74	mΩ mΩ

### DYNAMIC CHARACTERISTICS

T<sub>mb</sub> = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> = 25 V; I <sub>D</sub> = 15 A	4	-	-	S
Q <sub>g(tot)</sub>	Total gate charge	I <sub>D</sub> = 30 A; V <sub>DD</sub> = 44 V; V <sub>GS</sub> = 10 V	-	26	-	nC
Q <sub>gs</sub>	Gate-source charge		-	7.5	-	nC
Q <sub>gd</sub>	Gate-drain (Miller) charge		-	11	-	nC
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz	-	700	880	pF
C <sub>oss</sub>	Output capacitance		-	200	240	pF
C <sub>rss</sub>	Feedback capacitance		-	100	140	pF
t <sub>d on</sub>	Turn-on delay time	V <sub>DD</sub> = 30 V; I <sub>D</sub> = 15 A;	-	11	16	ns
t <sub>r</sub>	Turn-on rise time	V <sub>GS</sub> = 10 V; R <sub>G</sub> = 10 Ω	-	35	50	ns
t <sub>d off</sub>	Turn-off delay time	Resistive load	-	25	35	ns
t <sub>f</sub>	Turn-off fall time		-	22	29	ns
L <sub>d</sub>	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L <sub>d</sub>	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L <sub>s</sub>	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T<sub>j</sub> = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>DR</sub>	Continuous reverse drain current		-	-	37	A
I <sub>DRM</sub>	Pulsed reverse drain current		-	-	148	A
V <sub>SD</sub>	Diode forward voltage	I <sub>F</sub> = 25 A; V <sub>GS</sub> = 0 V I <sub>F</sub> = 34 A; V <sub>GS</sub> = 0 V	-	0.95 1.0	1.2 -	V
t <sub>rr</sub>	Reverse recovery time	I <sub>F</sub> = 34 A; -di <sub>F</sub> /dt = 100 A/µs;	-	40	-	ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>GS</sub> = -10 V; V <sub>R</sub> = 30 V	-	0.16	-	µC

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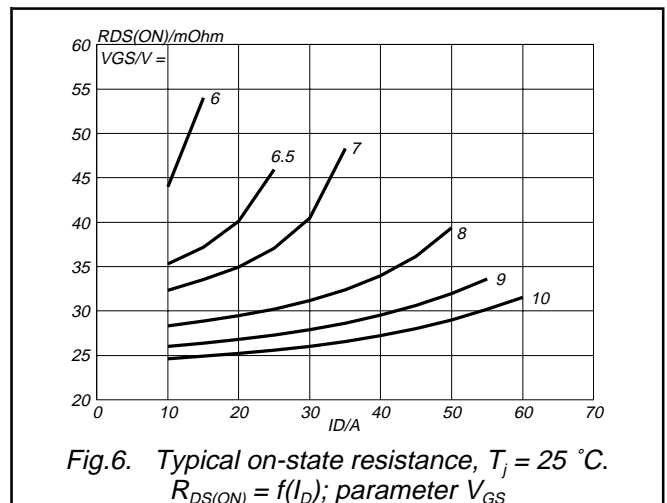
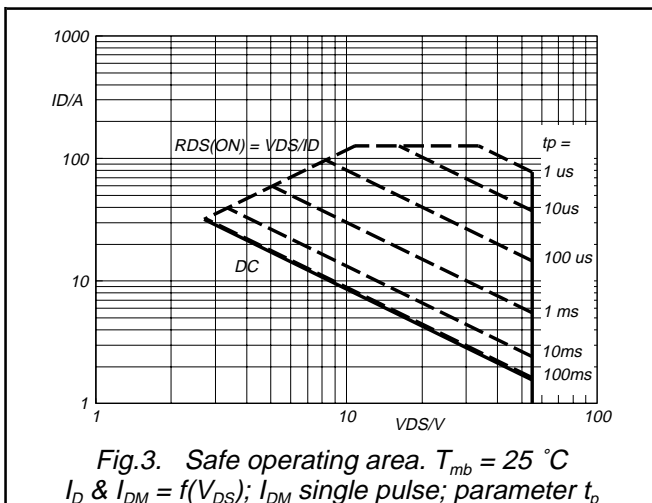
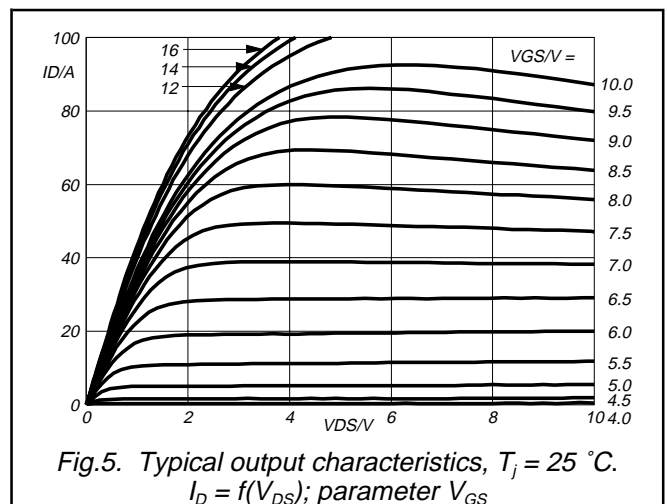
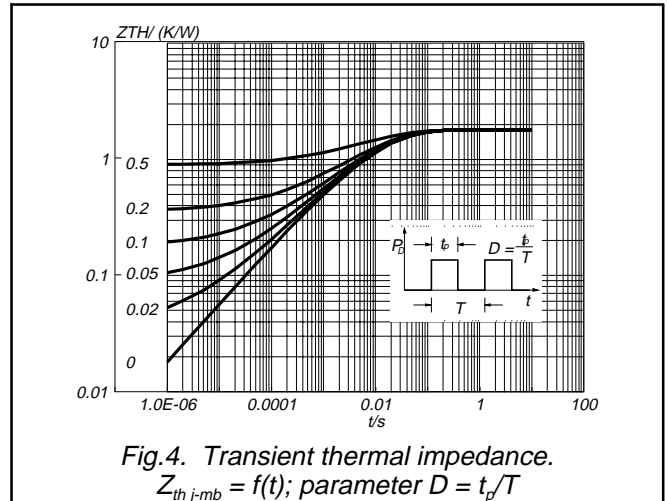
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**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 20 \text{ A}; V_{DD} \leq 25 \text{ V};$ $V_{GS} = 10 \text{ V}; R_{GS} = 50 \Omega; T_{mb} = 25 \text{ }^\circ\text{C}$	-	-	45	mJ

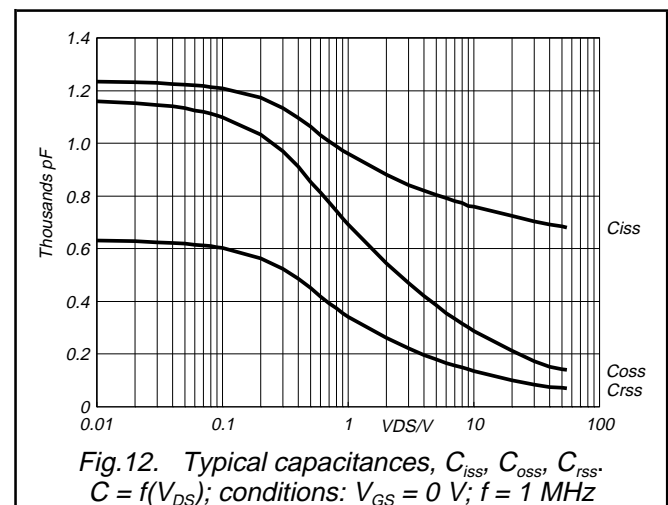
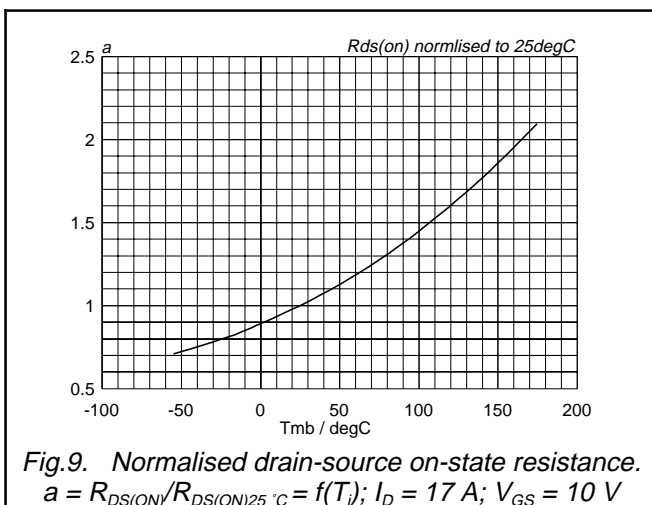
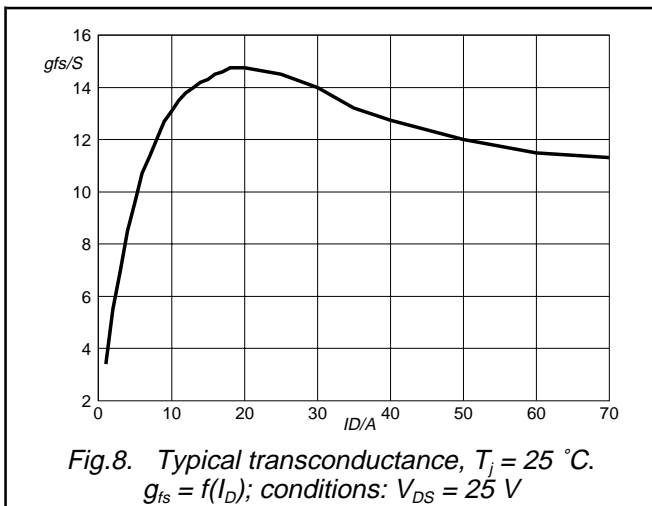
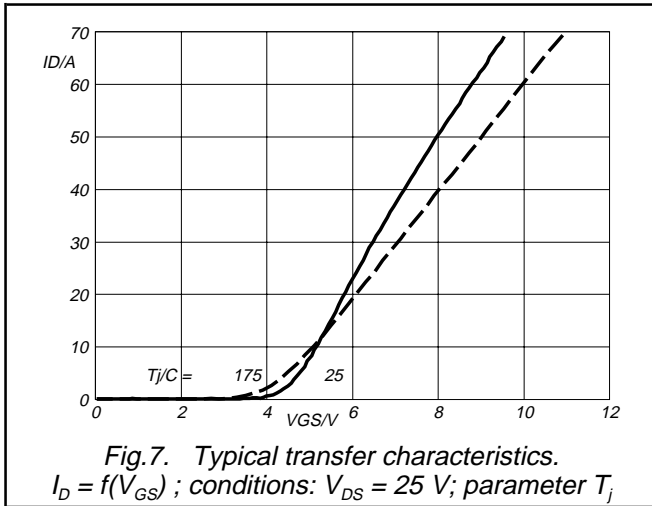
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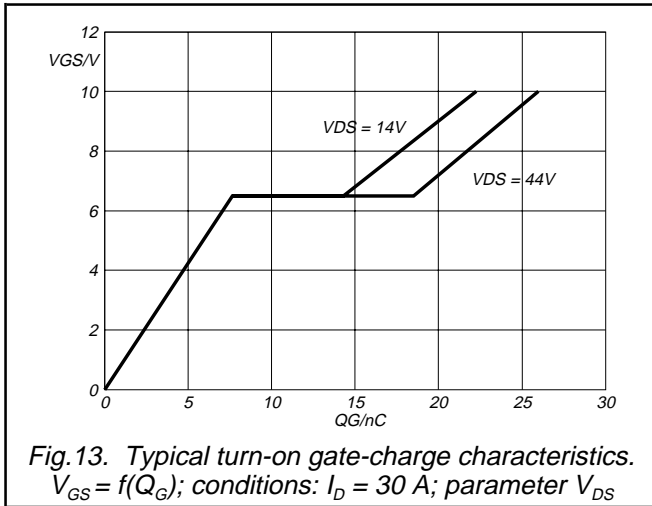


Fig. 13. Typical turn-on gate-charge characteristics.  $V_{GS} = f(Q_G)$ ; conditions:  $I_D = 30\text{ A}$ ; parameter  $V_{DS}$

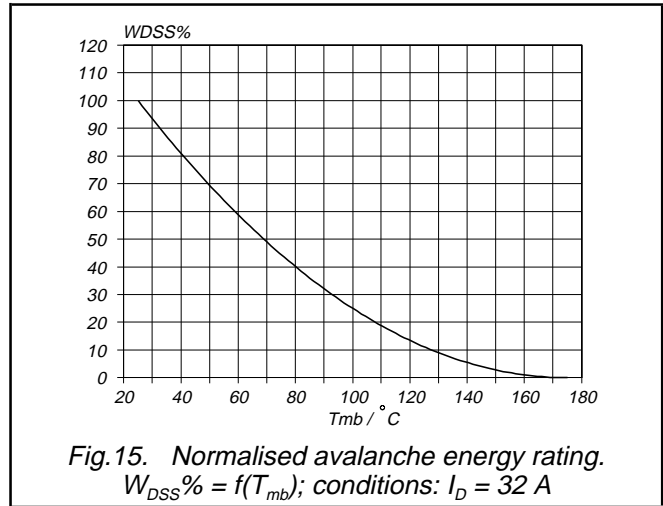


Fig. 15. Normalised avalanche energy rating.  $W_{DSS}\% = f(T_{mb})$ ; conditions:  $I_D = 32\text{ A}$

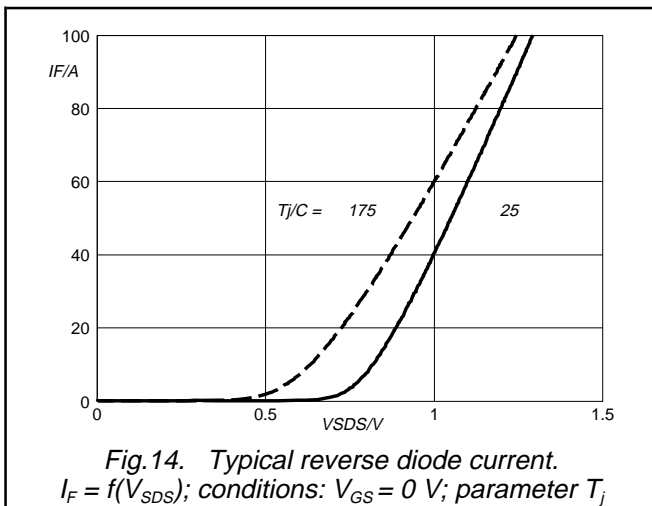


Fig. 14. Typical reverse diode current.  $I_F = f(V_{SDS})$ ; conditions:  $V_{GS} = 0\text{ V}$ ; parameter  $T_j$

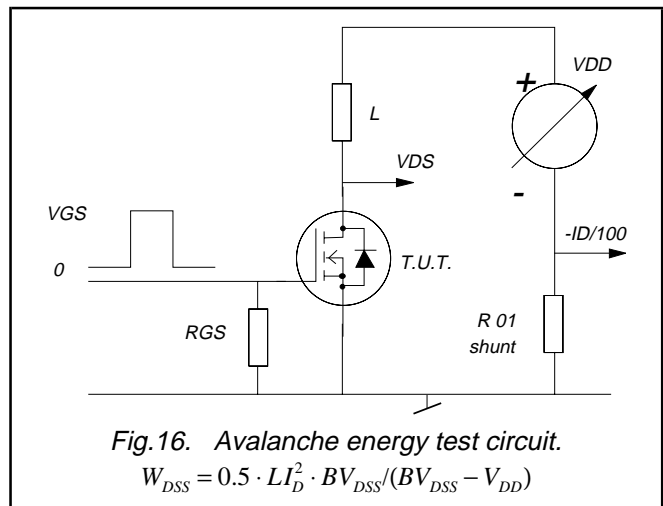


Fig. 16. Avalanche energy test circuit.  $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

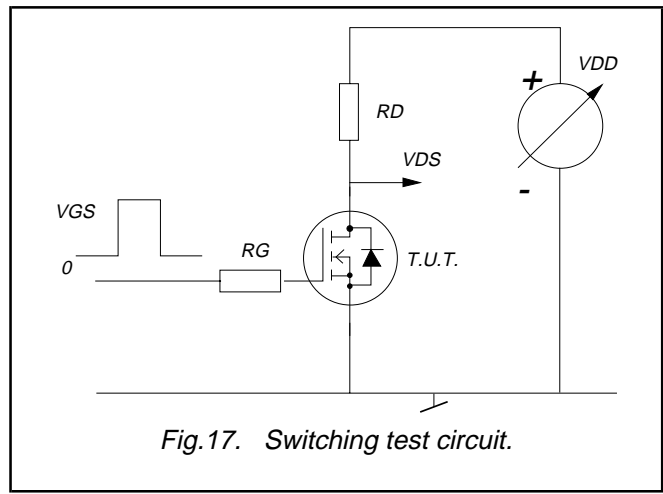


Fig. 17. Switching test circuit.

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**MECHANICAL DATA**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
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<b>Application information</b>	
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