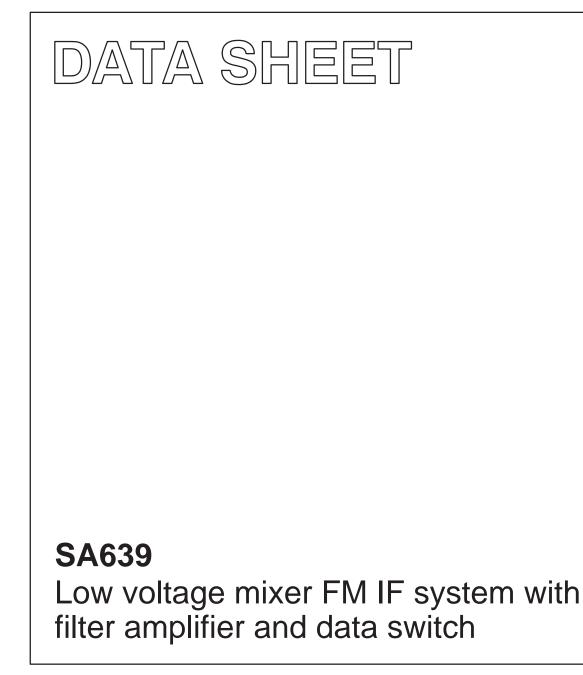
INTEGRATED CIRCUITS



Product specification

1998 Feb 10

IC17 Data Handbook





SA639

DESCRIPTION

The SA639 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two wideband limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), fast RSSI op amps, voltage regulator, wideband data output, post detection filter amplifier and data switch. The SA639 is available in 24-lead TSSOP (Thin shrink small outline package).

The SA639 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The data output provides a minimum bandwidth of 1MHz to demodulate wideband data. The RSSI output is amplified and has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

The post-detection amplifier may be used to realize a low pass filter function. A programmable data switch routes a portion of the data signal to an external integration circuit that generates a data comparator reference voltage.

SA639 incorporates a power down mode which powers down the device when Pin 8 is high. Power down logic levels are CMOS and TTL compatible with high input impedance.

APPLICATIONS

- DECT (Digital European Cordless Telephone)
- FSK and ASK data receivers

FEATURES

- V_{CC} = 2.7 to 5.5V
- Low power consumption: 8.6mA typ at 3V
- Wideband data output (1MHz min.)
- Fast RSSI rise and fall times
- Mixer input to >500MHz
- Mixer conversion power gain of 9.2dB and noise figure of 11dB at 110MHz

PIN CONFIGURATION

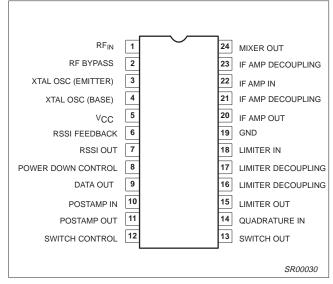


Figure 1. Pin Configuration

- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 92dB of IF Amp/Limiter power gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 80dB
- RSSI output internal op amp
- Post detection amplifier for filtering
- Programmable data switch
- Excellent sensitivity: 2.24μ V into 50Ω matching network for 10dB SNR (Signal to Noise Ratio) with RF at 110MHz and IF at 9.8MHz
- ESD hardened
- Power down mode

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic TSSOP (Thin Shrink Small Outline Package)	-40 to +85°C	SA639DH	SOT-355

SA639

BLOCK DIAGRAM

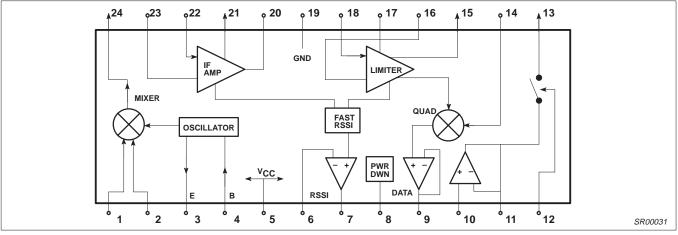


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V _{CC}	Single supply voltage	-0.3 to 6	V
V _{IN}	Voltage applied to any other pin ¹	-0.3 to (V _{CC} +0.3)	V
T _{STG}	Storage temperature range	-65 to +150	°C
T _A	Operating ambient temperature range SA639 ²	-40 to +85	°C

NOTE:

1. Except logic input pins (Pins 8 and 12) which can have 6V maximum.

2. θ_{JA} Thermal impedance (DH package) 117°C/W

DC ELECTRICAL CHARACTERISTICS

 V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS		_	UNITS				
			MIN	-3 σ	TYP	+3 σ	MAX		
V _{CC}	Power supply voltage range		2.7		3.0		5.5	V	
I _{CC}	DC current drain	Pin 8 = LOW, Pin 12 = HIGH		8.33	8.6	8.87	10	mA	
I _{CC}	Standby	Pin 8 = HIGH, Pin 12 = HIGH		131.9	140	148.1	500	μΑ	
	Input ourrept	Pin 8 = LOW					10		
	Input current	Pin 8 = HIGH					4	μA	
	Lenged level	Pin 8 = LOW	0				0.3V _{CC}	V	
	Input level	Pin 8 = HIGH ^{NO TAG}	0.7V _{CC}				6		
t _{ON}	Power up time	RSSI valid (10% to 90%)			10			μs	
t _{OFF}	Power down time	RSSI invalid (90% to 10%)			5			μs	
	Power up settling time	Data output valid			100		200	μs	
	•	•	•						
	Switch closed	Pin 12 = LOW, PIN 8 = LOW	0				0.3 V _{CC}	V	
	Switch open (output tri-state)	Pin 12 = HIGH	0.7 V _{CC}				6	V	
	land an and	Pin 12 = LOW					10		
	Input current	Pin 12 = HIGH					4	μA	
	Switch activation time				0.5		1	μs	

NOTE:

1. When the device is forced in power down mode via Pin 8, the Data Switch will output a voltage close to 1.6V and the state of the switch control input will have no effect.

SA639

AC ELECTRICAL CHARACTERISTICS

 $T_A = 25^{\circ}$ C; $V_{CC} = +3V$, unless otherwise stated. RF frequency = 110.592MHz ;LO frequency = 120.392MHz; IF frequency = 9.8MHz; RF level = -45dBm; FM modulation = 576kHz with ±288kHz peak deviation, discriminator tank circuit Q=4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

			LIMITS SA639						
SYMBOL	PARAMETER	TEST CONDITIONS							
			MIN	-3 σ	TYP	+3 σ	MAX		
	section (ext LO = -14dBm)								
f _{IN}	Input signal frequency				500			MHz	
fosc	External oscillator (buffer)		0.2		500			MHz	
	Noise figure at 110MHz			10.4	11	11.6		dB	
	Third-order input intercept point	Matched f1=110.592MHz; f2=110.852MHz		-11	-9.5	-8		dBm	
	Conversion power gain		6	8.6	9.2	11.1		dB	
	RF input resistance	Single-ended input			800			Ω	
	RF input capacitance				3.5			pF	
	Mixer output resistance	(Pin 24)			330			Ω	
F section	· · ·								
	IF amp gain		1	38.86	40	41.14		dB	
	Limiter gain		1	50.44	52	53.56		dB	
	Input limiting -3dB	Test at Pin 22	1		-100			dBm	
	IF input impedance				330			Ω	
	IF output impedance				330			Ω	
	Limiter input impedance				330			Ω	
	Limiter output impedance				300			Ω	
	Limiter output level with no load				130			mV _{RM}	
RF/IF sect	tion (ext LO = -14dBm)					1		-	
	Data level	$R_{1} = 10k\Omega, C_{1} = 30pF$	260		360	1		mV _{P-F}	
	Data bandwidth			2.1	2.4	2.7		MHz	
S/N	Signal-to-noise ratio	No modulation for noise	1	56.1	60	63.9		dB	
	AM rejection	80% AM 1kHz		34.8	36	37.2		dB	
		RF level = -90dBm	0	0.232	0.4	0.568	0.75		
	RF RSSI output with buffer	RF level = -45dBm	0.5	0.732	0.9	1.068	1.3		
		RF level = -10dBm	0.8	1.032	1.2	1.368	1.6	1	
	RF RSSI output rise time	IF frequency = 9.8MHz							
	(10kHz pulse, w/ 9.8MHz filter)	RF level = -45dBm			0.8				
	(no RSSI bypass capacitor)	RF level = -28dBm			0.8			μs	
	RF RSSI output fall time	IF frequency = 9.8MHz						-	
	(10kHz pulse, w/ 9.8MHz filter)	RF level = -45dBm			2.0				
	(no RSSI bypass capacitor)	RF level = -28dBm			1.8			μs	
	RSSI range		1		80			dB	
	RSSI accuracy				±1.5			dB	
	SINAD	RF level = -85dBm	1	9.45	12	14.55		dB	
	S/N	RF level = -100dBm		5.8	10	14.2		dB	

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AC ELECTRICAL CHARACTERISTICS (Continued)

			LIMITS						
SYMBOL	PARAMETER	TEST CONDITIONS	SA639						
			MIN	-3 σ	TYP	+3 σ	MAX		
Post detec	ction filter amplifier						-		
	Amplifier 3dB bandwidth	AC coupled: $R_L = 10k\Omega$, $C_L = 33pF$		11.7	12.8	13.8		MHz	
	Amplifier gain	AC coupled: $R_L = 10k\Omega$, $V_{OUT DC} = 1.6V$			-0.2			dB	
	Slew rate	AC coupled: $R_L = 10k\Omega$, $C_L = 33pF$			2.4			V/µs	
	Input resistance		300					kΩ	
	Input capacitance						3	pF	
	Output impedance				150		800	Ω	
	Output load resistance	AC coupled	5					kΩ	
	Output load capacitance ¹	AC coupled			30			pF	
	DC output level ²		1.5	1.682	1.7	1.718	1.9	V	
Data swite	:h	-				•			
	DC input voltage range ³		1.2		1.6		2.0	V	
	AC input swing				400			mV _{P-P}	
	Input impedance		100					kΩ	
	Input capacitance						5	pF	
	Output load resistance				500			Ω	
Through N	lode (Pin 12 = LOW)	-							
	AC voltage gain ⁴				-1.5			dB	
	Output drive capability	Sink/source, V _{OUT DC} = 1.6V	3					mA	
	Slew rate	V _{OUT DC} = 1.6V			>14.0			V/µs	
	Static offset voltage ⁵	V _{IN DC} = 1.2 to 2.0V		-0.6	0.30	1.2	±5	mV	
	Description for the large 2 fo		-7				+7		
	Dynamic offset voltage ^{2, 6}	V _{IN DC} = 1.4 to 2.0V; V _{CC} = 3.0 to 5.0V; RF level = -40 to -5 dBm	-10				+10	- mV	
Tri-State N	lode (Pin 12 = HIGH)								
	Output leakage current	V _{OUT DC} = 1.2 to 2.0V		9.5	20	30.5	100	nA	

NOTES:

1. Includes filter feedback capacitance, comparator input capacitance. PCB stray capacitances and switch input capacitance.

2. Demodulator output DC coupled with Post Detection Filter Amplifier input and the demodulator tank exactly tuned to center frequency.

3. Includes DC offsets due to frequency offsets between Rx and Tx carrier and demodulator tank offset due to mis-tuning.

4. With a 400mV_{P-P} sinusoid at 600kHz driving Pin 10. Output load resistance 500Ω in series with 10nF.

5. With a DC input and capacitor in the RC load fully charged.

7. Standard deviations are measured based on application of 60 parts.

^{6.} The switch is closed every 10ms for a duration of 40µs. The DC offset is determined by calculating the difference of 2 DC measurements, which are determined as follows: 1) The first DC value is measured at the integrating capacitor of the switch when the switch is in the closed position immediately before it opens. The value to be measured is in the middle of the peak-to-peak excursion of the superimposed sine-wave. (DClow + (DChigh – DClow)/2). 2) The second DC value (calculated as above) is measured at Pin 11 immediately after the switch opens, and is the DC value which gives the largest DC offset to the first DC measurement within a 400µs DECT burst. Minimum and maximum limits are not tested, however, they are guaranteed by design and characterization using an optimized layout and application circuit.

SA639

CIRCUIT DESCRIPTION

The SA639 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 44dB(v) of gain from a 50 Ω source. The bandwidth of the limiter is about 28MHz with about 58dB(v) of gain from a 50 Ω source. However, the gain/bandwidth distribution is optimized for 9.8MHz, 330 Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as digital cordless phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 11dB, conversion power gain of 9.2dB, and input third-order intercept of -9.5dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330 Ω resistor permitting direct connection to a 330 Ω ceramic filter. The input resistance of the limiting IF amplifiers is also 330 Ω . With most 330 Ω ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 6dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 20) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequency at 9.8MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA) of the quadrature is a low impedance voltage output. This output is designed to handle a minimum bandwidth of 1MHz. This is designed to demodulate wideband data, such as in DECT applications.

Post Detection Filter Amplifier

The filter amplifier may be used to realize a group delay optimized low pass filter for post detection. The filter amplifier can be configured for Sallen & Key low pass with Bessel characteristic and a 3dB cut frequency of about 800kHz.

The filter amplifier provides a gain of 0dB. The output impedance is less than 500Ω in order to reduce frequency response changes as a result of amplifier load variations. The filter amplifier has a 3dB bandwidth of at least 4 MHz in order to keep the amplifier's

frequency response influence on the filter group delay characteristic at a minimum. At the center of the carrier it is mandatory to provide a filter output DC bias voltage of 1.6V in order to be within the input common mode range of the external data comparator. The filter output DC bias voltage specification holds for an exactly center tuned demodulator tank and for the demodulator output connected to the filter amplifier input.

Data Switch

The SA639 incorporates an active data switch used to derive the data comparator reference voltage by means of an external integration circuit. The data switch is typically closed for 10 μ s before and during reception of the synchronization word pattern, and is otherwise open. The external integration circuit is formed by an R/C low pass with a time constant of 5 to 10 μ s.

The active data switch provides excellent tracking behavior over a DC input range of 1.2 to 2.0V. For this range with an RC load (no static current drawn), the DC output voltage will not differ more than \pm 5mV from the input voltage. Since the active data switch is designed to behave like a non-linear charge pump (to allow fast tracking of the input signal without slew rate limitations under dynamic conditions of a 576kHz input signal with 400mV_{P-P} and the RC load), the output signal will have a 340mV_{P-P} output with a DC average that will not vary from the input DC average by more than \pm 10mV.

The data switch is able to sink/source 3mA from/to the external integration circuit in order to minimize the settling time after long power-down periods (DECT paging mode). In addition, during power-down conditions a reference voltage of approximately 1.6V will be used as the input to the switch. The switch will be in a low current mode to maintain the voltage on the external RC load. This will further reduce the settling time of the capacitor after power-up. It should be noted that during power-down the switch can only source and sink a trickle current (10 μ A). Thus, the user should make sure that other circuits (like the data comparator inputs) are not drawing current from the RC circuit.

The data switch provides a slew rate better than $1V/\mu s$ in order to track with system DC offset from receive slot to receive slot (DECT idle lock or active mode). When the data switch is opened the output is in a tri-state mode with a leakage current of less than 100nA. This reduces discharge of the external integration circuit. When powered-down, the data switch will output a reference of approximately 1.6V to maintain a charge on the external RC circuit.

A Receive Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 80dB and is temperature compensated. This log signal strength indicator exceeds the criteria for DECT cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20log V_{OUT}/V_{IN}$

SA639

PIN No.	PIN MNEMONIC			PIN No.	PIN MNEMONIC		EQUIVALENT CIRCUIT
1	RF IN	+1.07	0.8k 0.8k	6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	0.00	
4	XTAL OSC	+2.32	<u>з</u> <u>т</u> <u>т</u> <u>т</u> <u>т</u> 150µА <u>т</u> <u>т</u>	9	DATA OUT	+1.7	
5	V _{CC}	+3.00	5 VREF O BANDGAP O	10	POST AMP IN	+1.70	10 — 20µА — 20µА — SR00032

PIN FUNCTIONS All DC voltages measured with Pin 8 = Pin 12 = Pin 19 = 0V, Pin 5 = 3V and Pin 9 connected to Pin 10.

Figure 3. Pin Functions

SA639

PIN FUNCTIONS (continued)

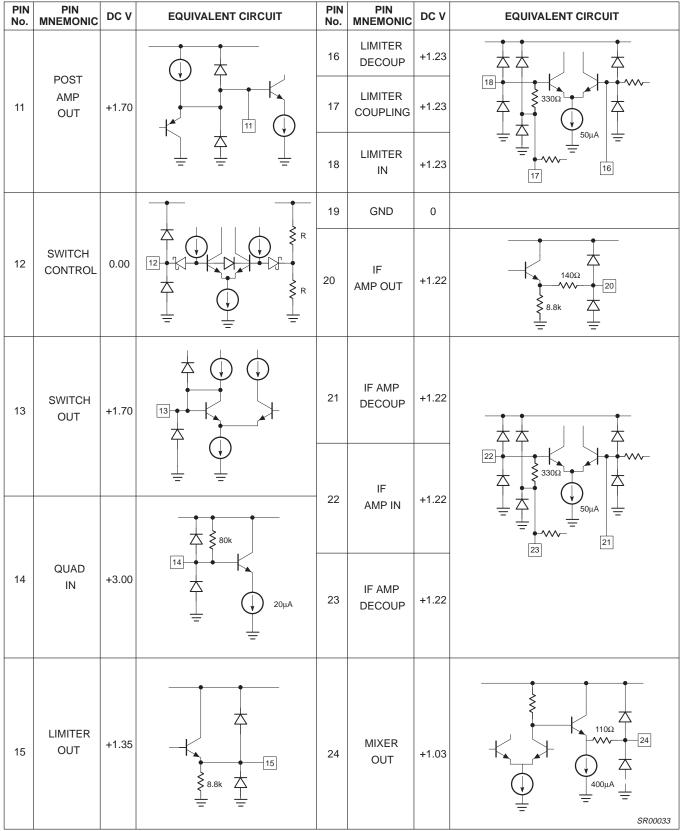


Figure 4. Pin Functions (cont.)

SA639

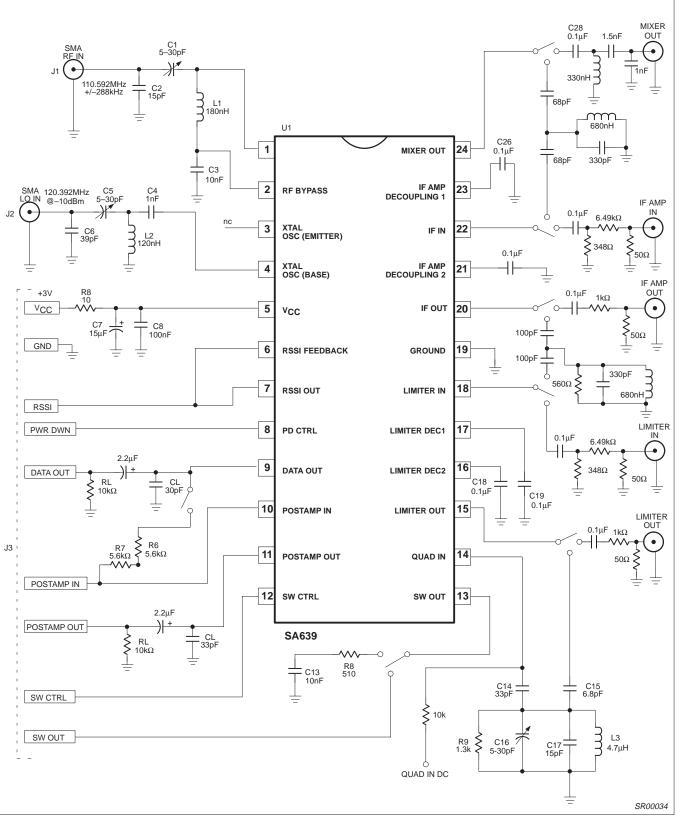


Figure 5. SA639 Test Circuit

SA639



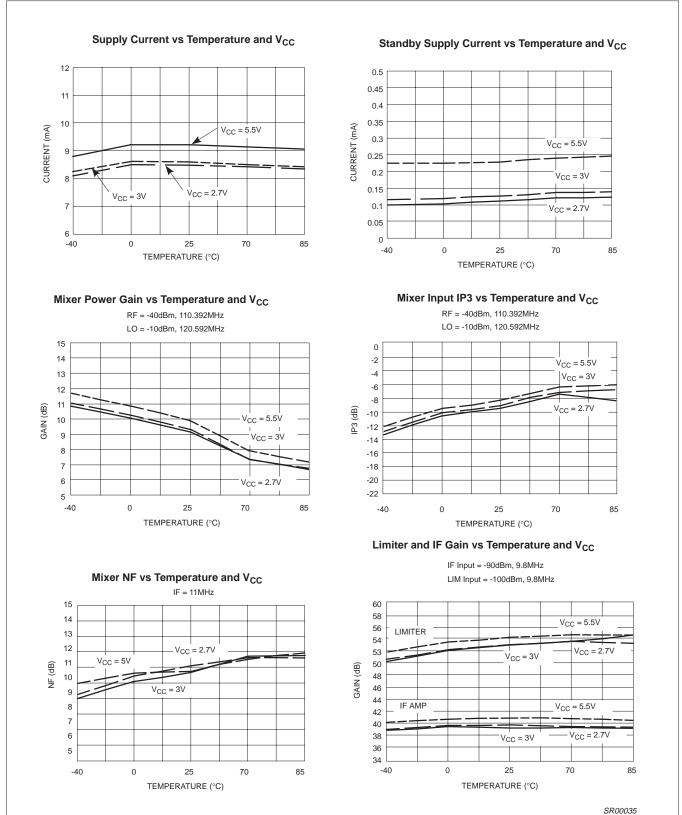


Figure 6. Typical Performance Characteristics

SA639

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

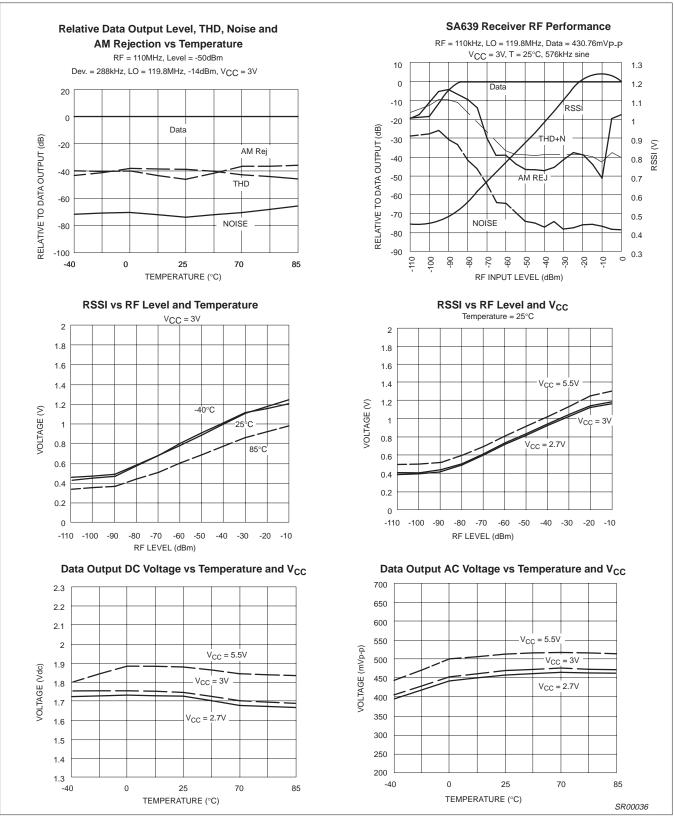
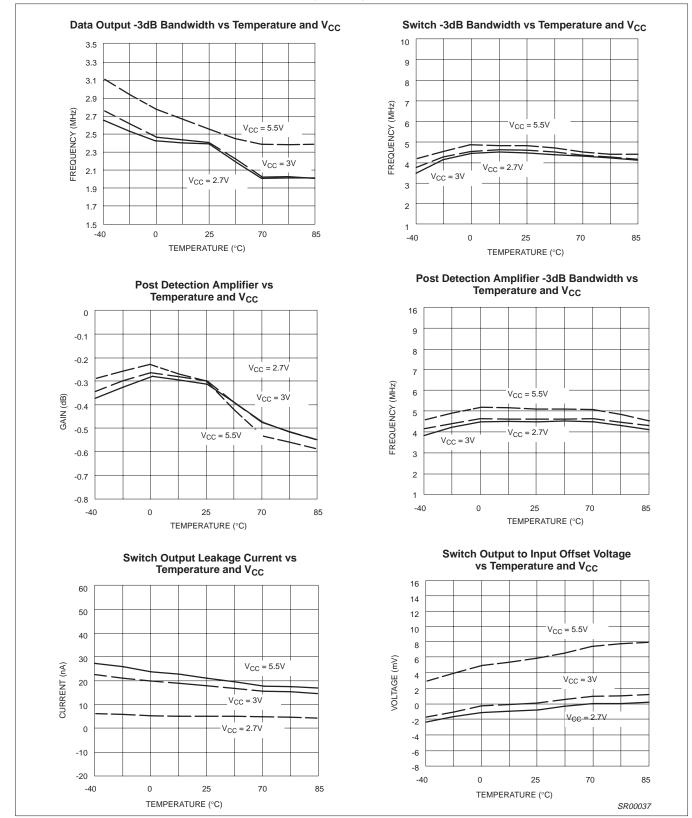


Figure 7. Typical Performance Characteristics (cont.)

SA639



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Figure 8. Typical Performance Characteristics (cont.)

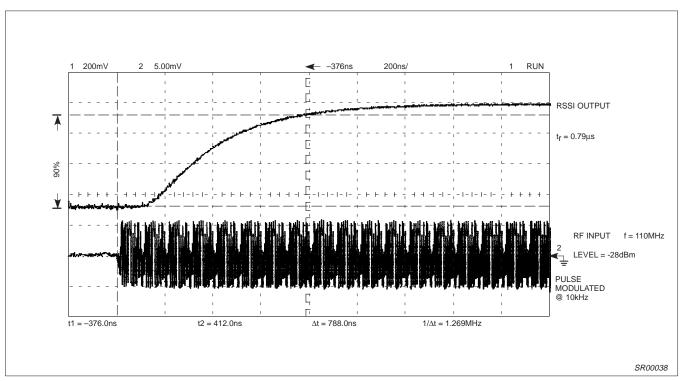


Figure 9. SA639 RSSI Rise Time

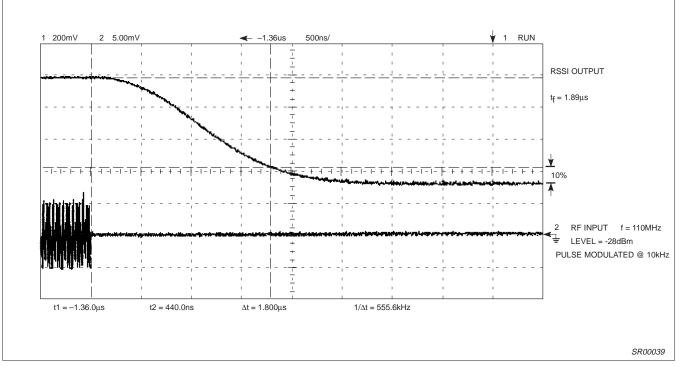


Figure 10. SA639 RSSI Fall Time

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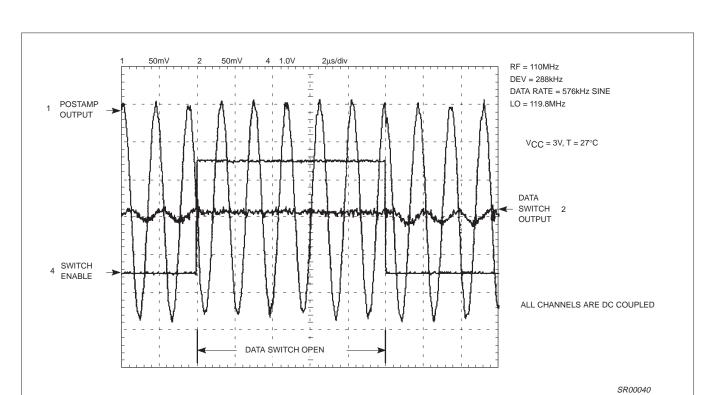


Figure 11. SA639 System Dynamic Response

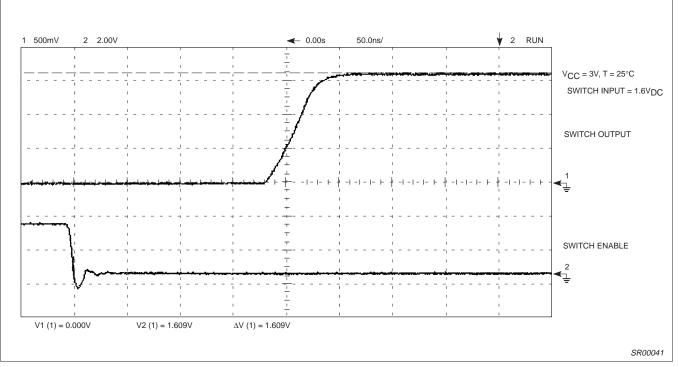
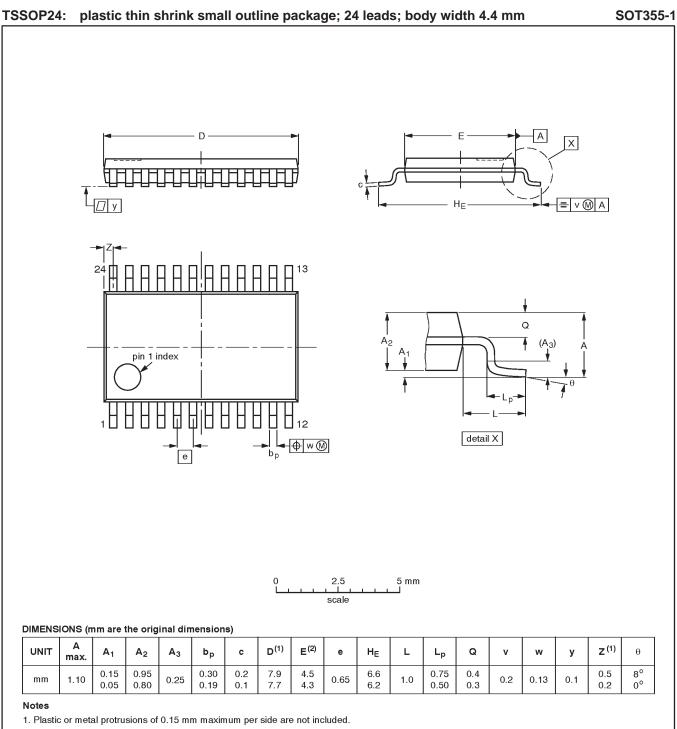


Figure 12. SA639 Data Switch Activation Time

SA639

SA639

Product specification



2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	REFERENCES EUROPEAN		ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT355-1		MO-153AD				- 93-06-16- 95-02-04

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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微波光电部专业代理经销高频、微波、光纤、光电元器件、组件、部件、模块、整机;电磁兼容元器件、材料、设备;微波 CAD、EDA 软件、开发测试仿真工具;微波、光纤仪器仪表。 欢迎国外高科技微波、光纤厂商将优秀产品介绍到中国、共同开拓市场。长期大量现货专业批发 高频、微波、卫星、光纤、电视、CATV 器件: 晶振、VCO、连接器、PIN 开关、变容二极管、开 关二极管、低噪晶体管、功率电阻及电容、放大器、功率管、MIIC、混频器、耦合器、功分器、 振荡器、合成器、衰减器、滤波器、隔离器、环行器、移相器、调制解调器;光电子元器件和组 件:红外发射管、红外接收管、光电开关、光敏管、发光二极管和发光二极管组件、半导体激光 二极管和激光器组件、光电探测器和光接收组件、光发射接收模块、光纤激光器和光放大器、光 调制器、光开关、DWDM 用光发射和接收器件、用户接入系统光光收发器件与模块、光纤连接器、 光纤跳线/尾纤、光衰减器、光纤适 配器、光隔离器、光耦合器、光环行器、光复用器/转换器; 无线收发芯片和模组、蓝牙芯片和模组。

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