DATA SHEET

SAA7811HL
Single-chip DVD-ROM

Preliminary specification
File under Integrated Circuits, IC22

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FEATURES

Host interface

- Enhanced Integrated Drive Electronics (IDE) Advanced Technology Attachment Program Interface (ATAPI) host interface
- Built-in 12-byte ATAPI Packet command First-In, First-Out (FIFO)
- Supports Advanced Technology Attachment (ATA) and ATA-2 PIO and multi-word Direct Memory Access (DMA) data transfer modes
- Supports ATA/ATAPI-4 Ultra DMA transfer modes with data rate up to 33 MBytes/s
- Configurable as generic DMA interface, for use with external host interface devices
- Automatic sequencing of ATAPI packet command protocol; including command termination
- Automatic determination of block length for mode2, form 1 and form 2 sectors (block length transferred is programmable).

Block decoder

- Supports CD-ROM, CD-R and CD-R/W; CD-DA and DVD-ROM formats
- Supports real time error detection and correction in hardware for CD-ROM mode
- CD-ROM error corrector switchable between single or dual pass (both with Error Detection/Correction [EDC])
- Internal registers are memory-mapped
- Embedded DVD-video authentication module.

Buffer memory controller

- Supports up to 2 MBytes of DRAM buffer
- Block based sector addressing.

Channel decoder

- Selectable differential and single-ended HF inputs; compatible with TZA1033 (DVDalas2plus) and TZA1020A (Aeger2); single-ended input has bypassable AGC
- Internal 6-bit ADC
- Digital PLL and slicer for HF clock regeneration
- Supports Eight-to-Fourteen Modulation (EFM) and EFM+ demodulation
- Full CD error correction strategy; t = 2 and e = 4
- On-chip CD error corrector memory with ±8 frame jitter margin
- Built-in hardware for double pass DVD error corrector; (can correct 5 errors in C1 frame and 16 errors in C2 frame)
- Error corrector monitor signal available
- I^{2}C-bus output available via programmable vampire pins.

Spindle motor control

- Advanced motor control loop allows Constant Angular Velocity (CAV), Constant Linear Velocity (CLV) and pseudo-CLV playback
- Support for 3-pin and 1-pin tacho control
- Motor control via incoming bit stream or tacho.

Speed operation

- Supports up to 56 × CD-ROM playback
- Supports up to 10 × DVD-ROM playback.

Multimedia functions and built-in DAC

- Supports audio playback via DRAM buffer; allows audio discs to be played at higher speeds
- IEC958 (SPDIF, AES/EBU and DOBM) output with Q to W subcode bits and programmable category code, output at n = 1 rate
- Built-in digital audio DAC including: –4 × oversampling filter
- Built-in digital volume control, attenuator and single-sample interpolator
- Separate left and right channel routing and mute control.

Microcontroller interface

- Embedded microcontroller can operate as 33 MHz or 67 MHz equivalent 80C51
- Embedded co-processor for fast multiply, divide, shift, and normalize instructions; supported by C-compilers
- Co-processor for MSF calculations
- Memory mapped interfaces to sub functions
- External microcontroller support

- Embedded SRAM (1.5 kbytes Xdata, 512 bytes Idata, 224 bytes data and registers)
- 4 banks: on Idata and registers; for better multi-tasking support
- External flash EPROM programming support
  - Serial boot possible with empty flash EPROM
  - Internal program upload support.
- Code space support up to 1 Mbyte through built-in bank switching
- Debug interface for embedded microcontroller.

Servo processor

- Switched current analog-to-digital converters for diode and error signal inputs
- Selectable servo error or servo diode inputs
- Focus and radial servo loops
- Automatic closed loop gain control available for focus and radial loops
- Built-in access procedure with fast track count input
- High-speed track crossing velocity measurement (>350 kHz) for CD and DVD
- Special DVD track crossing support
- Fast radial brake circuitry
- EFM actuator damping circuitry
- Sledge motor servo loop with enhanced Position Control Sledge (PCS) support
- Sledge stepper motor support
- Adaptive Repetitive Control (ARC)
- Debug interface for servo.

Clock multiplier

- On-chip clock multipliers allows the use of 8.4672 MHz crystal.

Disclaimer

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

GENERAL DESCRIPTION

The SAA7811 is a single-chip device for high speed DVD-ROM applications. The device contains the following blocks previously contained in separate ICs:

- channel decoder
- block decoder
- servo processor
- microcontroller.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DDD(CO)}$	supply voltage digital part core; note 1	3.0	3.3	3.6	V
$V_{DDD1(3P)}$	supply voltage digital part pad cells 3 V	3.0	3.3	3.6	V
$V_{DDD2(5P)}$	supply voltage digital part pad cells 5 V	4.5	5.0	5.5	V
V_{DDA}	supply voltage analog part; note 1	3.0	3.3	3.6	V
I_{DD}	supply current	–	tbf	–	mA
f_{XTAL}	crystal frequency	8	8.4672	35	MHz
T_{amb}	operating ambient temperature	0	–	60	°C
T_{stg}	storage temperature	–55	–	+125	°C

Note

1. The analog and digital core supply pins (V_{DDA} and $V_{DDD(CO)}$) must be connected to the same external supply.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7811HL	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1

BLOCK DIAGRAM

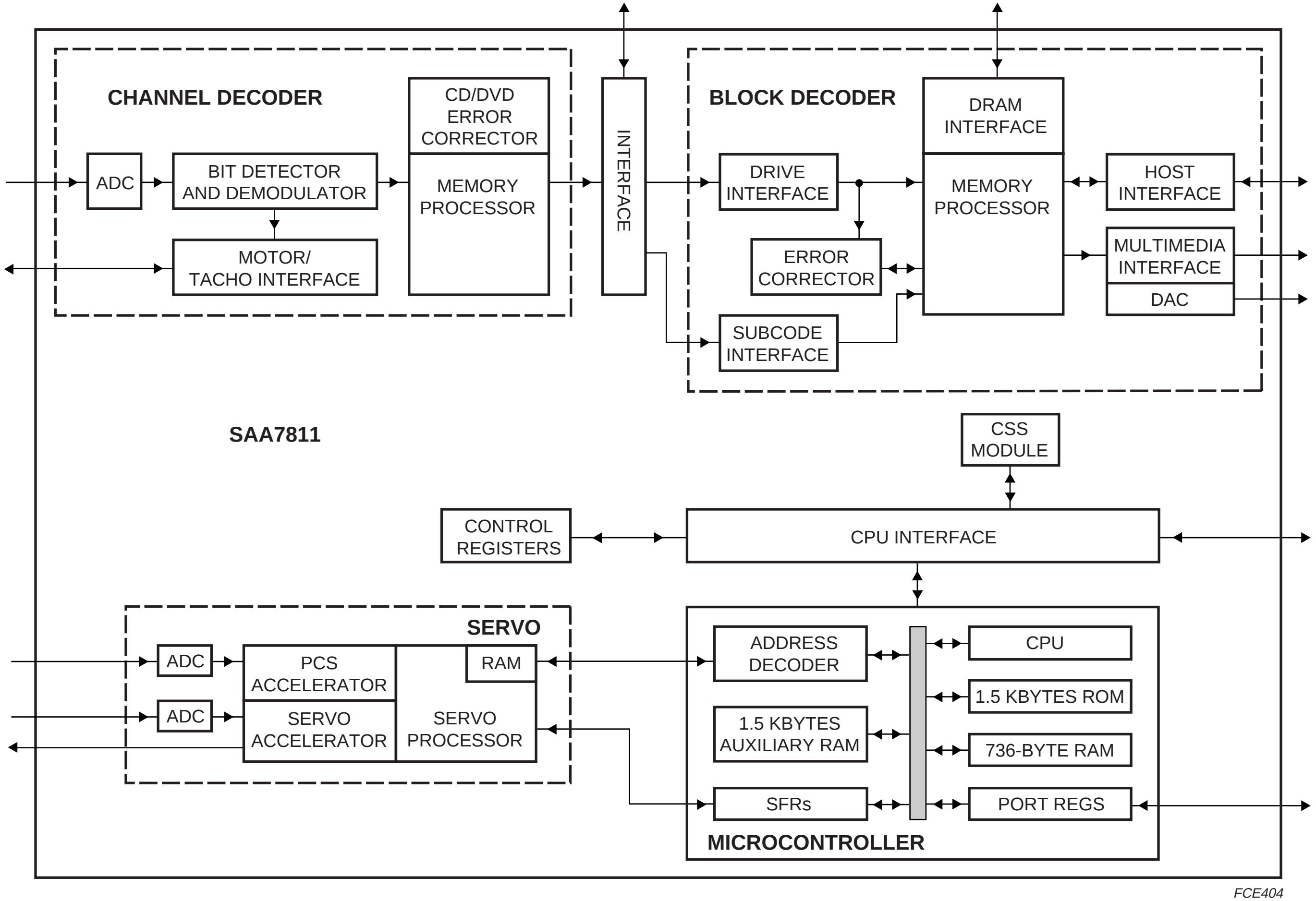


Fig.1 Block diagram.

PINNING

See note 1

SYMBOL	PIN	DESCRIPTION
$V_{DDD1(3P)}$	1	pad digital supply (3.3 V)
$V_{SSD1(3P)}$	2	pad digital ground (3.3 V)
T1	3	tacho 1 input, tcb_tck_pregate
T2	4	tacho 2 input
T3	5	tacho 3 input
DAC/RP	6	DAC differential output right (positive)/debug signal from MACE (opc_int)
DAC/RN	7	DAC differential output right (negative)/debug signal from MACE (servo_int)
DAC_VPOS	8	DAC V_{ref} (positive)
DAC_VNEG	9	DAC V_{ref} (negative)
DAC_LP	10	DAC differential output left (positive)/debug signal from MACE (dakota_int0)
DAC_LN	11	DAC differential output left (negative)/debug signal from MACE (dakota_int1)
TEST1	12	test input, tcb_tms and tcb_tdi connected to an internal pull-down resistor
TEST2	13	test input, tcb_trstn connected to an internal pull-down resistor
CRIN	14	clock input
CROUT	15	clock output
V_{DDA}	16	analog supply (3.3 V)
V_{SSA}	17	analog supply ground
HFIN_DN	18	differential HF in (negative)
HFIN_DP	19	differential HF in (positive)
HFIN_SE	20	single-ended HF in (AGC)
VCOM	21	common mode reference signal (DVDalas2plus)
I_{ref}	22	analog current reference
WREFLO	23	V_{ref} low; connect to V_{SSA} via capacitor
TEST3	24	test input; connect to V_{SSA}
V_{SSA}	25	analog supply ground
V_{DDA}	26	analog supply (3.3 V)
SIN_PHI	27	sine input from hall detectors
COS_PHI	28	cosine input from hall detectors
TEST4	29	test input; connect to V_{SSA}
XDET	30	auxiliary ADC input
ACT_EMFP	31	EMF of the actuator; positive input
ACT_EMFN	32	EMF of the actuator; negative input
TEST5	33	test input; connect to V_{SSA}
TEST6	34	test input; connect to V_{SSA}
TEST7	35	test input; connect to V_{SSA}
UOPB	36	decoupling point for ADC ladder
UOPT	37	upper reference voltage for ADC ladder
ALPHA0	38	gain control for TZA1030 (DROPPI)
V_{SSA}	39	analog supply ground

SYMBOL	PIN	DESCRIPTION
V_{DDA}	40	analog supply (3.3 V)
D1	41	diode input
D2/TLN	42	diode input (normalized); track-loss signal
D3/REN	43	diode input (normalized); radial error signal
D4/FEN	44	diode input (normalized); focus error signal
S1/MIRN	45	satellite diode (normalized); mirror signal
S2	46	satellite diode
VRIN	47	I/O voltage reference; for servo ADC
FTCH	48	track count input
P5_7/$\overline{DEFO}$	49	defect output (active LOW)/general purpose I/O
P5_6/$\overline{DEFI}$	50	defect input (active LOW)/general purpose I/O
P5_5/TL	51	track-loss means output/general purpose I/O
P5_4/RP/FOK	52	radial polarity/focus OK/general purpose I/O
P5_3/CE1	53	CS external SRAM/programmable I/O
P5_2/CLO	54	servo clock output/alpha0 step pulse for LADIC
P5/SDA	55	I^2C-bus data/general purpose I/O
P5_0/SCL	56	I^2C-bus clock/general purpose I/O
RA	57	radial output (3-state during reset)
SL	58	sledge output (3-state during reset)
FO	59	focus output (3-state during reset)
RAC_SW	60	disconnects radial actuator (active HIGH)
REF_SIN	61	pulse density modulated reference signal; removes DC offset from sin_phi
REF_COS	62	pulse density modulated reference signal; removes DC offset from cos_phi
$V_{DDD1(3P)}$	63	pad digital supply (3.3 V)
$V_{SSD1(3P)}$	64	pad digital ground (3.3 V)
P4_7/PXT2EN	65	timer 2 input enable/SIDA for DVDalas2plus
P4_6/PXT2	66	timer 2 clock input/SICL for DVDalas2plus
P4_5/PXT0	67	timer 1 clock input/SILD for DVDalas2plus
P4_4/PXT	68	timer 0 clock input/CS2 for external device
$V_{DDD(3CO)}$	69	core digital supply (3.3 V)
$V_{SSD(3CO)}$	70	core digital ground
P4_3/A19	71	A19 to EPROM
P4_2/A18	72	A18 to EPROM
P4_1/A17	73	A17 to EPROM
P4_0/A16	74	A16 to EPROM
UA15	75	port 2; upper microcontroller address lines
UA14	76	port 2; upper microcontroller address lines
UA13	77	port 2; upper microcontroller address lines
UA12	78	port 2; upper microcontroller address lines
UA11	79	port 2; upper microcontroller address lines
UA10	80	port 2; upper microcontroller address lines

SYMBOL	PIN	DESCRIPTION
UA9	81	port 2; upper microcontroller address lines
UA8	82	port 2; upper microcontroller address lines
$V_{DDD1(3P)}$	83	pad digital supply (3.3 V)
$V_{SSD1(3P)}$	84	pad digital ground (3.3 V)
$\overline{EA}$_$\overline{WAIT}$	85	address input/wait output internal pull-up resistor (active LOW)
DSDEN_SRST	86	microcontroller reset
SCCLK	87	microcontroller clock for testing
PSENN_CS	88	programme strobe enable/output enable for external device internal pull-up resistor
ALE_ASTB	89	address latch; chip select internal pull-up resistor
$V_{DDD(3CO)}$	90	core digital supply (3.3 V)
$V_{SSD(3CO)}$	91	core digital ground
UA7_P1_7	92	port 1; demultiplexed lower microcontroller address lines (mode3 = vampire7; V4)
UA6_P1_6	93	port 1; demultiplexed lower microcontroller address lines (mode3 = vampire6; SYNC)
UA5_P1_5	94	port 1; demultiplexed lower microcontroller address lines (mode3 = MON_D)
UA4_P1_4	95	port 1; demultiplexed lower microcontroller address lines (mode3 = MON_A)
UA3_P1_3	96	port 1; demultiplexed lower microcontroller address lines (mode3 = DEB_OUT)
UA2_P1_2	97	port 1; demultiplexed lower microcontroller address lines (mode3 = OTD)
UA1_P1_1	98	port 1; demultiplexed lower microcontroller address lines
UA0_P1_0	99	port 1; demultiplexed lower microcontroller address lines
$V_{DDD1(3P)}$	100	pad digital supply (3.3 V)
$V_{SSD1(3P)}$	101	pad digital ground (3.3 V)
UDA0	102	port 0; multiplexed microcontroller data/lower address lines
UDA1	103	port 0; multiplexed microcontroller data/lower address lines
UDA2	104	port 0; multiplexed microcontroller data/lower address lines
UDA3	105	port 0; multiplexed microcontroller data/lower address lines
UDA4	106	port 0; multiplexed microcontroller data/lower address lines
UDA5	107	port 0; multiplexed microcontroller data/lower address lines
UDA6	108	port 0; multiplexed microcontroller data/lower address lines
UDA7	109	port 0; multiplexed microcontroller data/lower address lines
P3_7/$\overline{RD}$	110	read signal (active LOW)
P3_6/$\overline{WR}$	111	write signal (active LOW)
P3_5/TXD2	112	UART 2 transmit data line
P3_4/RXD2	113	UART 2 receive data line
$V_{DDD1(3P)}$	114	pad digital supply (3.3 V)
$V_{SSD1(3P)}$	115	pad digital ground (3.3 V)
P3_3/INT1	116	interrupt 1 input/programmable I/O
P3_2/INT0	117	interrupt 0 input/programmable I/O
P3_1/TXD1	118	UART 1 transmit data line
P3_0/RXD1	119	UART 1 receive data line
HRESET	120	host reset
$V_{DDD2(5P)}$	121	pad digital supply (5.0 V)

SYMBOL	PIN	DESCRIPTION
$V_{SSD5(pad3)}$	122	pad digital ground (5.0 V)
DD7	123	host interface; generic DMA
DD8	124	host interface; generic DMA (mode1 = MEAS1_CFLG)
DD6	125	host interface; generic DMA
DD9	126	host interface; generic DMA (mode1 = MEAS1)
DD5	127	host interface; generic DMA
DD10	128	host interface; generic DMA (mode1 = MON_A)
DD4	129	host interface; generic DMA
DD11	130	host interface; generic DMA (mode1 = MON_D)
DD3	131	host interface; generic DMA
DD12	132	host interface; generic DMA (mode1 = DEB_OUT)
DD2	133	host interface; generic DMA
DD13	134	host interface; generic DMA (mode1 = OTD)
DD1	135	host interface; generic DMA
DD14	136	host interface; generic DMA
DD0	137	host interface; generic DMA
DD15	138	host interface; generic DMA
$V_{DDD2(5P)}$	139	pad digital supply (5.0 V)
$V_{SSD2(5P)}$	140	pad digital ground (5.0 V)
DMARQ/GACK	141	host DMA request; generic DMA acknowledge
DIOW	142	host interface write strobe
DIOR	143	host interface read strobe
IORDY	144	host interface ready
DMACK/GRQ	145	host DMA acknowledge; generic DMA request
INTRQ	146	host interface interrupt request
IOCS16	147	host interface $^{8}/_{16}$ bit port
DA1_GWR	148	host add bit 1; generic write
PDIAG	149	host interface passed test (mode1 = vampire6; SYNC)
DA0	150	host add bit 0
DA2_GRD	151	host add bit 2; generic read
$V_{DDD2(5P)}$	152	pad digital supply (5.0 V)
$V_{SSD2(5P)}$	153	pad digital ground (5.0 V)
CS0	154	host interface chip select 0
CS1	155	host interface chip select 1
DASP	156	host interface active slave present (mode1 = vampire7; V4)
$V_{DDD1(3P)}$	157	pad digital supply (3.3 V)
$V_{SSD1(3P)}$	158	pad digital ground (3.3 V)
XDA0	159	DRAM address
XDA1	160	DRAM address
XDA2	161	DRAM address
XDA3	162	DRAM address

SYMBOL	PIN	DESCRIPTION
XDA4	163	DRAM address
XDA5	164	DRAM address
XDA6	165	DRAM address
XDA7	166	DRAM address
XDA8	167	DRAM address
XDA9	168	DRAM address
$V_{DDD(3CO)}$	169	core digital supply (3.3 V)
$V_{SSD(3CO)}$	170	core digital ground
XRAS	171	DRAM RAS strobe
XCAS_HI	172	DRAM CAS strobe
XCAS_LO	173	DRAM CAS strobe
XWR	174	DRAM write strobe
$V_{DDD1(3P)}$	175	pad digital supply (3.3 V)
$V_{SSD1(3P)}$	176	pad digital ground (3.3 V)
XDD0	177	DRAM data bus
XDD1	178	DRAM data bus
XDD2	179	DRAM data bus
XDD3	180	DRAM data bus
XDD4	181	DRAM data bus
XDD5	182	DRAM data bus
XDD6	183	DRAM data bus
XDD7	184	DRAM data bus
XDD8	185	DRAM data bus
XDD9	186	DRAM data bus
XDD10	187	DRAM data bus
XDD11	188	DRAM data bus
XDD12	189	DRAM data bus
XDD13	190	DRAM data bus
XDD14	191	DRAM data bus
XDD15	192	DRAM data bus
$V_{SSD1(3P)}$	193	pad digital ground (3.3 V)
$V_{DDD1(3P)}$	194	pad digital supply (3.3 V)
IECO/CL1	195	IEC958 output/CL1 output from HDr62
MCK	196	multimedia master clock input/output (mode2 = MEAS_CFLG)
$V_{DDD(3CO)}$	197	core digital supply (3.3 V)
$V_{SSD(3CO)}$	198	core digital ground
WCLK_WSI	199	I^2C-bus word clock output/input (mode2 = MEAS1)
BCLK_SCKI	200	I^2C-bus bit clock output/input (mode2 = MON_D)
DATA_SDI	201	I^2C-bus data output/input (mode2 = MON_A)
FLAG	202	I^2C-bus flag output/input (mode2 = DEB_OUT)
TEST8	203	test output; leave unconnected

SYMBOL	PIN	DESCRIPTION
TEST9	204	test output; leave unconnected
TEST10	205	test output; leave unconnected
$\overline{\text{POR}}$	206	Power-on reset (active LOW)
BCA	207	BCA input
MOTO1	208	motor control output

Note

1. All supply pins must be connected to the same external power supply voltage.

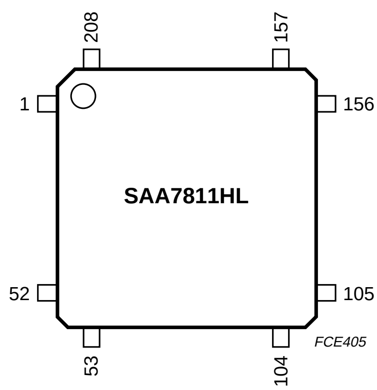


Fig.2 Pin configuration.

CHARACTERISTICS

$V_{DDD(3CO)}$ = 3.0 to 3.6 V; $V_{DDD1(3P)}$ = 3.0 to 3.6 V; V_{DDA} = 3.0 to 3.6 V; $V_{DDD2(5P)}$ = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = 0 to 60 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: HFIN_DN and HFIN_DP						
$f_{clk(sample)}$	clock frequency sample rate		–	–	140	MHz
B_{rec}	recovered bandwidth	⅓ Nyquist	–	46.6	–	MHz
$N_{bit(eff)}$	effective number of bits	$f_{clk(sample)}$ = 140 MHz	–	5	–	
$V_{i(dif)(p-p)}$	differential input signal voltage (peak-to-peak value)	0 dB; depends on V_{DDA}	–	1.4	$1.4V_{DDA}$	V
$V_{i(se)(p-p)}$	single-ended input signal voltage (peak-to-peak voltage)	0 dB; depends on V_{DDA}	–	0.7	$1.7V_{DDA}$	V
$V_{offset(dif)}$	differential offset voltage	V_{HFIN_DP}; V_{HFIN_DN}	–100	–	+100	mV
$V_{offset(cm)}$	common mode offset voltage		–200	–	+100	mV
$V_{offset(ADC)}$	ADC offset voltage		–60	–	+60	mV
C_i	static input capacitance	input to ground	–	7	–	pF
		input to input	–	3	–	pF
R_i	input resistance		–	∞	–	kΩ
$t_{d(g)}$	group delay		–	–	100	ps
Pin: HFIN_SE						
$f_{clk(sample)}$	clock frequency sample rate		–	–	–	MHz
B_{rec}	recovered bandwidth		–	35	–	MHz
G_{AGC}	AGC gain (32 steps)		–2.1	–	+11.4	dB
THD	total harmonic distortion	signal = 25 MHz; at V_{dif} = 1.4 V(p-p)	–	–	–35	dB
S/N	signal to noise ratio and distortion of AGC		–	50	–	dB
$V_{i(se)(p-p)}$	single-ended input signal voltage (peak-to-peak voltage)	0 dB; depends on V_{DDA}	–	0.7	$0.7V_{DDA}$	V
C_i	static input capacitance	input to ground	–	7	–	pF
R_i	input resistance		–	8.6	–	kΩ
$t_{d(g)}$	group delay flatness	0 to 35 MHz	–	–	600	ps
Pins: D1, D2/$\overline{TL}$, D3/$\overline{RE}$, S1/$\overline{MIR}$ and S2						
$I_{i/o(max)}$	maximum input/output current	selectable via gain; note 1	1	–	16	µA
V_i	voltage at input		–	V_{VRIN}	–	V
G_{tol}	gain tolerance		–20	0	+20	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG	variation of gain between channels (D1 to D2/$\overline{TL}$, D3/$\overline{RE}$ to D4/$\overline{FE}$ and S1/$\overline{MIR}$ to S2)		–2	–	+2	%
$C_{par(max)}$	maximum parasitic capacitance connected to input		–	–	25	pF
f_{clk}	clock frequency sample rate		–	8.4672	–	MHz
B_{rec}	recovered bandwidth		–	20	–	kHz
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	I_{sink} or I_{source} = 6 μA	–	–	–30	dB
DR	dynamic range	I_{sink} or I_{source} = 6 μA	50	–	–	dB
Pin: VRIN						
$V_{o(VRIN)}$	output voltage		0.75	0.9	1.05	V
$V_{i(VRIN)}$	input voltage		1.0	–	$\frac{1}{2}V_{DDA}$ + 0.1	V
Pin: FTCH						
$V_{(comp)(offset)(FTC)}$	comparator FTC offset voltage		–20	–	+20	mV
$V_{(comp)(hys)(FTC)}$	comparator FTC hysteresis voltage		–10	–	+10	mV
V_{cm}	common mode voltage		–	1.2	–	V
f_{sample}	sample rate		–	8.4672	–	MHz
C_i	input capacitance	input to ground	–	7	–	pF
R_i	input resistance		100	–	–	kΩ
Pins: UOPB and UOPT						
$V_{i(UOPB)}$	input voltage on UOPB		–	0	–	V
$V_{i(UOPT)}$	input voltage on UOPT		–	2.9	–	V
Pins: ACT_EMFP and ACT_EMFN						
V_i	input voltage		0	–	$V_{i(UOPT)}$	V
V_{cm}	common mode voltage		–	tbf	–	V
G	gain	note 2	–	5	–	V
B	bandwidth		–	265	–	kHz
R_i	input resistance		80	100	120	kΩ
C_i	static input capacitance		–	7	–	pF
Pins: SIN_PHI, COS_PHI, XDET and ACT_EMFP; note 3						
V_i	input voltage		0	–	$V_{(UOPT)}$	V
ΔG	gain matching between channels		–1	–	+1	%
R_i	input resistance		–	∞	–	kΩ
$C_{i(static)}$	static input capacitance		–	7	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_{i(dynamic)}$	dynamic input capacitance		–	5	–	pF
$f_{clk(sample)}$	clock frequency sample rate		–	1.05	–	MHz
B_{rec}	recovered bandwidth		5	–	–	kHz
$N_{bit(eff)}$	effective number of bits	at 1.05 MHz	–	7.2	–	
$CODE_{minvi}$	output code for $V_{i(UOPB)}$ input		0	5	10	
$CODE_{maxvi}$	output code for $V_{i(UOPT)}$ input		251	253	255	
Pin: ALPHA0						
f_{clk}	clock frequency sample rate		–	1.05	–	MHz
V_o	output voltage		0	–	$V_{i(UOPT)}$	V
C_L	load capacitance		–	–	25	pF
R_L	load resistance		10	–	30	kΩ
Pins: DAC_LN, DAC_LP, DAC/RN and DAC/RP						
f_{clk}	clock frequency sample rate		–	4.236	–	MHz
B	frequency bandwidth		–	–	20	kHz
S/N_{AW}	A-weighted signal-to-noise ratio	note 4	90	–	–	dB
THD	total harmonic distortion	note 4	–	–	–80	dB
Digital inputs						
$\overline{POR}$, HRESET AND BCA (SCHMITT TRIGGERS) TTL INPUT WITH HYSTERESIS						
$V_{sw(th)(r)}$	switching threshold voltage (rising)		1.4	–	1.9	V
$V_{sw(th)(f)}$	switching threshold voltage (falling)		0.9	–	1.45	V
V_{hys}	hysteresis voltage		0.4	–	0.7	V
C_I	input capacitance		–	–	10	pF
DESIGNATED BY ‘T’ TTL INPUT; note 5						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
I_{LI}	input leakage current	V_{LI} = 0 to $V_{DDD1(3P)}$	–10	–	+10	μA
C_i	input capacitance		–	–	10	pF
Digital outputs						
DESIGNATED BY ‘L’ (CMOS LEVELS)						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	$0.85V_{DDD1(3P)}$	–	–	V
C_L	load capacitance		–	–	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{o(r)}$	output rise time	C_L = 20 pF; 10% to 90% levels	–	–	20	ns
$t_{o(f)}$	output fall time	C_L = 20 pF; 90% to 10% levels	–	–	20	ns
DESIGNATED BY 'M' (CMOS LEVELS)						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	$0.85V_{DDD1(3P)}$	–	–	V
C_L	load capacitance		–	–	20	pF
$t_{o(r)}$	output rise time	C_L = 20 pF; 10% to 90% levels	–	–	20	ns
$t_{o(f)}$	output fall time	C_L = 20 pF; 90% to 10% levels	–	–	20	ns
$I_{L(3\text{-state})}$	3-state leakage current	V_{LI} = 0 to $V_{DDD1(3P)}$	–10	–	+10	μA
DESIGNATED BY 'AL' (ATA DATA BUS LEVELS)						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	$0.9V_{DDD2(5P)}$	–	–	V
C_L	load capacitance		–	–	100	pF
$t_{o(r)}$	output rise time	C_L = 100 pF; 0.5 V to 90% $V_{DDD2(5P)}$	5	–	–	ns
$t_{o(f)}$	output fall time	C_L = 100 pF; 90% $V_{DDD2(5P)}$ to 0.5 V	5	–	–	ns
DESIGNATED BY 'AH' (ATA LEVELS)						
V_{OL}	LOW-level output voltage	I_{OL} = 12 mA	–	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	$0.9V_{DDD2(5P)}$	–	–	V
C_L	load capacitance		–	–	100	pF
$t_{o(r)}$	output rise time	C_L = 100 pF; 0.5 V to 90% $V_{DDD2(5P)}$	5	–	–	ns
$t_{o(f)}$	output fall time	C_L = 100 pF; 90% $V_{DDD2(5P)}$ to 0.5 V	5	–	–	ns
Input: CRIN (external clock)						
V_{IL}	LOW-level input voltage		–0.3	–	+0.5	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDA} + 0.3	V
t_{IH}	input HIGH time	relative to period	45	–	55	%
I_{LI}	input leakage current		–10	–	+10	μA
C_i	input capacitance		–	–	7	pF
Output: CROUT						
f_{XTAL}	crystal frequency	note 6	–	8.4672	–	MHz
$g_{m(mutual)}$	mutual conductance at start-up		–	17	–	mA/V

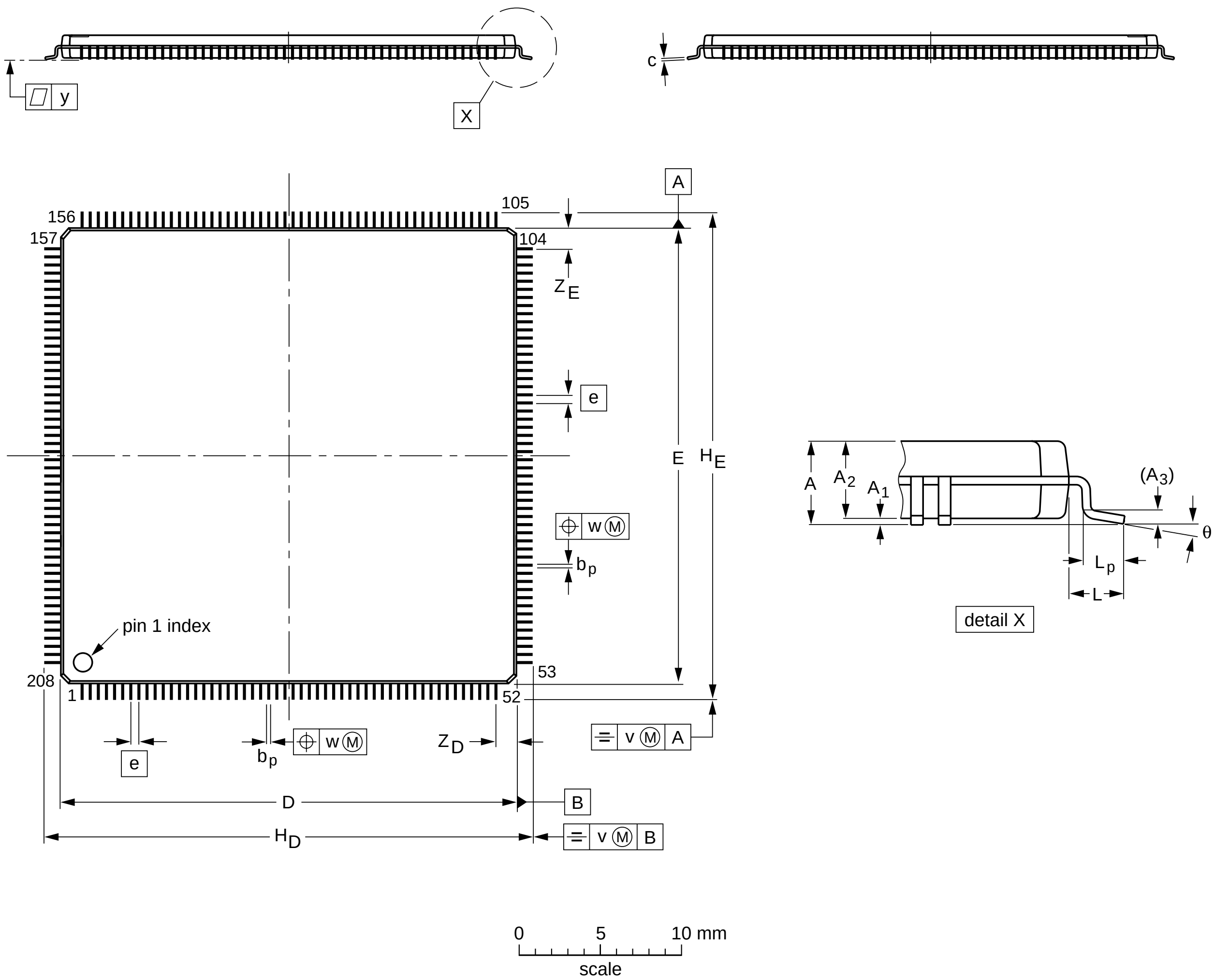
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_{(feedback)}$	feedback capacitance		–	–	2	pF
C_o	output capacitance		–	–	7	pF
R_{bias}	internal bias resistor		–	200	–	kΩ

Notes

1. Clips at maximum gain setting; input can handle two times the maximum signal amplitude.
2. Gain depends on application components.
3. Pin ACT_EMFP operating in bypass mode.
4. Performance largely determined by application circuit.
5. Does not apply to pins $\overline{EA}$_$\overline{WAIT}$, PSENN_CS and ALE_ASTB as they have internal pull-up resistors.
6. It is recommended that the nominal running series resistance of the crystal or ceramic resonator is ≤ 60 Ω.

PACKAGE OUTLINE

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1.0	0.75 0.45	0.12	0.15	0.1	1.43 1.08	1.43 1.08	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT459-1						~~97-10-02~~ 98-06-17

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	**REFLOW**(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
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