GENERAL

QUALITY

Total Quality Management

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system which is described in our Quality manuals. The basis is outlined in the following paragraphs.

QUALITY ASSURANCE

Based on ISO 9000 standards, customer standards such as FDC, QS 9000 and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

PARTNERSHIPS WITH CUSTOMERS

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

PARTNERSHIPS WITH SUPPLIERS

Ship-to-stock, statistical process control and ISO 9000 audits.

QUALITY IMPROVEMENT PROGRAMME

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical process parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase in preparation for production under statistical process control.

Product conformance

The assurance of product conformance is an integral part of our Quality Assurance (QA) practice. This is achieved by:

- Incoming material control through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Process steps are under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications SNW-EQ-611 part A.
- Periodic inspections to monitor and measure the conformance of products (see SNW-EQ-611 part A).
- Qualification tests (see SNW-EQ-611 part A).

Product reliability

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the product's reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer response

Our quality improvement depends on working together with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

PRO ELECTRON TYPE NUMBERING SYSTEM

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A Germanium or other material with a band gap of 0.6 to 1 eV

B Silicon or other material with a band gap of 1 to 1.3 eV

C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb}$ > 15 K/W and power types by $R_{th\ j\text{-}mb} \leq$ 15 K/W.

A Diode; signal, low power

B Diode; variable capacitance

C Transistor; low power, audio frequency

D Transistor; power, audio frequency

E Diode; tunnel

F Transistor; low power, high frequency

G Multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter; see under Section “Serial number”.

H Diode; magnetic sensitive

L Transistor; power, high frequency

N Photocoupler

P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q Radiation generator; e.g. LED, laser; with special third letter

R Control or switching device; e.g. thyristor, low power; with special third letter

S Transistor; low power, switching

T Control or switching device; e.g. thyristor, power; with special third letter

U Transistor; power, switching

W Surface acoustic wave device

X Diode; multiplier, e.g. varactor, step recovery

Y Diode; rectifying, booster

Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1)

Version letter

A letter may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS

The letter symbols for transistors detailed in this section are based on IEC publication number 148.

Letter symbols for currents, voltages and powers

BASIC LETTERS

I, i current

V, v voltage

P, p power.

Upper-case letter symbols are used to represent all values except instantaneous values that vary with time, these are represented by lower-case letters.

SUBSCRIPTS

A, a	anode terminal
(AV), (av)	average value
B, b	base terminal
C, c	collector terminal
D, d	drain terminal
E, e	emitter terminal
F, f	forward
G, g	gate terminal
K, k	cathode terminal
M, m	peak value
O, o	as third subscript: the terminal not mentioned is open-circuit
R, r	as first subscript: reverse. As second subscript: repetitive. As third subscript: with a specified resistance between the terminal not mentioned and the reference terminal

(RMS), (rms)	root-mean-square value
S, s	as first or second subscript: source terminal (FETs only). As second subscript: non-repetitive (not FETs). As third subscript: short circuit between the terminal not mentioned and the reference terminal
X, x	specified circuit
Z, z	replaces R to indicate the actual working voltage, current or power of voltage reference and voltage reference diodes.

No additional subscript is used for DC values.

Upper-case subscripts are used for the indication of:

- Continuous (DC) values (without signal), e.g. I_B
- Instantaneous total values, e.g. i_B
- Average total values, e.g. $I_{B(AV)}$
- Peak total values, e.g. I_{BM}
- Root-mean-square total values, e.g. $I_{B(RMS)}$.

Lower-case subscripts are used for the indication of values applying to the varying component alone:

- Instantaneous values, e.g. i_b
- Root-mean-square values, e.g. $I_{b(rms)}$
- Peak values, e.g. I_{bm}
- Average values, e.g. $I_{b(av)}$.

If more than one subscript is used, the subscript for which both styles exist are either all upper-case or all lower-case.

ADDITIONAL RULES FOR SUBSCRIPTS

Transistor currents

If it is necessary to indicate the terminal carrying the current, this should be done by the first subscript (conventional current flow from the external circuit into the terminal is positive).

Examples: I_B, i_B, i_b, I_{bm}.

Transistor voltages

If it is necessary to indicate the points between which a voltage is measured, this should be done by the first two subscripts. The first subscript indicates the terminal at which the voltage is measured and the second the reference terminal or the circuit node. Where there is no possibility of confusion, the second subscript may be omitted.

Examples: V_{BE}, v_{BE}, v_{be}, V_{bem}.

Supply voltages or currents

Supply voltages or supply currents are indicated by repeating the appropriate terminal subscript.

Examples: V_{CC}, I_{EE}.

If it is necessary to indicate a reference terminal, this should be done by a third subscript.

Example: V_{CCE}.

Subscripts for devices with more than one terminal of the same kind

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal, followed by a number. In the case of multiple subscripts, hyphens may be necessary to avoid confusion.

Examples:

I_{B2}	continuous (DC) current flowing into the second base terminal
$V_{B2\text{-}E}$	continuous (DC) voltage between the terminals of second base and emitter terminals.

Subscripts for multiple devices

For multiple unit devices, the subscripts are modified by a number preceding the letter subscript. In the case of multiple subscripts, hyphens may be necessary to avoid confusion.

Examples:

I_{2C}	continuous (DC) current flowing into the collector terminal of the second unit
$V_{1C\text{-}2C}$	continuous (DC) voltage between the collector terminals of the first and second units.

Application of the rules

Figure 1 represents a transistor collector current as a function of time. It comprises a continuous (DC) current and a varying component.

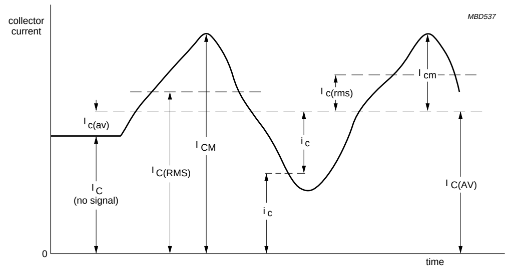


Fig.1 Collector current as a function of time.

Letter symbols for electrical parameters

DEFINITION

For the purpose of this publication, the term 'electrical parameter' applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

BASIC LETTERS

The following list comprises the most important basic letters used for electrical parameters of semiconductor devices.

B, b	susceptance (imaginary part of an admittance)
C	capacitance
G, g	conductance (real part of an admittance)
H, h	hybrid parameter
L	inductance
R, r	resistance (real part of an impedance)
X, x	reactance (imaginary part of an impedance)
Y, y	admittance
Z, z	impedance.

Upper-case letters are used for the representation of:

- Electrical parameters of external circuits and of circuits in which the device forms only a part
- All inductances and capacitances.

Lower-case letters are used for the representation of electrical parameters inherent in the device, with the exception of inductances and capacitances.

SUBSCRIPTS

General subscripts

The following list comprises the most important general subscripts used for electrical parameters of semiconductor devices.

F, f	forward (forward transfer)
I, i (or 1)	input
L, l	load
O, o (or 2)	output
R, r	reverse (reverse transfer)
S, s	source.

Examples: Z_s, h_f, h_F.

The upper-case variant of a subscript is used for the designation of static (DC) values.

Examples:

h_{FE}	static value of forward current transfer ratio in common-emitter configuration (DC current gain)
R_E	DC value of the external emitter resistance.

The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript is used for the designation of small-signal values.

Examples:

h_{fe}	small-signal value of the short-circuit forward current transfer ratio in common-emitter configuration
$Z_e = R_e + jX_e$	small-signal value of the external impedance.

If more than one subscript is used, subscripts for which both styles exist are either all upper-case or all lower-case.

Examples: h_{FE}, y_{RE}, h_{fe}.

Subscripts for four-pole matrix parameters

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer.

Examples: h_i (or h_{11}), h_o (or h_{22}), h_f (or h_{21}), h_r (or h_{12}).

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples: h_{fe} (or h_{21e}), h_{FE} (or h_{21E}).

DISTINCTION BETWEEN REAL AND IMAGINARY PARTS

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts should be used. If basic symbols for the real and imaginary parts exist, these may be used.

Examples: $Z_i = R_i + jX_i$, $y_{fe} = g_{fe} + jb_{fe}$.

If such symbols do not exist, or if they are not suitable, the following notation is used:

Examples:

Re (h_{ib}) etc. for the real part of h_{ib}

Im (h_{ib}) etc. for the imaginary part of h_{ib}.

S-PARAMETER DEFINITIONS

S-parameters S_{11} and S_{22} (return losses)

In accordance with IEC 747-7.

DEFINITION

The return losses or reflection coefficients of a module can be defined as the S_{11} and the S_{22} of a two-port network (see Fig.2).

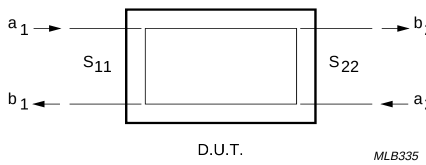


Fig.2 Two-port network with reflection coefficients S_{11} and S_{22}.

$$b_1 = S_{11} \cdot a_1 + S_{12} \cdot a_2 \quad (1)$$

$$b_2 = S_{21} \cdot a_1 + S_{22} \cdot a_2 \quad (2)$$

where:

$$a_1 = \frac{1}{2 \cdot \sqrt{Z_0}} \cdot (V_1 + Z_0 \cdot i_1) = \text{signal into port 1} \quad (3)$$

$$a_2 = \frac{1}{2 \cdot \sqrt{Z_0}} \cdot (V_2 + Z_0 \cdot i_2) = \text{signal into port 2} \quad (4)$$

$$b_1 = \frac{1}{2 \cdot \sqrt{Z_0}} \cdot (V_1 + Z_0 \cdot i_1) = \text{signal out of port 1}$$

$$b_2 = \frac{1}{2 \cdot \sqrt{Z_0}} \cdot (V_2 + Z_0 \cdot i_2) = \text{signal out of port 2}$$

From (1) and (2) formulae for the return losses can be derived:

$$S_{11} = \left.\frac{b_1}{a_1}\right| a_2 = 0 \quad (5)$$

$$S_{22} = \left.\frac{b_2}{a_2}\right| a_1 = 0 \quad (6)$$

In (5), $a_2 = 0$ means output port terminated with Z_0 (derived from formula (4)).

In (6), $a_1 = 0$ means input port terminated with Z_0 (derived from formula (3)).

MEASUREMENT

The return losses are measured with a network analyzer after calibration, where the influence of the test jig is eliminated. The necessary termination of the other port with Z_0 is done automatically by the network analyzer.

The network analyser must have a directivity of at least 40 dB to obtain an accuracy of 0.5 dB when measuring return loss figures of 20 dB. A full two-port correction method can be used to improve the accuracy.

Spice parameter data

Spice parameters are included with this data handbook on floppy disks labelled “Philips simulation data selection program for LF small-signal transistors”.

EQUIVALENT PACKAGE DESIGNATORS

Philips designator	Industry designator	Philips designator	Industry designator
Leaded metal can		**Surface-mount plastic**	
SOT5/11	TO-39	SOT23	SOT23
SOT18/9	TO-72	SOT89	SOT89
SOT18/13	TO-18	SOT143	SOT143
SOT31	TO-71	SOT223	SOT223
Leaded plastic		SOT323	SC-70
SOT32	TO-126	SOT346	SC-59
SOT54	TO-92	SOT363	SC-88
SOT128	TO-202	SOT416	SC-75

TRANSISTOR RATINGS

Voltage ratings

COLLECTOR TO BASE

V_{CBmax} The maximum permissible instantaneous voltage between collector and base terminals. The collector voltage is negative with respect to base in pnp transistors and positive with respect to base in npn types.

V_{CBmax} ($I_E = 0$) The maximum permissible instantaneous voltage between collector and base terminals when the emitter terminal is open-circuit.

EMITTER TO BASE

V_{EBmax} The maximum permissible instantaneous voltage between emitter and base terminals. The emitter voltage is negative with respect to base in pnp transistors and positive with respect to base in npn types.

V_{EBmax} ($I_C = 0$) The maximum permissible instantaneous voltage between emitter and base terminals when the collector terminal is open-circuit.

COLLECTOR TO EMITTER

V_{CEmax} The maximum permissible instantaneous voltage between collector and emitter terminals. The collector voltage is negative with respect to emitter in pnp transistors and positive with respect to emitter in npn types. This rating is very dependent on circuit conditions and collector current, and it is necessary to refer to the curve of V_{CE} versus I_C for the appropriate circuit condition in order to obtain the correct rating.

V_{CEmax} (Cut-off) The maximum permissible instantaneous voltage between collector and emitter terminals when the emitter current is reduced to zero by means of a reverse emitter base voltage, i.e. the base voltage is normally positive with respect to emitter for pnp transistors and negative with respect to emitter for npn types. The term ‘(Cut-off)’ is sometimes replaced by V_{BE} > x V, or $R_B/R_E \leq$ y, which are equivalent conditions under which the transistor may be cut off.

V_{CEmax} (I_C = x mA) The maximum permissible instantaneous voltage between collector and emitter terminals when the collector current is at a high value, often the maximum rated value.

V_{CEmax} ($I_B = 0$) The maximum permissible instantaneous voltage between collector and emitter terminals when the base terminal is open-circuit or when a very high resistance is in series with the base terminal. Special care must be taken to ensure that thermal runaway due to excessive collector leakage current does not occur in this condition.

Due to the current dependency of V_{CE} it is usual to present this information as a voltage rating chart, a curve of collector current as a function of collector-to-emitter voltage (see Fig.3). The permissible area of operation under all conditions of base drive (provided the dissipation rating is not exceeded) is shown as area 1 and operation under certain specified conditions is shown as area 2.

To assist in determining the rating in area 2, further curves can relate the voltage rating to external circuit conditions, for example: R_B/R_E, R_B, Z_{Bg}, V_{BE}, I_B or V_{BB}/R_B. An example of this type of curve is given in Fig.4 with V_{CE} as a function of R_B/R_E for two values of collector current.

It should be noted that when R_E is shunted by a capacitor, during switching, the collector voltage V_{CE} must be restricted to a value that does not rely on the effect of R_E.

In the case of an inductive load, when an energy rating is given, it may be safe to operate outside the rated area provided the specified energy rating is not exceeded.

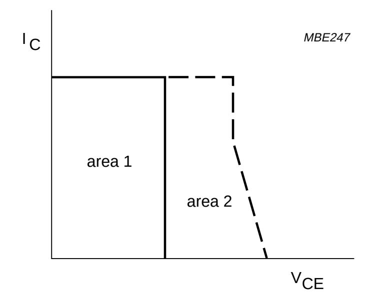


Fig.3 Graph of permissible operating areas.

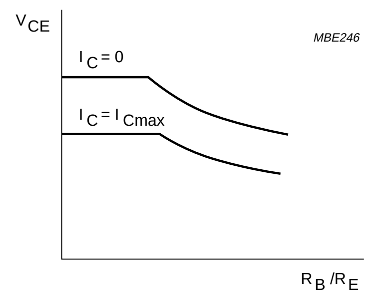


Fig.4 Graph showing effect of collector current on permissible operating areas.

Current ratings

COLLECTOR

I_{Cmax} The maximum permissible collector current. Without further qualification, the DC value is implied.

$I_{C(AV)max}$ The maximum permissible average value of the total collector current.

I_{CM} The maximum permissible instantaneous value of the total collector current.

Emitter

I_{Emax} The maximum permissible emitter current. Without further qualification, the DC value is implied.

$I_{E(AV)max}$ The maximum permissible average value of the total emitter current.

$I_{ER(AV)max}$ The maximum permissible average value of the total emitter current when operating in the reverse emitter-base breakdown region.

I_{EM} The maximum permissible instantaneous value of the total emitter current.

I_{ERM} The maximum permissible instantaneous value of the total emitter current when operating in the reverse breakdown region.

BASE

I_{Bmax} The maximum permissible base current. Without further qualification, the DC value is implied.

$I_{B(AV)max}$ The maximum permissible average value of the total base current.

$I_{BR(AV)max}$ The maximum permissible average value of the total base current when operating in the reverse breakdown region.

I_{BM} The maximum permissible instantaneous value of the total base current. The rating also includes the switch-off current.

I_{BRM} The maximum permissible instantaneous value of the total reverse current allowable in the reverse breakdown region.

Power ratings

The total maximum permissible continuous power dissipation in the transistor, $P_{tot\ max}$, includes collector-base dissipation and emitter-base dissipation. Under steady state conditions, the total power is given as:

$P_{tot} = V_{CE} \times I_C + V_{BE} \times I_B$.

In order to distinguish between ‘steady state’ and ‘pulse’ conditions, the terms ‘steady state power (P_S)’ and ‘pulse power (P_P)’ can be used. The permissible total power dissipation is dependent on temperature; this relationship is shown in Fig.5.

The temperature may be the ambient, the case or the mounting base temperature. Where a cooling clip or heatsink is attached to the device, the allowable power dissipation is also dependent on the efficiency of the heatsink.

The efficiency of this clip or heatsink is measured in terms of its thermal resistance ($R_{th\ h}$) normally expressed in degrees Kelvin per Watt (K/W). For mounting-base rated devices, the added effect of the contact resistance ($R_{th\ i}$) must be taken into account.

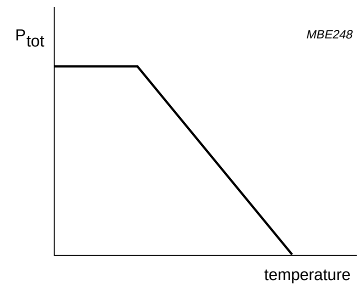


Fig.5 Permissible total power dissipation.

The effect of heatsinks of various thermal and contact resistance is often included in the graph of permissible total power dissipation.

The relationship between maximum power dissipation, ambient temperature and thermal heatsink resistance is given by:

$$P_{tot} = \frac{T_j - T_{amb}}{R_{th\,j-a}}$$

where $R_{th\,j\text{-}a}$ is the thermal resistance from the transistor junction to the ambient. For case rated or mounting-base rated devices, the thermal resistance $R_{th\,j}$ is made up of the thermal resistance junction to case or mounting-base ($R_{th\,j\text{-}mb}$), the contact thermal resistance ($R_{th\,i}$) and the heatsink thermal resistance ($R_{th\,h}$).

For the calculation of pulse power operation, the maximum pulse power is obtained using a graph as shown in Fig.6

The general expression from which the maximum pulse power dissipation can be calculated is:

$$P_p = \frac{T_j - T_{amb} - P_S \times R_{th\,j-a}}{Z_{in\,t} + d\,(R_{th\,c-a})}$$

where $Z_{th\,t}$ and δ are given in Fig.6 and $R_{th\,c-a}$ is the thermal resistance between case and ambient for a case rated device. For a mounting-base rated device, it is equal to $R_{th\,h}$ + $R_{th\,i}$ and is zero for a free-air rated device because the effect of the temperature rise of the case over the ambient for a pulse train is already included in $Z_{th\,t}$.

Temperature ratings

$T_{j\,max}$ The maximum permissible junction temperature which is used as the basis for the calculation of power ratings. Unless otherwise stated, the continuous value is implied.

$T_{j\,max}$ (continuous operation): indicates the maximum permissible continuous value.

$T_{j\,max}$ (intermittent operation): indicates the maximum permissible instantaneous junction temperature usually allowed for a total duration of 200 hours.

T_{mb} The temperature of the surface in contact with the heatsink. This is confined to devices where a flange or stud for fixing onto a heatsink forms an integral part of the package.

T_{case} The temperature of the package. This is confined to devices that may have a clip-on cooling fin attachment.

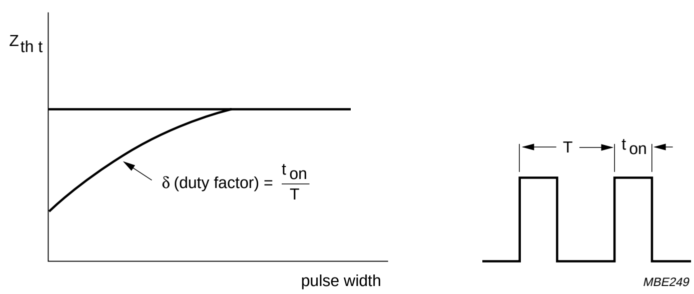


Fig.6 Pulse power operation.

THERMAL CONSIDERATIONS

Thermal resistance

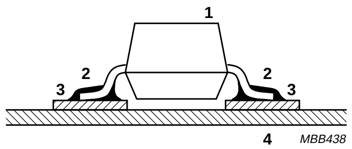
Circuit performance and long-term reliability are affected by the temperature of the transistor die. Normally, both are improved by keeping the die temperature (junction temperature) low.

Electrical power dissipated in any semiconductor device is a source of heat. This increases the temperature of the die about some reference point, normally an ambient temperature of 25 ºC in still air. The size of the increase in temperature depends on the amount of power dissipated in the circuit and the net thermal resistance between the heat source and the reference point.

Devices lose most of their heat by conduction when mounted on a printed board, a substrate or heatsink. Referring to Fig.7 (for surface mounted devices mounted on a substrate), heat conducts from its source (the junction) via the package leads and soldered connections to the substrate. Some heat radiates from the package into the surrounding air where it is dispersed by convection or by forced cooling air. Heat that radiates from the substrate is dispersed in the same way.

The elements of thermal resistance shown in Fig.8 are defined as follows:

- $R_{th\ j\text{-}mb}$ thermal resistance from junction to mounting base
- $R_{th\ j\text{-}c}$ thermal resistance from junction to case
- $R_{th\ j\text{-}s}$ thermal resistance from junction to soldering point
- $R_{th\ s\text{-}a}$ thermal resistance from soldering point to ambient
- $R_{th\ c\text{-}a}$ thermal resistance from case to ambient ($R_{th\ s\text{-}a}$ and $R_{th\ c\text{-}a}$ are the same for most packages)
- $R_{th\ j\text{-}a}$ thermal resistance from junction to ambient.



Heat radiates from the package (1) to ambient.
Heat conducts via leads (2), solder joints (3) to the substrate (4).

Fig.7 Heat losses.

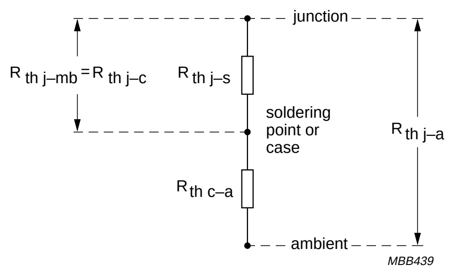


Fig.8 Representation of thermal resistance paths of a device mounted on a substrate or printed board.

The temperature at the junction depends on the ability of the package and its mounting to transfer heat from the junction region to the ambient environment. The basic relationship between junction temperature and power dissipation is:

$T_{j\,max} = T_{amb} + P_{tot\,max}\,(R_{th\,j\text{-}s} + R_{th\,s\text{-}a})$
$= T_{amb} + P_{tot\,max}\,(R_{th\,j\text{-}a})$

where

$T_{j\,max}$ is the maximum junction temperature

T_{amb} is the ambient temperature

$P_{tot\,max}$ is the maximum power handling capability of the device, including the effects of external loads when applicable.

In the expression for $T_{j\,max}$, only T_{amb} and $R_{th\,s\text{-}a}$ can be varied by the user. The package mounting technique and the flow of cooling air are factors that affect $R_{th\,s\text{-}a}$. The device power dissipation can be controlled to a limited extent but under recommended usage, the supply voltage and circuit loading dictate a fixed power maximum. The $R_{th\,j\text{-}s}$ value is essentially independent of external mounting method and cooling air; but is sensitive to the materials used in the package construction, the die bonding method and the die area, all of which are fixed.

Values of $T_{j\,max}$ and $R_{th\,j\text{-}s}$, or $R_{th\,j\text{-}c}$ or $R_{th\,j\text{-}a}$ are given in the device data sheets. For applications where the temperature of the case is stabilized by a large or temperature-controlled heatsink, the junction temperature can be calculated from:

$T_j = T_{case} + P_{tot} \times R_{th\,j\text{-}c}$ or, using the soldering point definition, from $T_j = T_{solder} + P_{tot} \times R_{th\,j\text{-}s}$.

$R_{th\,s\text{-}a}$ for SMDs

The thermal resistance $R_{th\,s\text{-}a}$ for SMDs mounted on a ceramic substrate (Al_2O_3) is a function of the substrate area as shown in Fig.9.

The thermal resistance $R_{th\,s\text{-}a}$ for SMDs mounted on a printed circuit board (FR4) is a function of the board type (single-sided or double-sided), track area and plated or unplated tracks as shown in Fig.10.

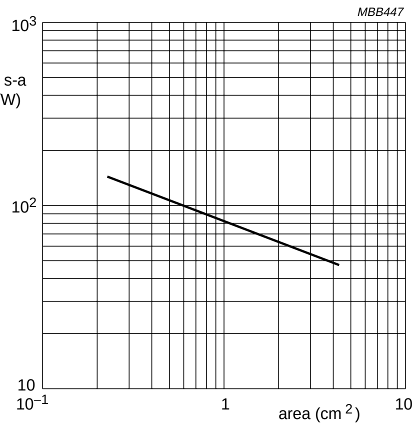
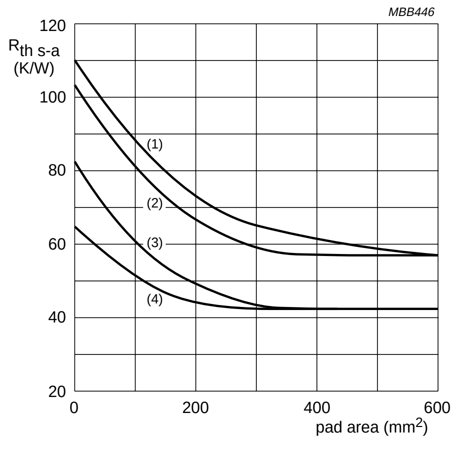


Fig.9 Thermal resistance ($R_{th\,s\text{-}a}$) as a function of area of ceramic substrate.



(1) Single-sided, unplated.
(2) Single-sided, plated.
(3) Double-sided, unplated.
(4) Double-sided, plated.

Fig.10 Thermal resistance ($R_{th\,s\text{-}a}$) as a function of copper area on different configurations of FR4 epoxy fibre-glass circuit board.

Temperature calculation under pulsed conditions

In pulsed power conditions, the peak temperature of the die depends on the pulse time and duty factor as well as the ability of the package and its mounting to disperse heat.

When power is applied in repetitive square-wave pulses with a certain duty factor (δ), the variation in junction temperature has a sawtooth characteristic.

The average steady-state junction temperature is:

$T_{j(av)} = T_{ref} + \delta \times P_d \times R_{th\ j\text{-}ref}$

The peak junction temperature, however, is the most relevant to performance reliability. This can be calculated by heating and cooling step functions that result in heating and cooling curves shifted in time as shown in Fig.11.

The peak value of T_j is reached at the end of a power pulse and the minimum value immediately before the next power pulse. The thermal ripple is the difference between $T_{j(peak)}$ and $T_{j(min)}$.

Calculation of $T_{j(peak)}$ after n pulses:

$$T_{j(peak)} = T_{ref} + P_d \times \sum_{a=0}^{a=n-1} [Z_{th(at+w)} - Z_{th(at)}]$$

where a is an integer number.

Approximation method of finding $T_{j(peak)}$

With this method it is assumed that the average load is immediately followed by two square power pulses as shown in Fig.12. This two-pulse approximation method is accurate enough for finding $T_{j(peak)}$.

The junction temperature at the end of the second pulse is:

$$T_{j(peak)} = T_{ref} + P_d \times [\delta \times R_{th(j\text{-}ref)} + (1 - \delta) \times Z_{th(t+w)} + Z_{th(w)} - Z_{th(t)}]$$

The junction temperature immediately before the second power pulse is:

$$T_{j(min)} = T_{ref} + P_d \times [\delta \times R_{th(j\text{-}ref)} + (1 - \delta) \times Z_{th(t)} - Z_{th(t-w)}]$$

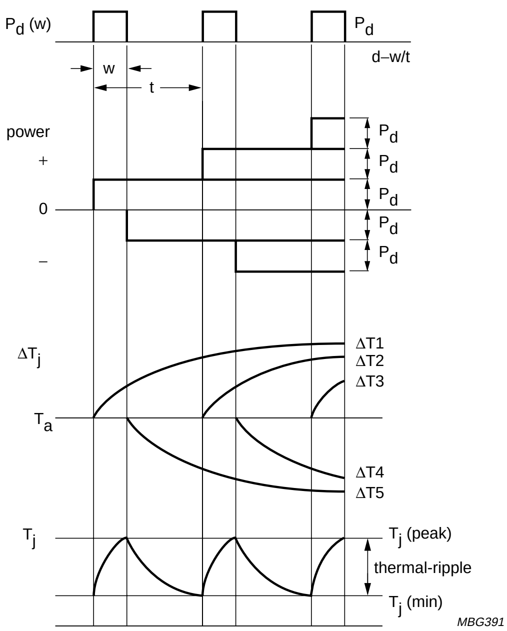


Fig.11 Heating effect of three identical power pulses after thermal stabilization.

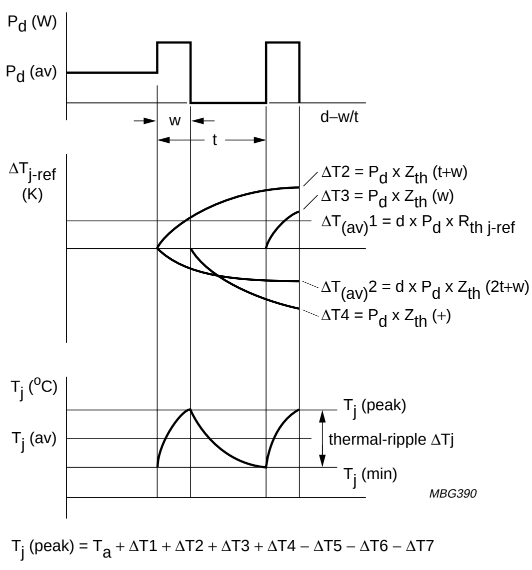


Fig.12 Two-pulse approximation method of finding peak steady-state junction temperature [$T_{j(peak)}$].

The thermal ripple is:

$\Delta T_j = T_{j(peak)} - T_{j(min)}$

$\Delta T_j = P_d \times [\delta \times (Z_{th(t)} - Z_{th(t+w)}) - 2 \times Z_{th(t)} + Z_{th(w)} + Z_{th(t-w)}]$

Reducing calculation time

To be able to point out the junction peak temperature at a certain pulse time and duty cycle, a graph similar to that shown in Fig.13 is included in relevant data sheets. In this example, the curves have been derived using the formula $T_{j(peak)} = T_{ref} + P_d \times [\delta \times R_{th(j\text{-}ref)} + (1 - \delta) \times Z_{th(t+w)} + Z_{th(w)} - Z_{th(t)}]$, with typical values inserted.

The pulse width along the X-axis meets a particular duty cycle curve, indicating the Z_{th} value in K/W along the Y-axis.

$T_{j(peak)} = P_{d(peak)} \times Z_{th(j\text{-}s)} + P_{d(av)} \times R_{th(s\text{-}a)} + T_a$ (°C)

Soldering point temperature provides a better reference point than ambient temperature as this is subject to many uncontrolled variables. Therefore, the thermal resistance from junction to soldering point [$R_{th(j\text{-}s)}$] is becoming a more relevant measurement path.

For transistors in small SMD packages which are usually mounted on FR4 epoxy fibre-glass printed circuit boards, only the thermal resistance from junction to ambient [$R_{th(j\text{-}a)}$] is published. In this case, the junction temperature can be calculated by:

$T_{j(peak)} = P_{d(peak)} \times Z_{th(j\text{-}a)} + T_a$ (°C)

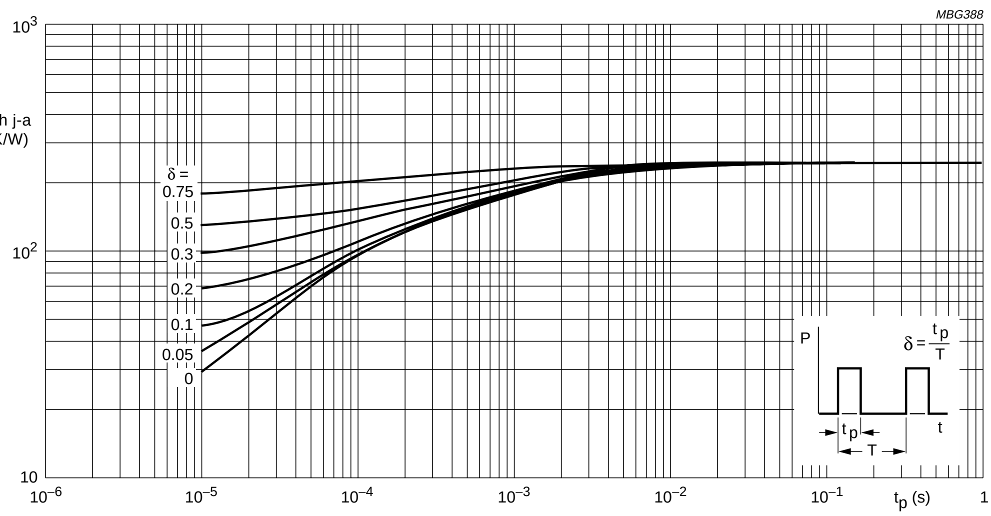


Fig.13 Direct reading of thermal impedance from junction to soldering point for calculation of junction temperature at pulsed power conditions.

POWER DERATING CURVES FOR SMDs

Figures 14 through 32 on the following pages show the power derating curves (P_{tot} versus T_{amb}) for transistors in SMD packages.

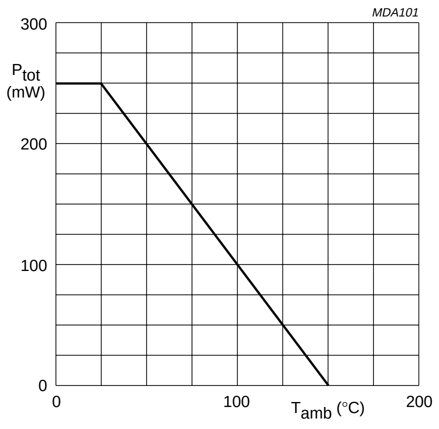


Fig.14 Power derating curve for SOT23.

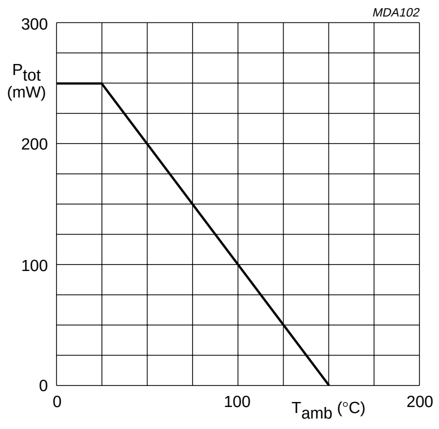


Fig.15 Power derating curve for SOT143.

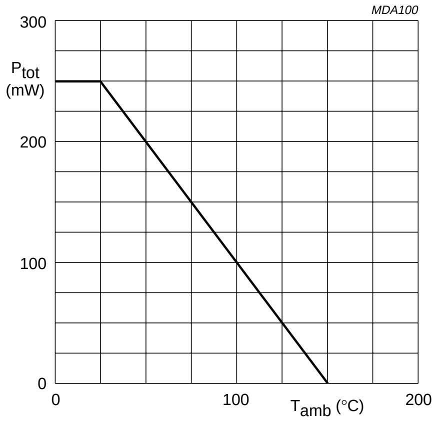


Fig.16 Power derating curve for SC-59 (SOT346).

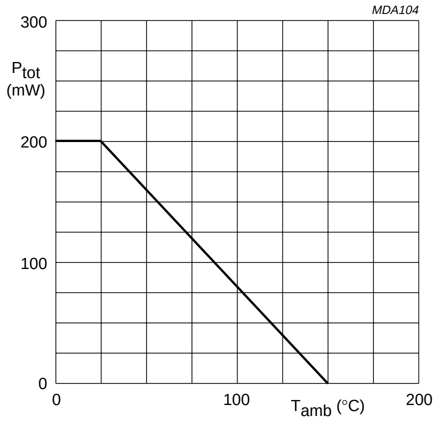
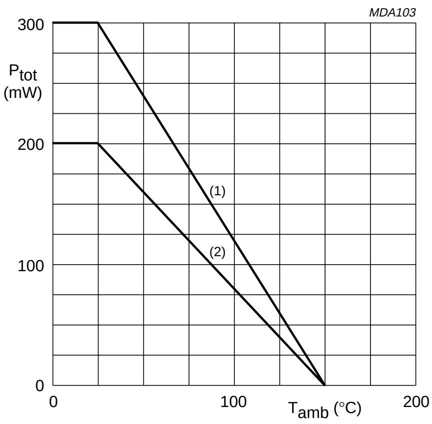


Fig.17 Power derating curve for SC-70 (SOT323).



(1) All transistors used.
(2) One transistor used.

Fig.18 Power derating curves for SC-88 (SOT363).

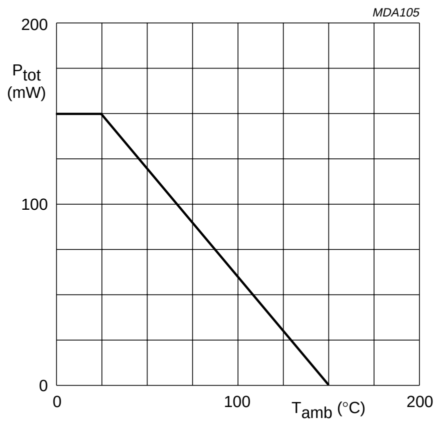
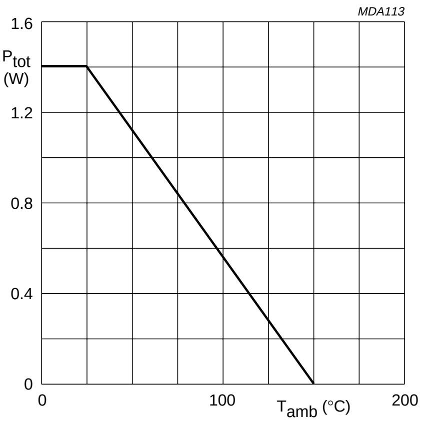
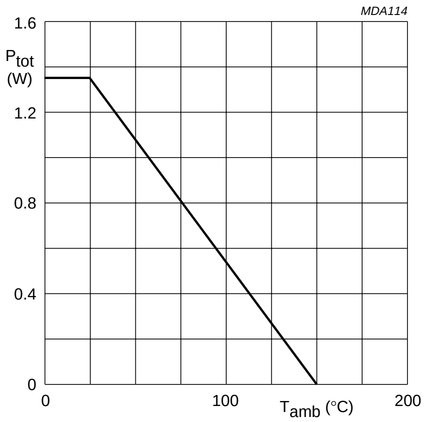


Fig.19 Power derating curve for SC-75 (SOT416).



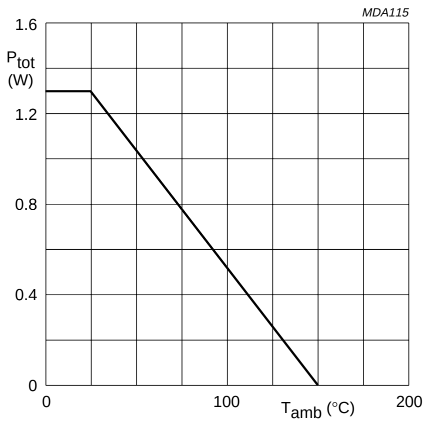
Device families:
BC868, BC869, BSR30, BSR40.

Fig.20 Power derating curve for SOT89.



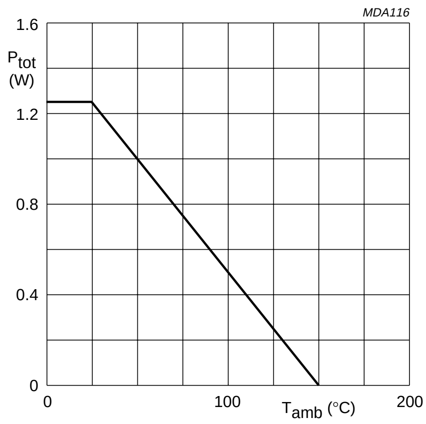
Device families:
BCX51, BCX54, BST15, BST50, BST60.

Fig.21 Power derating curve for SOT89.



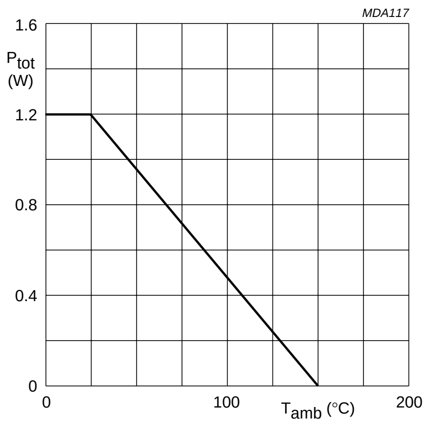
Device families:
BCV28/48, BCV29/49, PXTA14, PXTA27, PXTA64.

Fig.22 Power derating curve for SOT89.



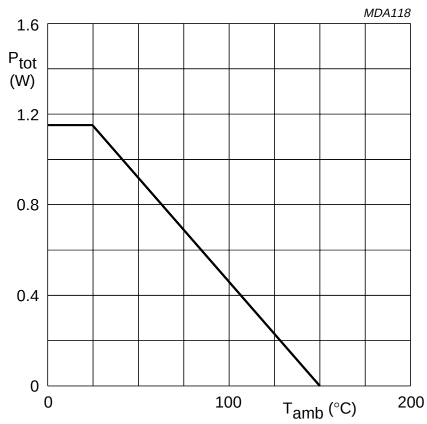
Device families:
BST39, PXTA42, PXTA92, PXT2907, PXT4403.

Fig.23 Power derating curve for SOT89.



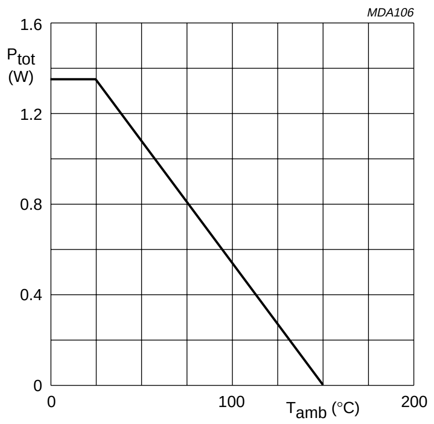
Device families:
BF620, BF621, PXT2222A, PXT4401.

Fig.24 Power derating curve for SOT89.



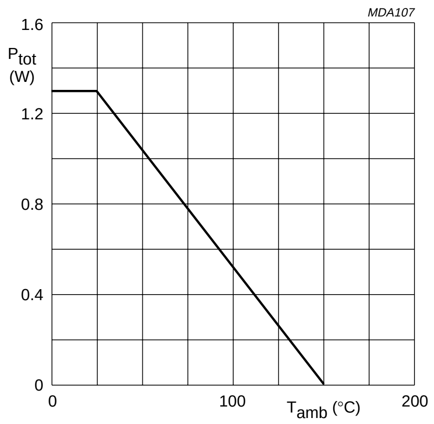
Device families:
PXT3904, PXT3906.

Fig.25 Power derating curve for SOT89.



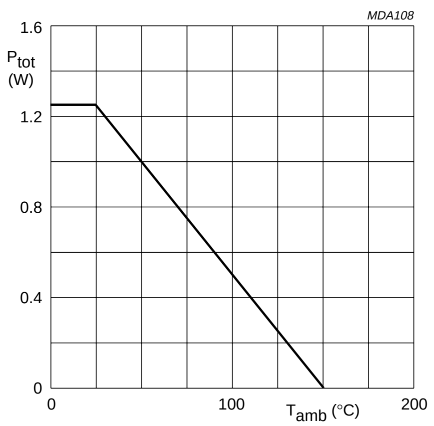
Device families:
BCP68, BCP69, BDL31, BDL32, BDP31, BDP32, PZTA44.

Fig.26 Power derating curve for SOT223.



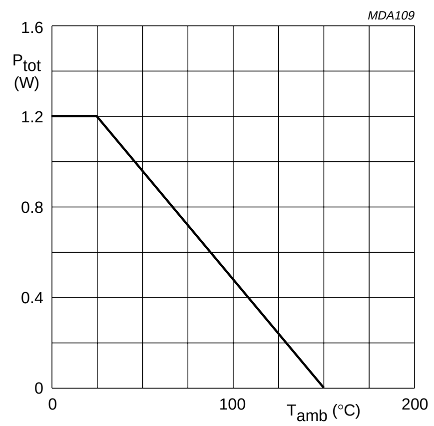
Device families:
BSP30, BSP40, BCP51, BCP54, BSP15.

Fig.27 Power derating curve for SOT223.



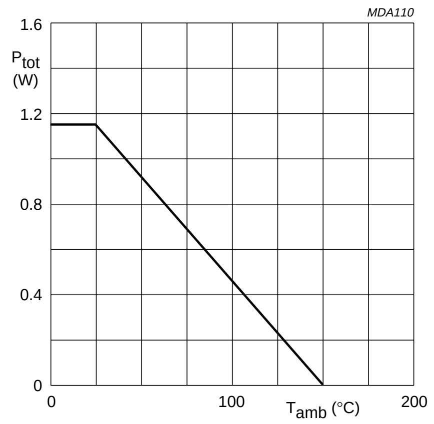
Device families:
BSP50, BSP60, BCP48, BCP49, PZTA13, PZTA63.

Fig.28 Power derating curve for SOT223.



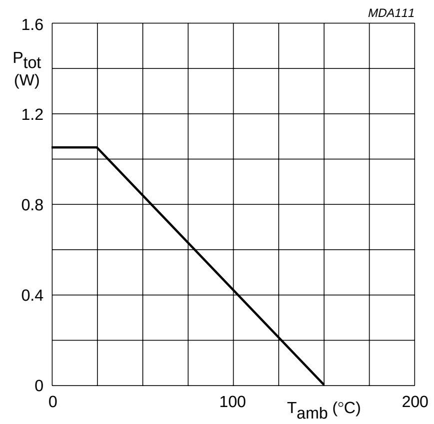
Device families:
PZTA05, PZTA55, BF720, BF721, BSP19, PZTA42, PZTA92.

Fig.29 Power derating curve for SOT223.



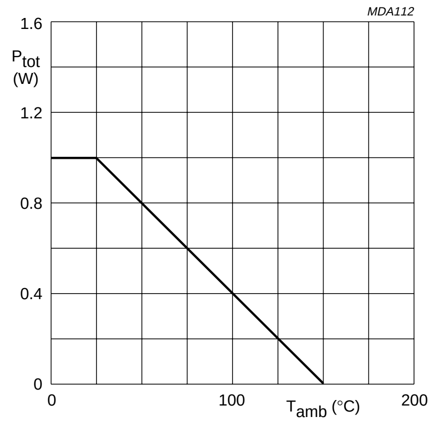
Device families:
PZTA2907A, PZT4403, PZT2222A, PZT4401, PZT5401, PZT5551.

Fig.30 Power derating curve for SOT223.



Device families:
PZT3904, PZT3906.

Fig.31 Power derating curve for SOT223.



Device family:
PZT2369A.

Fig.32 Power derating curve for SOT223.

THERMAL IMPEDANCE CURVES

Figures 33 through 54 on the following pages show the thermal impedance curves (Z_{th} versus t_p) for various duty cycles.

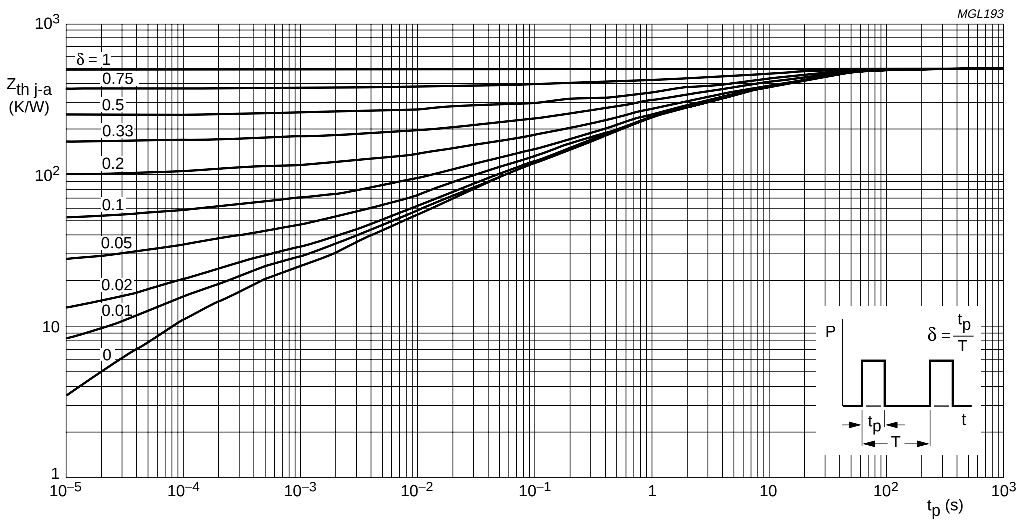


Fig.33 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT23.

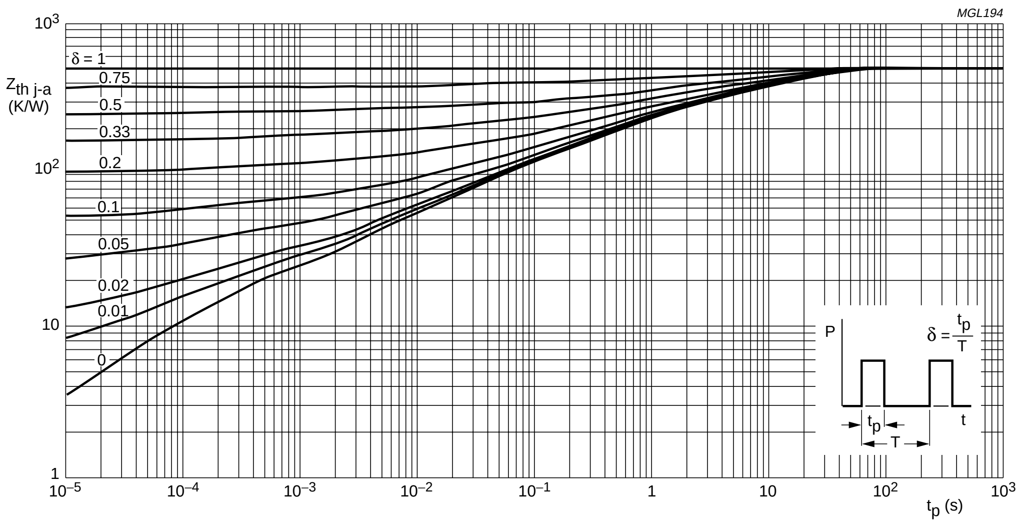


Fig.34 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT143.

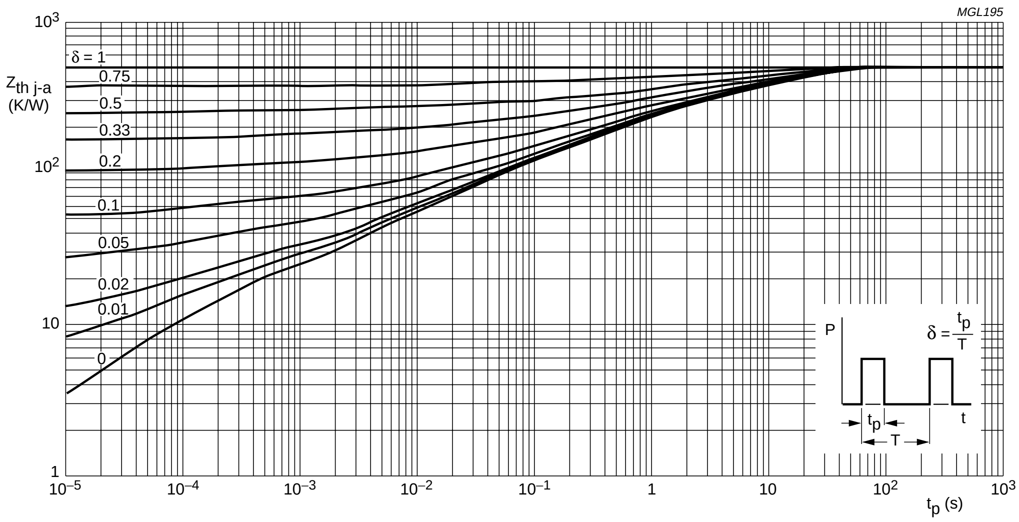


Fig.35 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SC-59 (SOT346).

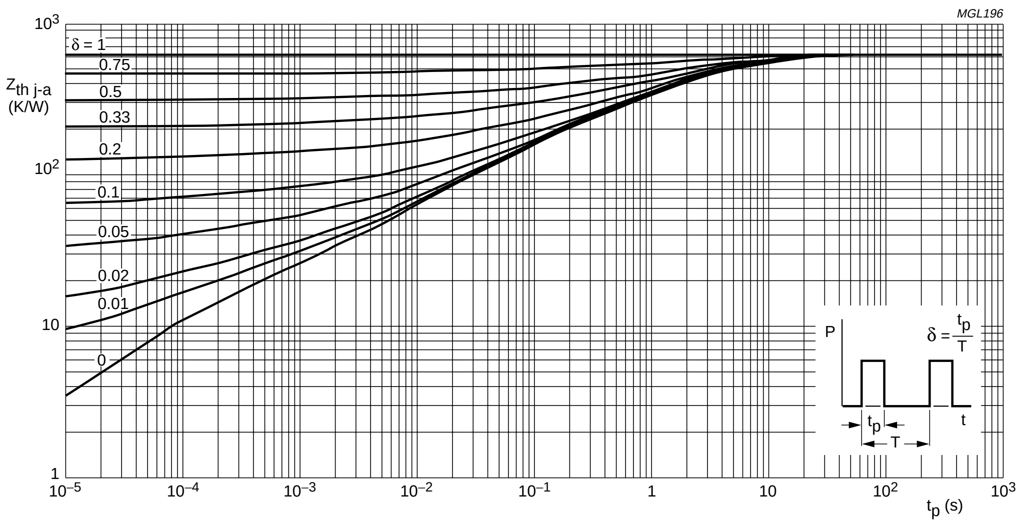


Fig.36 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SC-70 (SOT323).

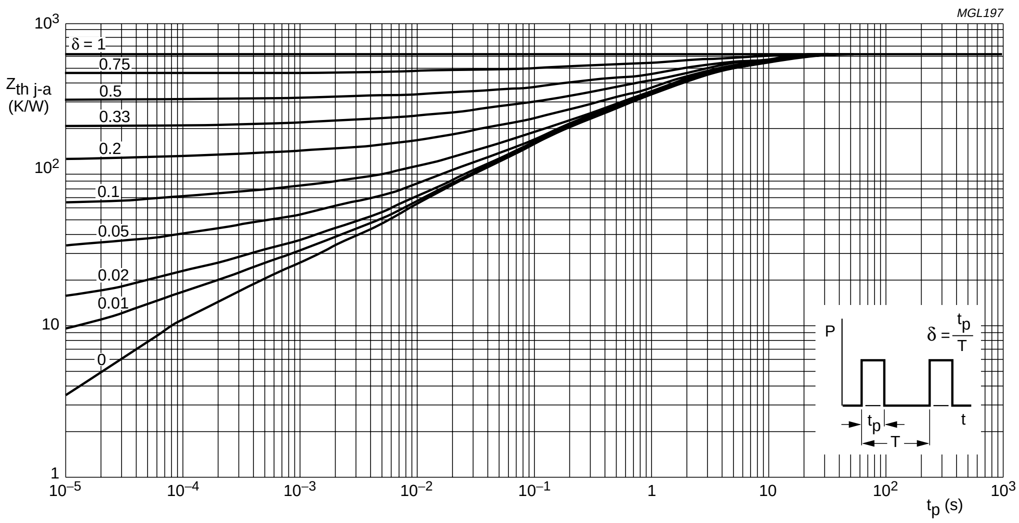


Fig.37 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SC-88 (SOT363).

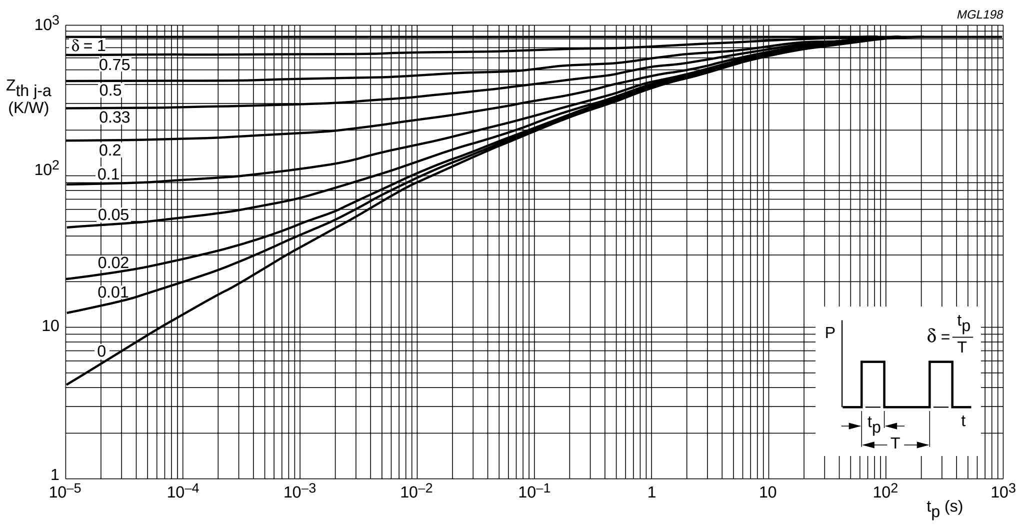
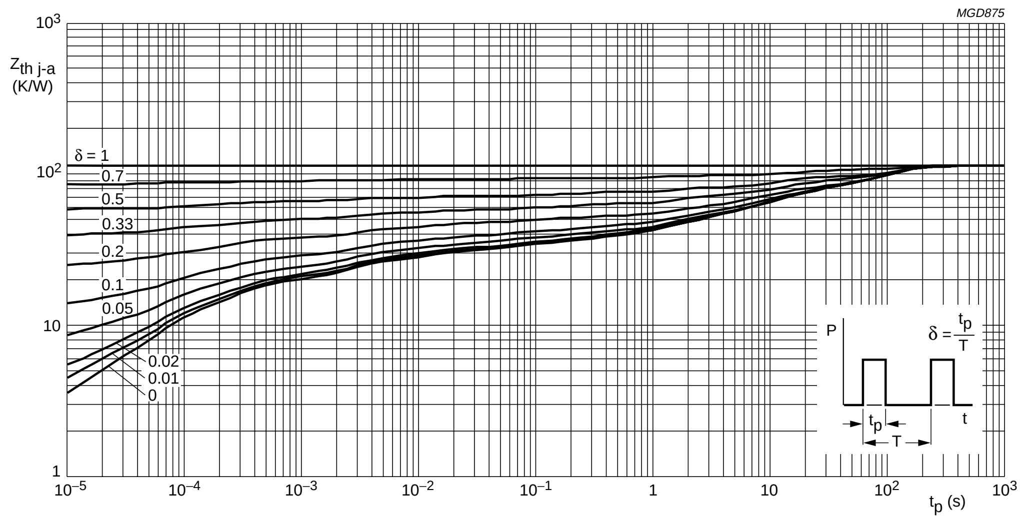
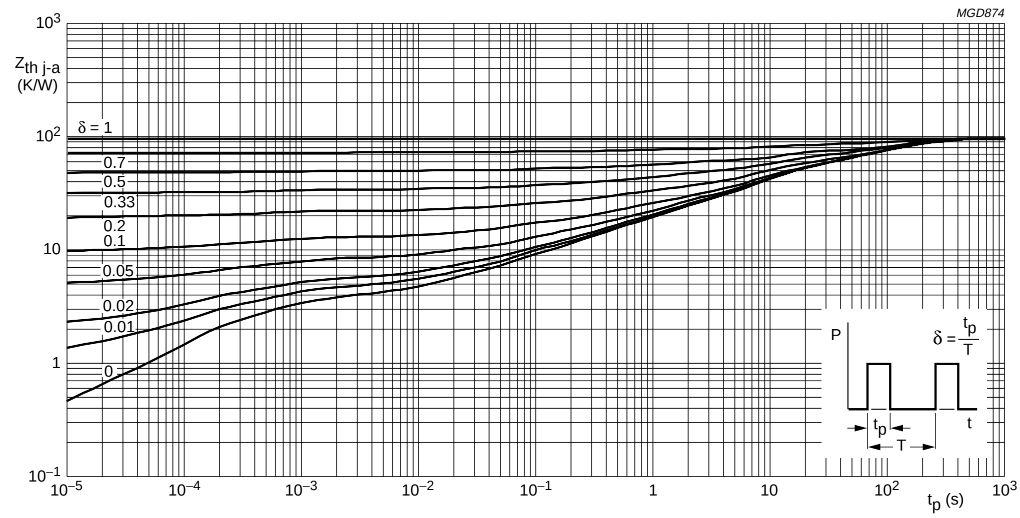


Fig.38 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SC-75 (SOT416).



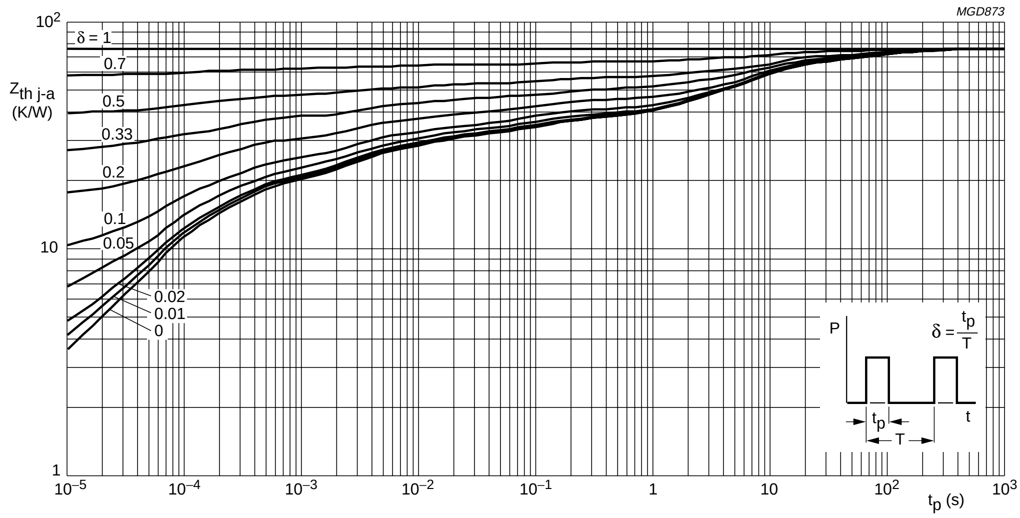
PCB, single-sided, unplated, Rth j-s = 25 K/W, Rth j-a = 113 K/W.
See also Fig.10 curve (1).

Fig.39 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT89.



PCB, single-sided, plated, Rth j-s = 7 K/W, Rth j-a = 95 K/W.
See also Fig.10 curve (2).

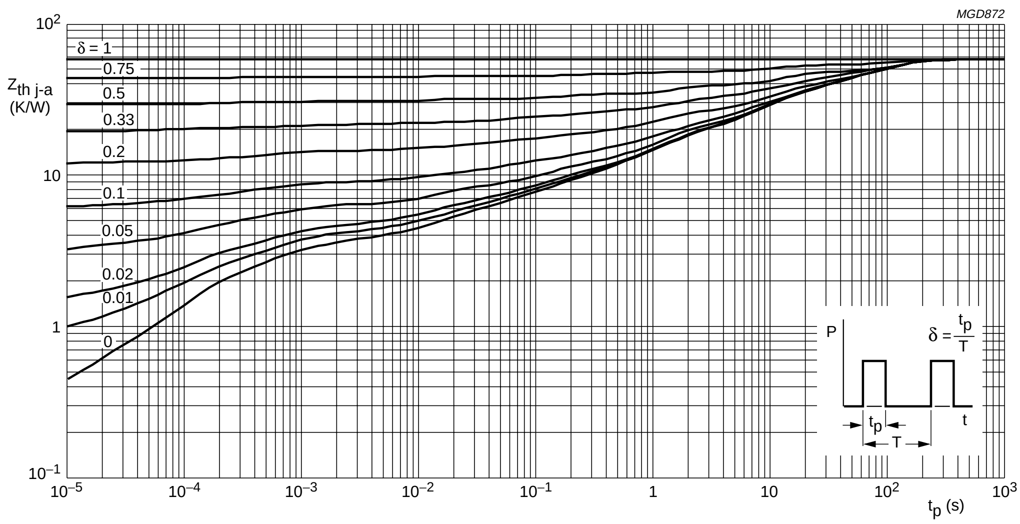
Fig.40 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT89.



PCB, double-sided, unplated, Rth j-s = 25 K/W, Rth j-a = 76 K/W.

See also Fig.10 curve (3).

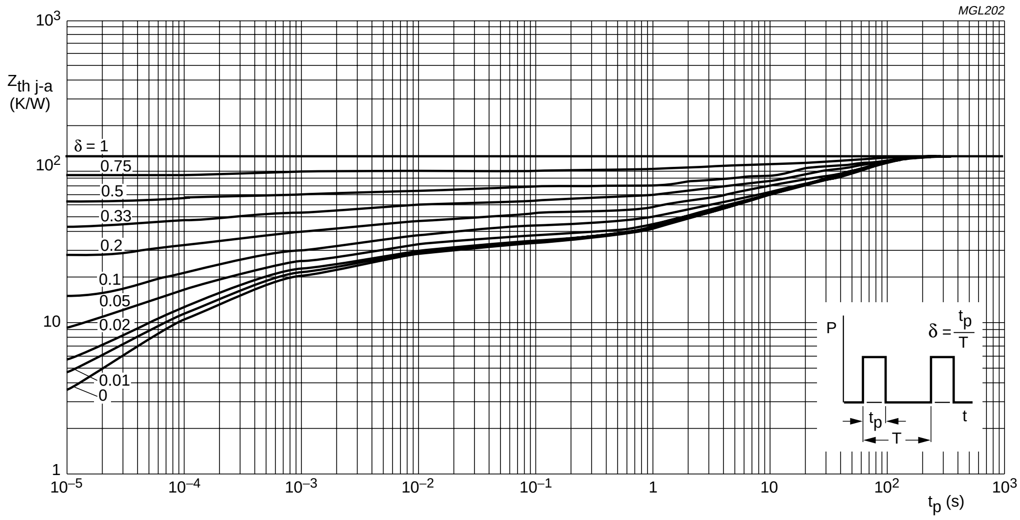
Fig.41 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT89.



PCB, double-sided, plated, Rth j-s = 7 K/W, Rth j-a = 58 K/W.

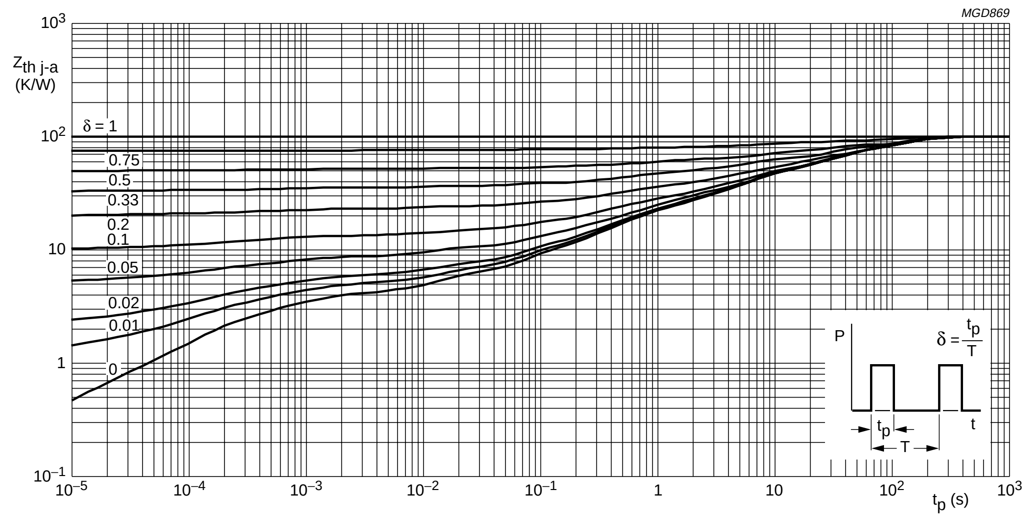
See also Fig.10 curve (4).

Fig.42 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT89.



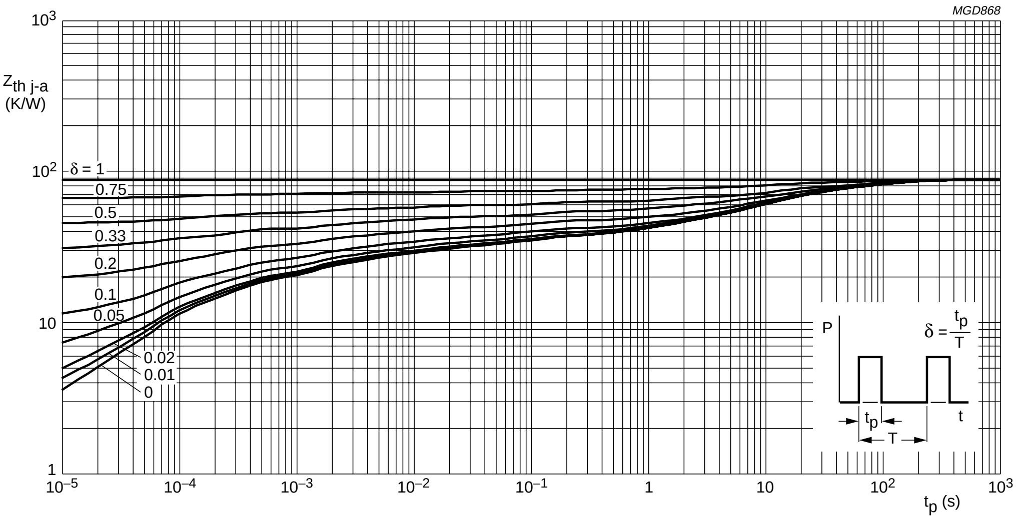
PCB, single-sided, unplated, Rth j-s = 36 K/W, Rth j-a = 124 K/W.
See also Fig.10 curve (1).

Fig.43 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT223.



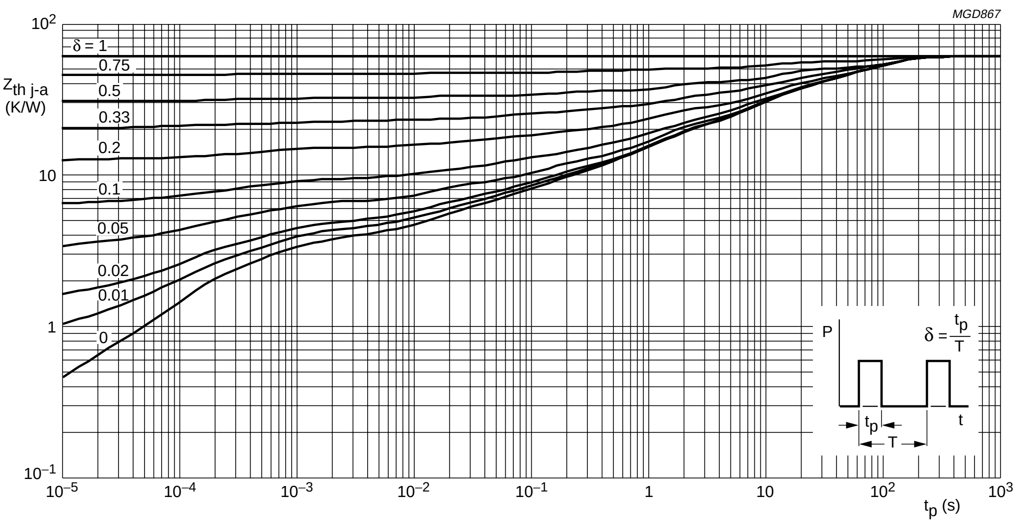
PCB, single-sided, plated, Rth j-s = 10 K/W, Rth j-a = 98 K/W.
See also Fig.10 curve (2).

Fig.44 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT223.



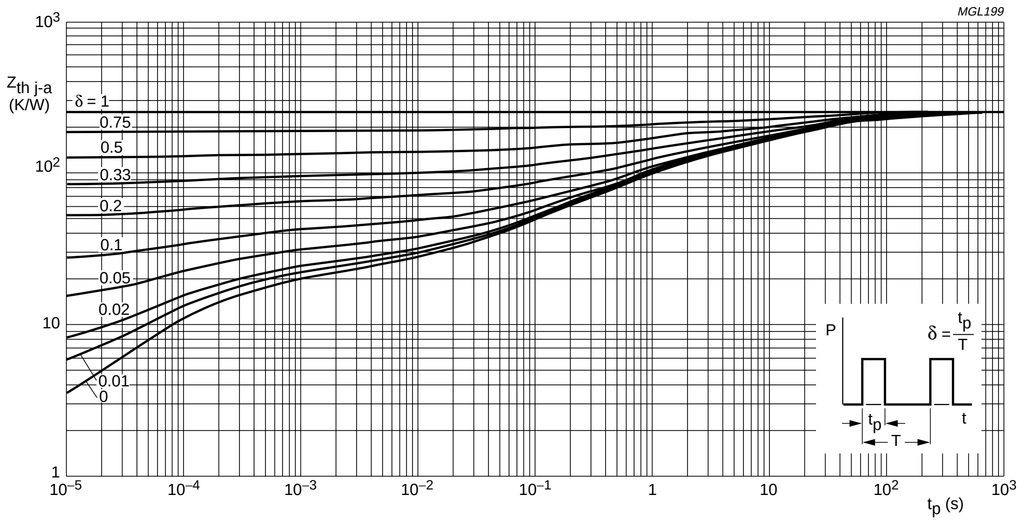
PCB, double-sided, unplated, Rth j-s = 36 K/W, Rth j-a = 87 K/W.
See also Fig.10 curve (3).

Fig.45 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT223.



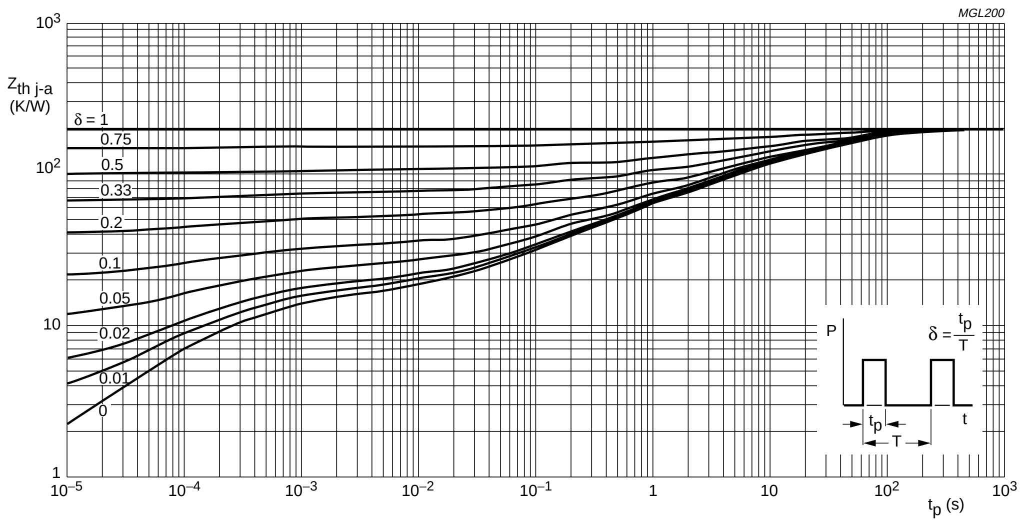
PCB, double-sided, plated, Rth j-s = 10 K/W, Rth j-a = 61 K/W.
See also Fig.10 curve (4).

Fig.46 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT223.



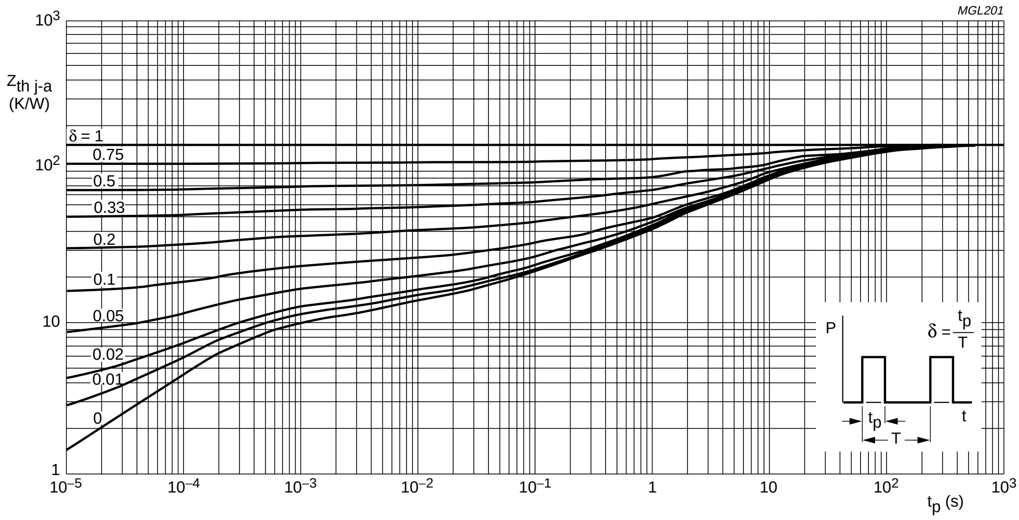
Curves are for devices with P_{tot} = 500 mW.

Fig.47 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT54.



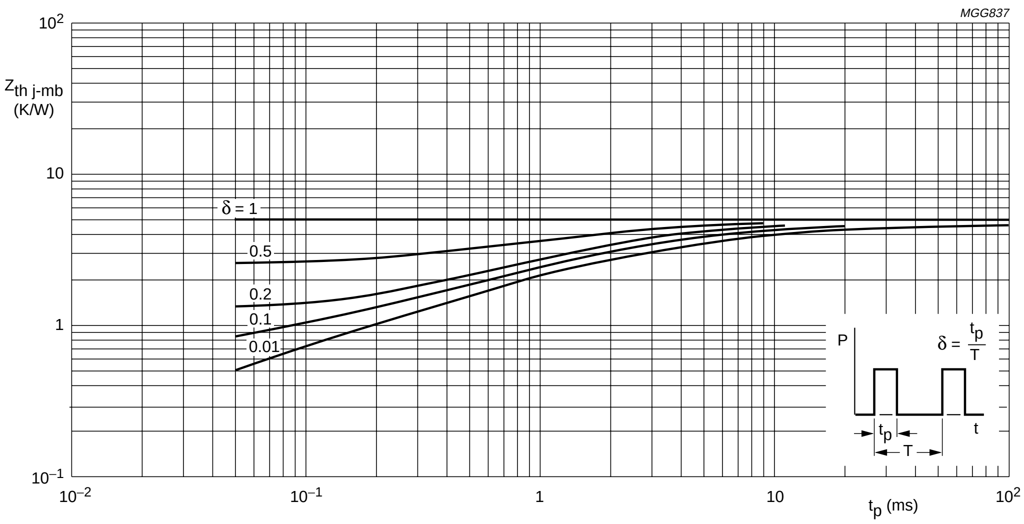
Curves are for devices with P_{tot} = 625 mW.

Fig.48 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT54.



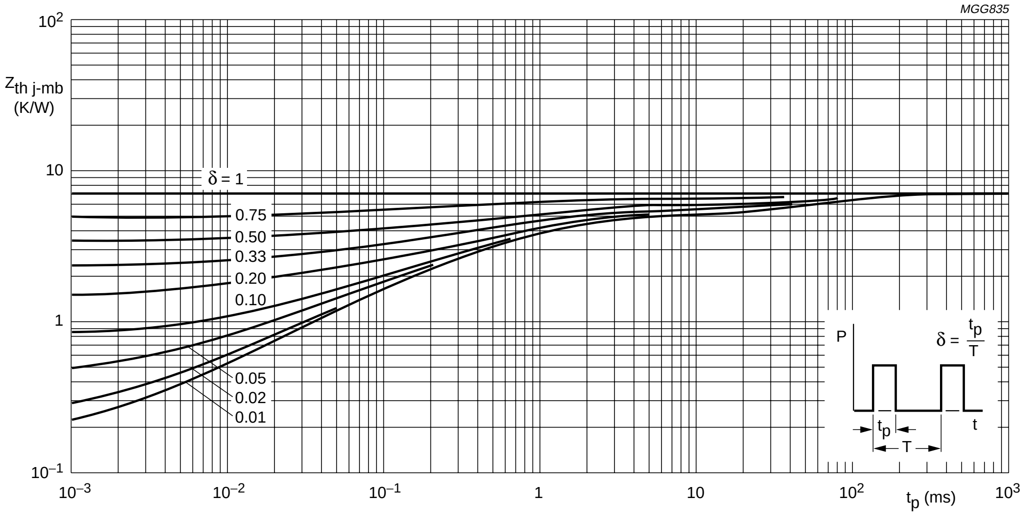
Curves are for devices with P_{tot} = 830 mW.

Fig.49 Thermal impedance curves (junction to ambient) for transistors mounted onto a PCB for SOT54.



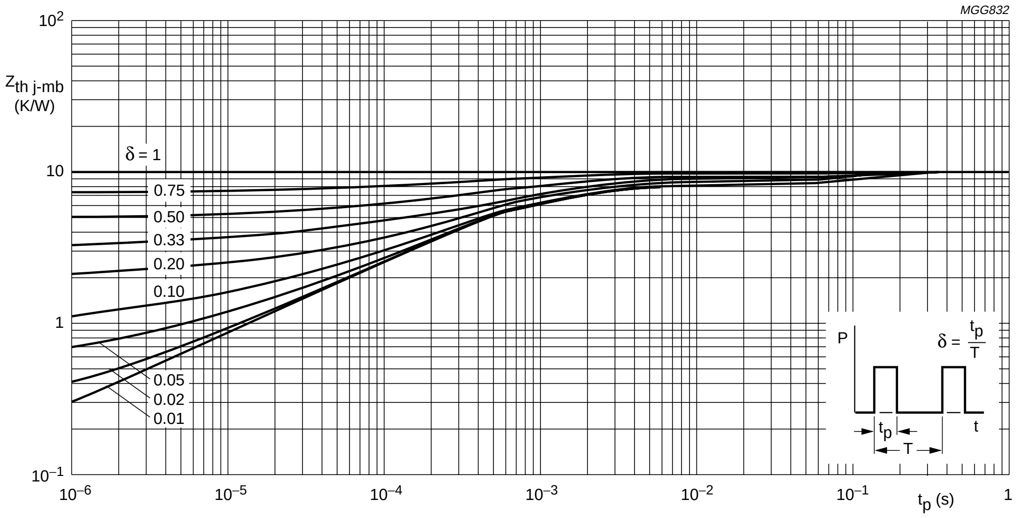
Device example: BDX35.

Fig.50 Thermal impedance curves (junction to mounting-base) for transistors mounted onto a PCB for TO-126 (SOT32).



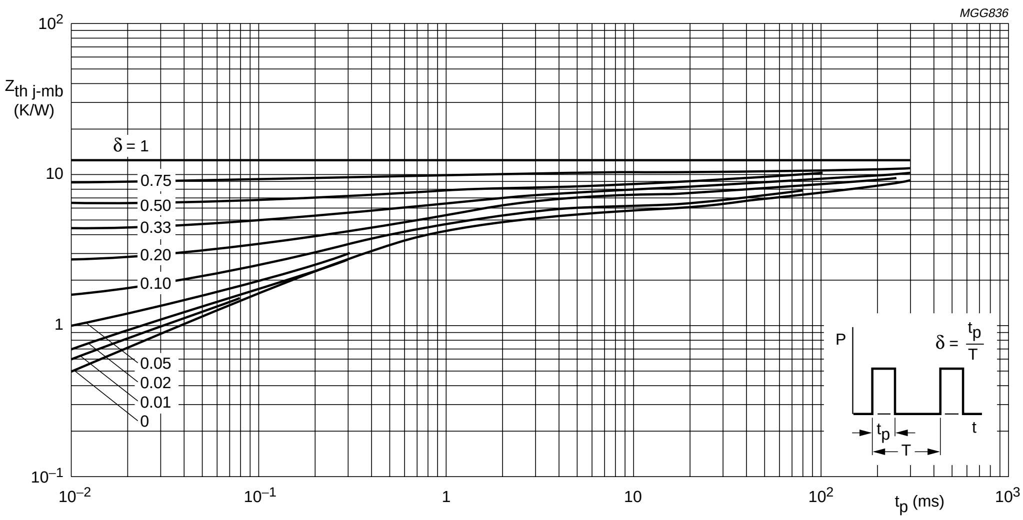
Device example: BD226.

Fig.51 Thermal impedance curves (junction to mounting-base) for transistors mounted onto a PCB for TO-126 (SOT32).



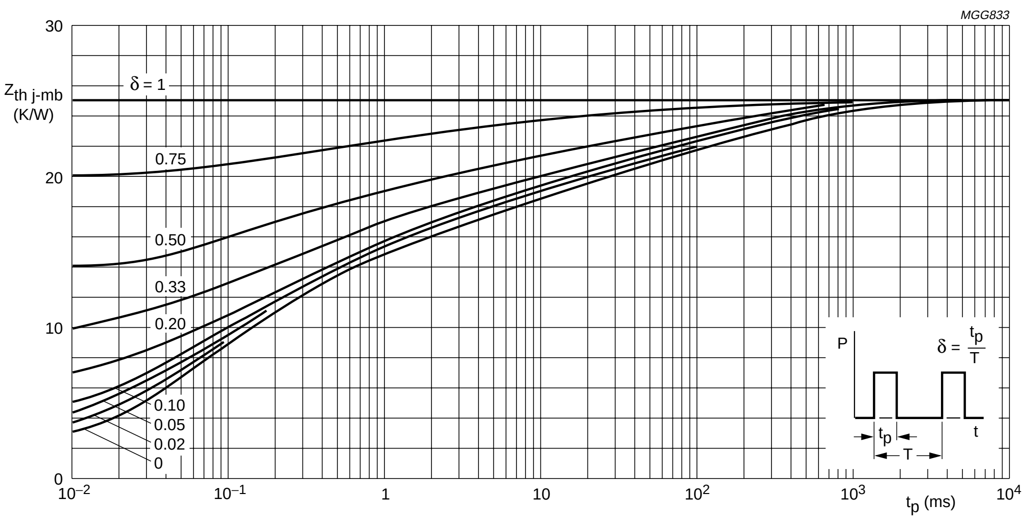
Device example: BD136.

Fig.52 Thermal impedance curves (junction to mounting-base) for transistors mounted onto a PCB for TO-126 (SOT32).



Device example: BD839.

Fig.53 Thermal impedance curves (junction to mounting-base) for transistors mounted onto a PCB for TO-202 (SOT128).



Device example: BF869.

Fig.54 Thermal impedance curves (junction to mounting-base) for transistors mounted onto a PCB for TO-202 (SOT128).

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