To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

RENESAS
Renesas Technology Corp.

RENESAS

Application Note

SRAM

Compatibility of Network SRAM and ZBT SRAM

RENESAS

Renesas Technology Corp.

Keep safety first in your circuit designs!

Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.

Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein. The information described here may contain technical inaccuracies or typographical errors. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors. Please also pay attention to information published by Mitsubishi Electric Corporation by various means, including the Mitsubishi Semiconductor home page (http://www.mitsubishichips.com).

When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.

Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.

The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.

If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination. Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.

Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.

RENESAS
Renesas Technology Corp.

Contents

1. Introduction

ZBT "Zero Bus Turnaround" is the functional technology of the synchronous fast SRAM advocated by IDT (Integrated Device Technology and Inc.) in October 1996. Now, this technology is the mainstream technology of the synchronous fast SRAM, and almost all each high-speed SRAM maker is developing the product of the same technology by the respectively original name (product name). "ZBT" name use is restricted to some makers, IDT, Micron, and Motorola on the relation of a trademark. Therefore, there are various product names* and it will be recognized as an incompatible product. However, each product is a product with the compatibility based on the same function of operation. The product of Mitsubishi Electric is called Network SRAM ("Network SRAM" is a JEDEC formal name).

This document is a technical document for reference which checked the compatibility (package form, pin arrangement, function of operation) of Mitsubishi Network SRAM and the other company ZBT SRAM. In addition, about a detailed function and a detailed electrical characteristic, there may be a difference in addition to the contents described by these technical document. When actually introduced to a customer, you confirm a data sheet or please consult to the Mitsubishi Electric design section.

  * Each maker product name
  ZBT (Zero Bus Turnaround) also manufactures Micron and Motorola with the trademark of IDT.
  NtRAM (No Turnaround RAM) also manufactures Toshiba with the trademark of Samsung.
  NoBL (No Bus Latency) is the trademark of Cypress.
  NBT (No Bus Turnaround) is the trademark of GSI.
  ZEROSB (ZERO Synchronous Burst) is the trademark of NEC.
  No-Wait Synchronous SRAM is the trademark of ISSI.
  ZBL (Zero Bus Latency) is the trademark of Hitachi.

2. Package, Pinout (Ball Bump)

Package and pinout are the most important items in the case of checking compatibility. Mitsubishi Network SRAM is offered with the 100 pin TQFP (Thin Quad Flat Package) package and the 165 ball FBGA (ball pitch 1.00mm). This TQFP package is a JEDEC standard package, and is offered by almost all the synchronous fast SRAM. Naturally, ZBT SRAM is also offered with the 100 pin TQFP and the 165 ball FBGA, and since pinout of an address, control, a power supply, etc. is also the same, it can be replaced easily. However, although layout of pinout is different by some address pins, when a customer actually use, there is no problem (Please refer to Figure 1, Table 1 and Table 2). About the pin compatible of a 100 pin TQFP package, the Mitsubishi's Network SRAM, IDT's IDT71T5602SxxPF, and Samsung's K7N163645 A-Q are compared. In addition, about the compatibility with a ball bump of a 165 ball FBGA package, Samsung's NtRAM KN7N163645 A-F is compared with the Mitsubishi's Network SRAM.

In the case of 165 balls, since there is a functional difference with some terminals (ball bump), please take care. (Please refer to Figure 2 and Table 3 to Table 5.)
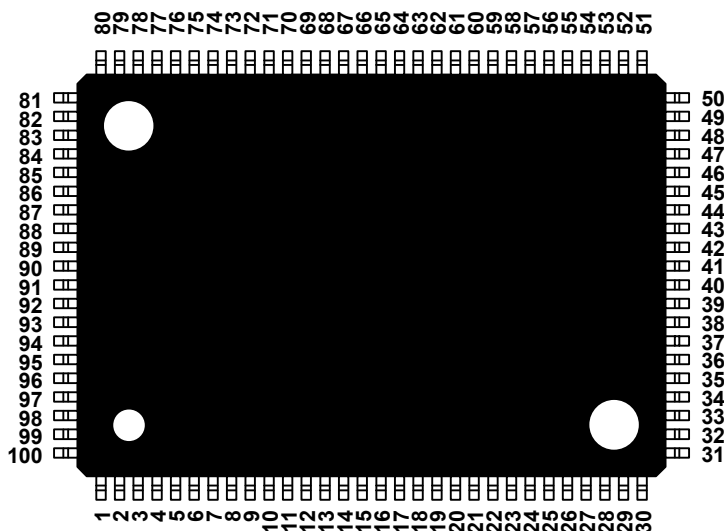

Figure 1 The Package Outside Figure of the 100 pin TQFP

Table 1 Pinout of Mitsubishi's Network SRAM, IDT's ZBT SRAM, and Samsung's NtRAM

Pin number	Mitsubishi's Network SRAM	IDT's ZBT SRAM	Samsung's NtRAM	Pin number	Mitsubishi's Network SRAM	IDT's ZBT SRAM	Samsung's NtRAM
1	DQPc	I/OP3	DQPc	51	DQPa	I/OP1	DQPa
2	DQc	I/O16	DQc0	52	DQa	I/O0	DQa0
3	DQc	I/O17	DQc1	53	DQa	I/O1	DQa1
4	VDDQ	VDDQ	VDDQ	54	VDDQ	VDDQ	VDDQ
5	VSSQ	VSS	VSSQ	55	VSSQ	VSS	VSSQ
6	DQc	I/O18	DQc2	56	DQa	I/O2	DQa2
7	DQc	I/O19	DQc3	57	DQa	I/O3	DQa3
8	DQc	I/O20	DQc4	58	DQa	I/O4	DQa4
9	DQc	I/O21	DQc5	59	DQa	I/O5	DQa5
10	VSSQ	VSS	VSSQ	60	VSSQ	VSS	VSSQ
11	VDDQ	VDDQ	VDDQ	61	VDDQ	VDDQ	VDDQ
12	DQc	I/O22	DQc6	62	DQa	I/O6	DQa6
13	DQc	I/O23	DQc7	63	DQa	I/O7	DQa7
14	MCH	VDD	VDD	64	ZZ	ZZ	ZZ
15	VDD	VDD	VDD	65	VDD	VDD	VDD
16	MCH	VDD	VDD	66	MCH	VDD	VDD
17	VSS	VSS	VSS	67	VSS	VSS	VSS
18	DQd	I/O24	DQd0	68	DQb	I/O8	DQb0
19	DQd	I/O25	DQd1	69	DQb	I/O9	DQb1
20	VDDQ	VDDQ	VDDQ	70	VDDQ	VDDQ	VDDQ
21	VSSQ	VSS	VSSQ	71	VSSQ	VSS	VSSQ
22	DQd	I/O26	DQd2	72	DQb	I/O10	DQb2
23	DQd	I/O27	DQd3	73	DQb	I/O11	DQb3
24	DQd	I/O28	DQd4	74	DQb	I/O12	DQb4
25	DQd	I/O29	DQd5	75	DQb	I/O13	DQb5
26	VSSQ	VSS	VSSQ	76	VSSQ	VSS	VSSQ
27	VDDQ	VDDQ	VDDQ	77	VDDQ	VDDQ	VDDQ
28	DQd	I/O30	DQd6	78	DQb	I/O14	DQb6
29	DQd	I/O31	DQd7	79	DQb	I/O15	DQb7
30	DQPd	I/OP4	DQPd	80	DQPb	I/OP2	DQPb
31	LBO#	LBO#	LBO#	81	A9	A9	A9
32	A5	A5	A5	82	A8	A8	A8
33	A4	A4	A4	83	A17	A17	A17
34	A3	A3	A3	84	A18	A18	A18
35	A2	A2	A2	85	ADV	ADV/LD#	ADV
36	A1	A1	A1	86	G#	OE#	OE#
37	A0	A0	A0	87	CKE#	CEN#	CKE#
38	NC	NC/TMS	N.C.	88	W#	R/W#	WE#
39	NC	NC/TDI	N.C.	89	CLK	CLK	CLK
40	VSS	VSS	VSS	90	VSS	VSS	VSS
41	VDD	VDD	VDD	91	VDD	VDD	VDD
42	NC	NC/TDO	N.C.	92	E3#	CE2#	CS2#
43	NC	NC/TCK	N.C.	93	BWa#	BW1#	BWa#
44	A16	A10	A10	94	BWb#	BW2#	BWb#
45	A15	A11	A11	95	BWc#	BW3#	BWc#
46	A14	A12	A12	96	BWd#	BW4#	BWd#
47	A13	A13	A13	97	E2	CE2	CS2
48	A12	A14	A14	98	E1#	CE1#	CS1#
49	A11	A15	A15	99	A7	A7	A7
50	A10	A16	A16	100	A6	A6	A6

Note 1.   The shaded part shows the pin by which a function is different between products (cautions are required).

Table 2 Difference between Mitsubishi's Network SRAM, IDT's ZBT SRAM, and Samsung's NtRAM (100 pin TQFP)

Pin number	Mitsubishi's Network SRAM	IDT's ZBT SRAM	Samsung's NtRAM
16	MCH (Must Connect High) (Note 2)	VDD	VDD
44	A16 (Note 3)	A10	A10
45	A15 (Note 3)	A11	A11
46	A14 (Note 3)	A12	A12
47	A13 (Note 3)	A13	A13
48	A12 (Note 3)	A14	A14
49	A11 (Note 3)	A15	A15
50	A10 (Note 3)	A16	A16
66	MCH (Must Connect High) (Note 2)	VDD	VDD

Note 2.   In Mitsubishi's Network SRAM, the pin numbers 16 and 66 are MCH (Must Connect High) pins.
Therefore, it is necessary to connect this pin to VDD or to input the voltage more than VIH ("High" input).
If the customer is using IDT's ZBT SRAM, Samsung's NtRAM and the pin numbers 16 and 66 are
connected to VDD, it is not necessary to change the design of a mounting board.

Note 3.   In Mitsubishi's Network SRAM, the address pins A16-A10 are assigned to the pin numbers 44-50, and
this assignment is the order of reverse of IDT's ZBT SRAM, and Samsung's NtRAM. In the case of the
synchronous fast SRAM, pin assignment of A0 address and A1 address is important because of
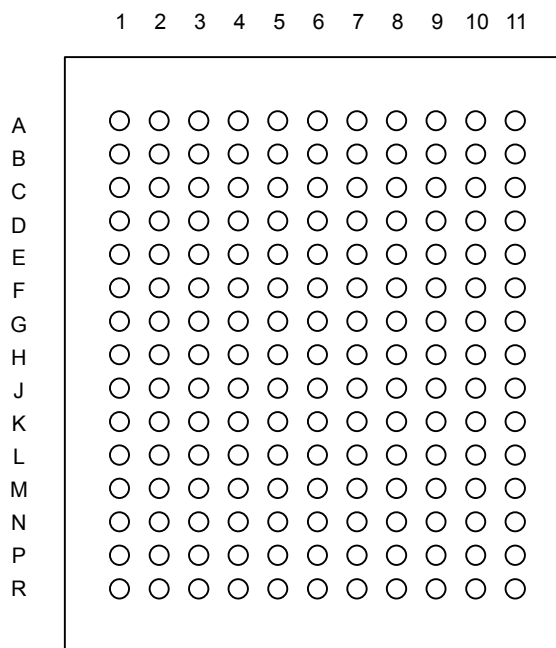internal burst counter control. However, even if it changes about other address pins, there is no
problem.

Figure 2 The Package Outside Figure of the 165 ball FBGA (Top View)

Table 3 Ball Bump of Mitsubishi's Network SRAM (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	E1#	BWc#	BWb#	E3#	CKE#	ADV	A17	A8	NC
B	NC	A6	E2	BWd#	BWa#	CLK	W#	G#	A18	A9	NC
C	DQPc	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	MCH	MCH	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	VSS	NC	NC	MCH	VSS	VDDQ	NC	DQPa
P	NC	NC	A5	A3	TDI	A1	TDO	A15	A13	A11	NC
R	LBO#	NC	A4	A2	TMS	A0	TCK	A16	A14	A12	A10

Table 4 Ball Bump of Mitsubishi's Network SRAM (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	CS1#	BWc#	BWb#	CE2#	CKE#	ADV	A	A	NC
B	NC	A	CS2	BWd#	BWa#	CLK	WE#	OE#	A	A	NC
C	DQPc	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQPa
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC
R	LBO#	NC	A	A	TMS	A0	TCK	A	A	A	A

Note 4.   The shaded part shows the ball by which a function is different between products.

Table 5 Difference between Mitsubishi's Network SRAM, Samsung's NtRAM (165 ball FBGA)

Bump number	Mitsubishi's Network SRAM	Samsung's NtRAM
H1	MCH (Must Connect High) (Note 5)	NC
N7	MCH (Must Connect High) (Note 5)	NC

Note 5.   In Mitsubishi's Network SRAM, the ball bump numbers H1 and N7 are MCH (Must Connect High) balls. Therefore, it is necessary to connect this ball to VDD or to input the voltage more than VIH ("High" input). The ball bump numbers H1 and N7 (NC ball) of the Samsung's NtRAM are non-connected ball bumps. Therefore, when the customers using NtRAM and replace to Network SRAM, it is necessary to change a substrate.

3. Function

3.1. ZBT Function

By using all bus cycles, ZBT SRAM is the synchronous fast SRAM which provides the maximum with the throughput of a system. When write operation and read operation are performed continuously, the turnaround cycle (dead cycle) of 2 cycle will produce the conventional synchronous fast SRAM represented by the pipeline burst SRAM.

As the name shows ZBT SRAM, even when write operation and read operation are performed continuously, an unnecessary turnaround cycle (dead cycle) is not generated. Therefore, a system can offer a fixed bandwidth. This function (feature) demonstrates the performance by the system (network equipment) which performs read operation and write operation to mutual (random) timing rather than systems (cache memory of a computer etc.[Note 6]) by which read operation or write operation continues. Each timing figure is shown in Figure 3.

• Operation of the pipeline burst SRAM
In read operation, an address is inputted by the rising edge of a clock and read data is outputted by the rising edge of the clock after 2 cycles by the pipeline circuit. In write operation, an address and write data are simultaneously inputted by the rising edge of a clock.

• Operation of the ZBT SRAM
In read operation, ZBT SRAM is also the same operation as the pipeline burst SRAM. Although write operation is different and an address is inputted by the rising edge of a clock, write data is not inputted to the same timing. Data is inputted by the rising edge of the clock after 2 cycles as well as read operation.
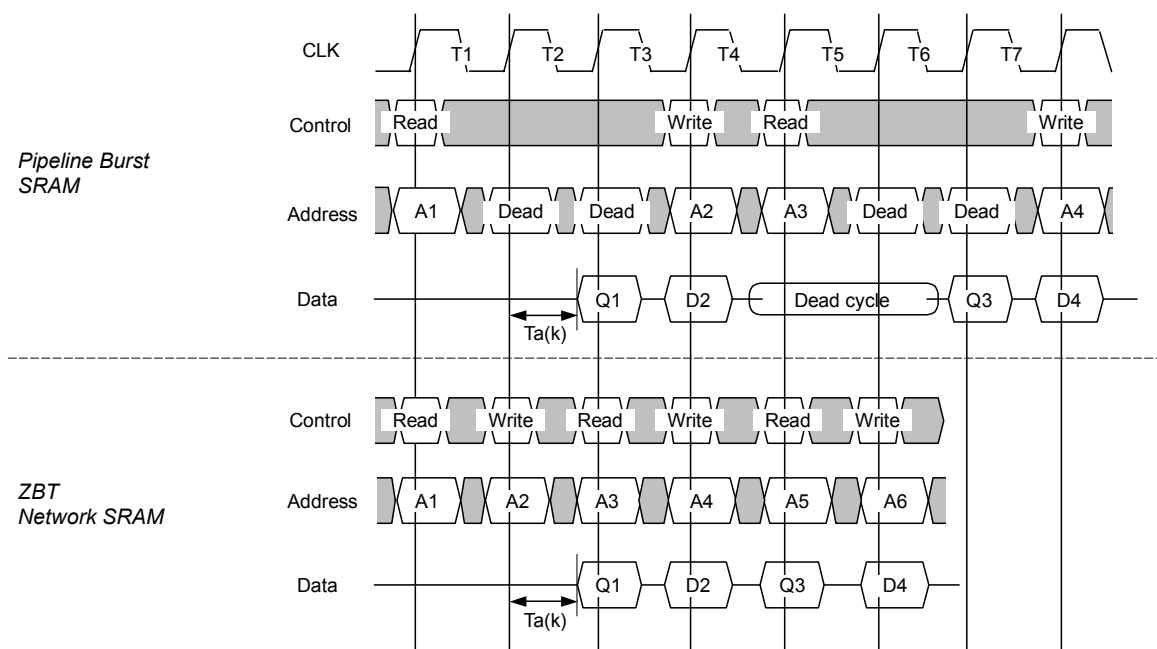

Figure 3 Read / write Operation Timing Figure of Pipeline Burst SRAM and ZBT SRAM (Network SRAM)

Note 6.   The pipeline burst SRAM is used as a secondary cache memory of a computer. Therefore, there are an ADSC# signal of the input from a cash controller and an ADSP# signal of the input from a processor as an address control signal of the pipeline burst SRAM in addition to an ADV# signal. As for ZBT SRAM, the address control signal is as simple as an ADV# signal.

3.2. Burst Sequence

The burst sequence (The method of an address motion at the time of burst operation, It is also called a burst order.) of the synchronous formula SRAM has two kinds, an Interleaved Burst[Note 7] and a Linear Burst[Note 7].

As for an Interleaved Burst sequence, the next reverses a bit 0 (A0) after the first address, and the next reverses a bit 1 and a bit 0, and, finally reverses a bit 0.

As for a linear burst sequence, an address progresses bits 0/1 in order of 00->01->10->11. Each sequence is shown in Table 3. In addition, each burst sequence is chosen on the input level[Note 8] of the LBO# pin (or MODE pin) of the pin number 31 (in the case of a TQFP package).

Each product, such as Network SRAM, ZBT SRAM, and NtRAM, is a synchronous fast SRAM product of the same burst sequence. Therefore, replacing between each product is possible.

Note 7.   A sequence changes with processors of a system. An interleaved burst sequence is used in the processor of the Intel (Intel) systems, such as 80486 and Pentium. Other RISC system processors etc. are using the linear burst sequence.

Note 8.   A linear burst sequence will be chosen if an LBO# (MODE) pin is made into a Low (VSS) level. An interleaved burst is chosen on a High (VDD) level (at Network SRAM, it can choose also in the open state : NC).

Table 6 Burst Sequence Table

Burst Mode	A [1:0]			
	First Access	Second Access	Third Access	Fourth Access
Linear Burst	00	01	10	11
	01	10	11	00
	10	11	00	01
	11	00	01	10
Interleaved Burst	00	01	10	11
	01	00	11	10
	10	11	00	01
	11	10	01	00

3.3. Operation

Operation of the synchronous fast SRAM including ZBT SRAM is performed synchronizing with the rising edge of a clock. Therefore, about operation, mode of operation is determined in the state of each control pin in clock edge. Each maker shows mode of operation as a truth table of a synchronous input within the data sheet. Table 7 is the result of comparing the contents of a truth table about the Mitsubishi's Network SRAM, the IDT's ZBT SRAM, and the Samsung's NtRAM. All modes of operation are the same. Therefore, replacing between each product is possible.

Table 7 The Truth Table in Mode of Operation of Mitsubishi's Network SRAM, IDT's ZBT SRAM, and Samsung's NtRAM

Operation	Mitsubishi's Network SRAM	IDT's ZBT SRAM	Samsung's NtRAM
Read Cycle (Begin Burst)	O	O	O
Read Cycle (Continue Burst)	O	O	O
Write Cycle (Begin Burst)	O	O	O
Write Cycle (Continue Burst)	O	O	O
NOP/Write About (Begin Burst)	O	O	O
NOP/Write About (Continue Burst)	O	O	O
Deselect Cycle	O	O	O
Continue Deselect Cycle	O	O	O
Ignore Clock edge, Stall	O	O	O
Snooze Mode	O	O	O

Note 9.   It is shown that a round mark is compatible.

4. Electrical Characteristics (3.3V Power Supply)

The main differences about the electrical characteristics of the Mitsubishi's Network SRAM (M5M5V5636GP) and the Samsung's NtRAM (K7N163601 A-Q) are described. The product of operation voltage 3.3V, the frequency of 166MHz of operation, and the package 100 pin TQFP is compared as product specification (Since there is no product with an of operation frequency of 166MHz, ZBT SRAM is not compared).

4.1. Absolute Maximum Ratings

The absolute maximum rating of the Mitsubishi's Network SRAM (M5M5V5636GP) and the Samsung's NtRAM (K7N163601 A-Q) is shown in Table 8.

Table 8 Absolute Maximum Ratings

Parameter	Mitsubishi's Network SRAM	Samsung's NtRAM	Unit
Power Supply Voltage	$-1.0^{Note\ 10} \sim 4.6$	$-0.3 \sim 4.6$	V
Input Voltage	$-1.0 \sim VDDQ+1.0^{Note\ 11}$	$-0.3 \sim VDDQ+0.3$	V

Note 10.   This is -1.0V when pulse width $\leq$ 2.0ns, and -0.5V in case of DC.
Note 11.   This is -1.0V - VDDQ+1.0V when pulse width $\leq$ 2.0ns, and -0.5V - VDDQ+0.5V in case of DC.
VDDQ=3.135~3.465V/2.375~2.625V

4.2. DC Electrical Characteristics

The DC electrical characteristics of the Mitsubishi's Network SRAM (M5M5V5636GP) and the Samsung's NtRAM (K7N163601 A-Q) is shown in   Table 9.

Table 9 DC Electrical Characteristics

Parameter	Mitsubishi's Network SRAM	Samsung's NtRAM	Unit
I/O Buffer Power Supply Voltage (2.5V I/O)	$2.375 \sim 2.625$	$2.375 \sim 2.9$	V
High-level Output Voltage (Min)	$VDDQ-0.4^{Note\ 12}$	2.0	V
Input Current (Max)	10	2	μA
Power supply current: operating	380	340	mA

Note 12.   VDDQ=3.135~3.465V/2.375~2.625V

4.3. Capacitance

The Capacitance of the Mitsubishi's Network SRAM (M5M5V5636GP) and the Samsung's NtRAM (K7N163601 A-Q) is shown in Table 10.

Table 10 Capacitance

Parameter	Mitsubishi's Network SRAM	Samsung's NtRAM	Unit
Input Capacitance (Max)	6	5	pF
Output (DQ) Capacitance	8	7	pF

4.4. Timing Characteristics

The Timing characteristics of the Mitsubishi's Network SRAM (M5M5V5636GP) and the Samsung's NtRAM (K7N163601 A-Q) is shown in Table 11.

Table 11 Timing Characteristics

Parameter	Mitsubishi's Network SRAM	Samsung's NtRAM	Unit
Clock HIGH time (Min)	2.7	2.2	ns
Clock LOW time (Min)	2.7	2.2	ns
Output valid Time (Max)	3.8	3.5	ns

5. Electrical Characteristics (2.5V Power Supply)

The main differences about the electrical characteristics of the Mitsubishi's Network SRAM (M5M5T5636GP) and the Samsung's NtRAM (K7N163645 A-Q) are described. The product of operation voltage 2.5V, the frequency of 200MHz of operation, and the package 100 pin TQFP is compared as product specification (Since there is no product with an of operation frequency of 200MHz, ZBT SRAM is not compared).

5.1. Absolute Maximum Ratings

The absolute maximum rating of the Mitsubishi's Network SRAM (M5M5T5636GP) and the Samsung's NtRAM (K7N163645 A-Q) is shown in Table 12 Absolute Maximum Ratings.

Table 12 Absolute Maximum Ratings

Parameter	Mitsubishi's Network SRAM	Samsung's NtRAM	Unit
Power Supply Voltage	$-1.0^{Note\ 13} \sim 3.6$	$-0.3 \sim 3.6$	V
Input Voltage	$-1.0 \sim VDDQ+1.0^{Note\ 14}$	$-0.3 \sim VDDQ+0.3$	V

Note 13.   This is -1.0V when pulse width $\leq$ 2.0ns, and -0.5V in case of DC.
Note 14.   This is -1.0V - VDDQ+1.0V when pulse width $\leq$ 2.0ns, and -0.5V - VDDQ+0.5V in case of DC.
VDDQ=2.375~2.625V/1.7~1.95V

5.2. DC Electrical Characteristics

The DC electrical characteristics of the Mitsubishi's Network SRAM (M5M5T5636GP) and the Samsung's NtRAM (K7N163645 A-Q) is shown in Table 13 DC Electrical Characteristics.

Table 13 DC Electrical Characteristics

Parameter	Mitsubishi's Network SRAM	Samsung's NtRAM	Unit
High-level Output Voltage (Min)	$VDDQ-0.4^{Note\ 15}$	2.0	V
Input Current (Max)	10	2	µA
Power Supply Current: Operating	440	400	mA
CMOS Standby Current	20	60	mA
Snooze Mode Standby Current	20	10	mA

Note 15.   VDDQ=2.375~2.625V/1.7~1.95V

5.3. Capacitance

The Capacitance of the Mitsubishi's Network SRAM (M5M5T5636GP) and the Samsung's NtRAM (K7N163645 A-Q) is shown in Table 14 Capacitance.

Table 14 Capacitance

Parameter	Mitsubishi's Network SRAM	Samsung's NtRAM	Unit
Input Capacitance (Max)	6	5	pF
Output (DQ) Capacitance	8	7	pF

5.4. Timing Characteristics

The Timing characteristics of the Mitsubishi's Network SRAM (M5M5T5636GP) and the Samsung's NtRAM (K7N163645 A-Q) is shown in Table 15 Timing Characteristics.

Table 15 Timing Characteristics

Parameter	Mitsubishi's Network SRAM	Samsung's NtRAM	Unit
Clock HIGH time (Min)	1.8	2.0	ns
Clock LOW time (Min)	1.8	2.0	ns
Setup Time (Min)	1.2	1.4	ns
Hold Time (Min)	0.5	0.4	ns

6. Comparison Table

About a detailed function and a detailed electrical characteristics, there may be a difference in addition to the matter indicated by these technical document. In addition, about a detailed function and a detailed electrical characteristic, there may be a difference in addition to the contents described by these technical documents.

Table 16 Comparison Table

Capacity (Organization)	Package	Vcc (V)	Frequency (MHz)	Mitsubishi's Network SRAM	IDT's ZBT SRAM	Micron's ZBT SRAM	Samsung's NtRAM	Toshiba's NtRAM	Cypress's NoBL SRAM
18M (x36)	100 pin TQFP	3.3	250		There is no product for comparison.		K7N163609A		
			225				K7N163609A		
			200				K7N163609A		CY7C1370B
			166	M5M5V5636GP			K7N163601A	TC55VD1636FF	CY7C1370B
			150					TC55VD1636FF	CY7C1370B
			133			MT55L512Y36PT	K7N163601A	TC55VD1636FF	
			100			MT55L512Y36PT			
		2.5	250				K7N163649A		
			225				K7N163649A		
			200	M5M5T5636GP			K7N163645A		CY7C1370B
			180						CY7C1370B
			166		IDT71T75602S	MT55V512Y36P	K7N163649A	TC55WD1636FF	CY7C1370B
			150		IDT71T75602S			TC55WD1636FF	CY7C1370B
			133		IDT71T75602S	MT55V512Y36P	K7N163649A	TC55WD1636FF	CY7C1370B
			100		IDT71T75602S	MT55V512Y36P			
	165 ball FBGA	2.5	250	M5M5T5636UG	There is no product for comparison.		K7N163649A	There is no product for comparison.	There is no product for comparison.
			225	M5M5T5636UG			K7N163649A		
			200	M5M5T5636UG			K7N163649A		
			166			MT55V512Y36F	K7N163649A		
			150						
			133			MT55V512Y36F	K7N163645A		
			100			MT55V512Y36F			

7. Glossary

Synchronous SRAM

SRAM which operates synchronizing with an external clock (Please refer to Figure 4). Since it works to synchronize with a clock, an internal circuit improves in the speed and various operation can be performed, and there are some methods, such as Pipeline Burst, a Flow-Through, and Late Write ("ZBT" is a kind in Late Write operation mode.). The general low power SRAM and high-speed SRAM are asynchronous SRAM.

Pipeline Burst SRAM

Synchronous fast SRAM which had a burst address generating circuit (burst counter) in the internal circuit, pipelined access of a memory, and attained improvement in the speed (Please refer to Figure 4). The address of the following cycle can be inputted reading the data of the cycle in front of 1 cycle (address) by pipeline circuit. Therefore, improvement in the speed of data transmission is possible, without accelerating the access time of a memory.

Flow-Through

The operation mode of the synchronous fast SRAM which inputs an address and a control signal synchronizing with an external clock (CLK) input, and the data of the address is asynchronous and is outputted (Please refer to Figure 4). This mode of operation also calls it Non-Pipeline.

Late Write

The operation mode of synchronous fast SRAM is that it latches the address and control signals at first cycle and at the next cycle latches write data. This mode of operation can reduce the dead cycle of 2 cycles generated when write operation and read operation are continuously performed by the usual pipeline burst SRAM in 1 cycle.

Double Late Write

The operation mode of synchronous fast SRAM which an address and a control signal input synchronizing with an external clock (CLK) input, and inputs the write data after 2 cycle of operation. This mode can remove the dead cycle generated when write-in operation continues after read-out operation. It is manufactured by various another names and there is "ZBT" "No Turnaround" etc. as a typical product name.

Burst

The function which outputs the data of the address which continued from the outside to the arbitrary head addresses inputted (Please refer to Figure 5). The synchronous fast SRAM that generally supported this function of burst is meant. In addition, the sequence of an address and burst length change with products. In Burst SRAM corresponding to the x86 processor after Pentium, four data is outputted continuously.
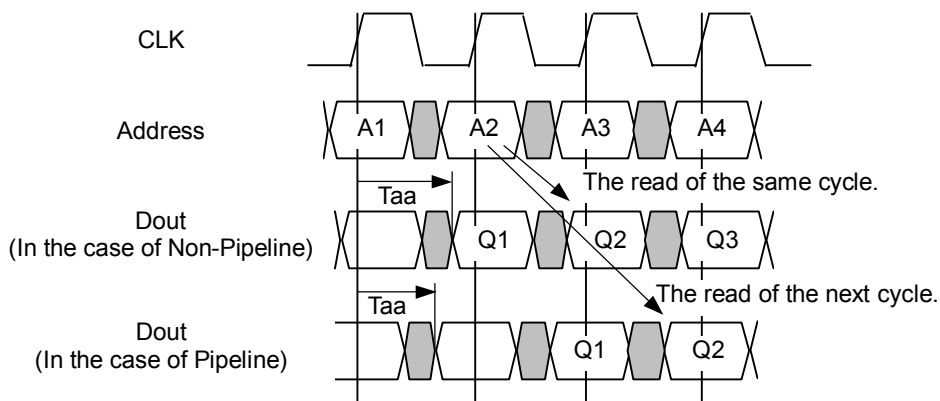
CLK

Address   A1   A2   A3   A4

Taa   The read of the same cycle.

Dout
(In the case of Non-Pipeline)   Q1   Q2   Q3

Taa   The read of the next cycle.

Dout
(In the case of Pipeline)   Q1   Q2

Figure 4 Operation Timing of the External Clock(CLK) Synchronous Fast SRAM

CLK

Address   A1   The address for 3 cycles
                 is unnecessary.   A5

Dout
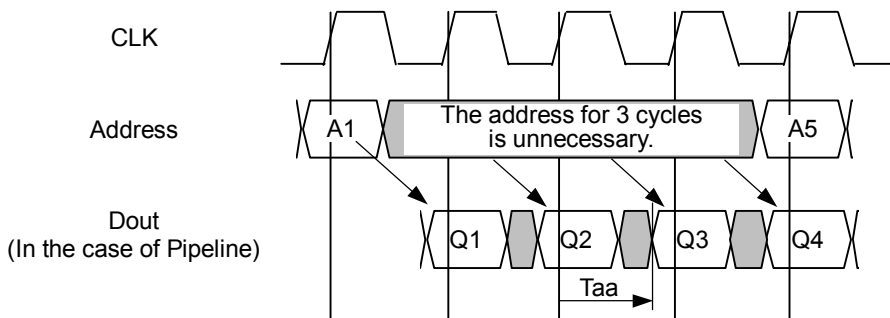(In the case of Pipeline)   Q1   Q2   Q3   Q4

Taa

Figure 5 Burst Operation Timing
* Continuous operation by the 2-bit address counter