To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Application Note

SRAM

The Advantage of 72-bit-wide Network SRAM over the 36-bit/18-bit-wide

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Contents

1. Introduction

In the field of networking applications that require higher data transmission rate, various kinds of SRAMs are used for the purpose of cache and/or buffer memory. From data bus utilization point of view, SRAMs that feature "no latency bus turnaround" are the mainstream technology of the latest synchronous SRAMs. To meet the requirement, we are supporting "Network SRAMs" that is the formal name adopted by JEDEC and is compatible with other no latency bus turnaround type of SRAMs such as ZBT (TM) and so forth.

If you want to improve the data transmission rate, the first thing you might select is to increase the clock frequency. And the alternative to that is to enlarge the data-bit (I/O) width of SRAMs. From this background, we are supporting 72-bit-wide in 18M-bit (i.e. 256K-word by 72-bit) Network SRAMs as much as 36-bit-wide (512K-word by 36-bit) type.

This technical document explains the advantage of 72-bit-wide Network SRAMs over less bit-width (such as 36- or 18-bit) types, in a system where the improvement of data transmission rate is an important design objective. As figures of merit, it verifies package area on PWB (printed wiring board), power consumption, clock frequency and timing relaxation, respectively.

In addition, there may be minor functional and electrical differences that are beyond the scope of this document, so customers should confirm technical details with the product datasheet or consult with our technical support personnel.

For further information about compatibility of Network SRAM with others, please refer to our application note: "Compatibility of Network SRAM with ZBT (TM) and Other No Latency Bus Turnaround SRAMs."

2. Package and Pin (Ball) Matrix of 72-bit-wide SRAM

Mitsubishi supports 72-bit-wide 18M-bit Network SRAMs (M5M5Y5672TG and M5M5T5672TG series) with a JEDEC standard 209 BGA package. Table 1 shows their pin (ball) configuration.

Table 1 Pin Configuration 209 BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A_6	E2	A_7	ADV	A_8	E3	A_9	DQb	DQb
B	DQg	DQg	BWc#	BWg#	NC	W#	A_{17}	BWb#	BWf#	DQb	DQb
C	DQg	DQg	BWh#	BWd#	NC	E1#	NC	BWe#	BWa#	DQb	DQb
D	DQg	DQg	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	DQb	DQb
E	DQPg	DQPc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPf	DQPb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
K	CQ2	CQ2#	CLK	NC	V_{SS}	MCL	V_{SS}	NC	NC	CQ1#	CQ1
L	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQPd	DQPh	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPa	DQPe
T	DQd	DQd	V_{SS}	NC	NC	LBO#	NC	NC	V_{SS}	DQe	DQe
U	DQd	DQd	NC	A_3	NC	A_{15}	NC	A_{11}	NC	DQe	DQe
V	DQd	DQd	A_5	A_4	A_{16}	A1	A_{13}	A_{12}	A_{10}	DQe	DQe
W	DQd	DQd	TMS	TDI	A_2	A0	A_{14}	TDO	TCK	DQe	DQe

Note 1. MCH means “Must Connect High”. MCH should be connected to HIGH.
Note 2. MCL means “Must Connect Low”. MCL should be connected to LOW.

3. Comparison of Package Area on PWB

Here is a simple case study where you construct a buffer memory of 2M-Byte with parity. The I/O width is 64-bit plus 8-bit. If it were not for 72-bit-wide SRAM, there is a need of two parts of 256K word by 36 (9M) bit SRAM. But this can be replaced with a single part by using Mitsubishi's 256K word by 72 (18M) bit SRAM. In the first place, this replacement leads to an area compaction on PWB (printed wiring board). The following is the estimation (Please also see Figure 1.) 100-pin TQFP and 119-ball BGA are common packages for 256K word by 36-bit SRAM. And 209-ball BGA is for 256K word by 72-bit. The total area of two 100TQFP's is 704mm^2 and 308mm^2 for one 209 BGA. The area can be reduced by 56.2% by using the 72-bit-wide. 119 BGA and 209 BGA are the same package outlines. In that case, the area can be reduced by 50%. This part number reduction also effects a relaxation of the pattern layout of PWB, although it is hard to express quantitatively.

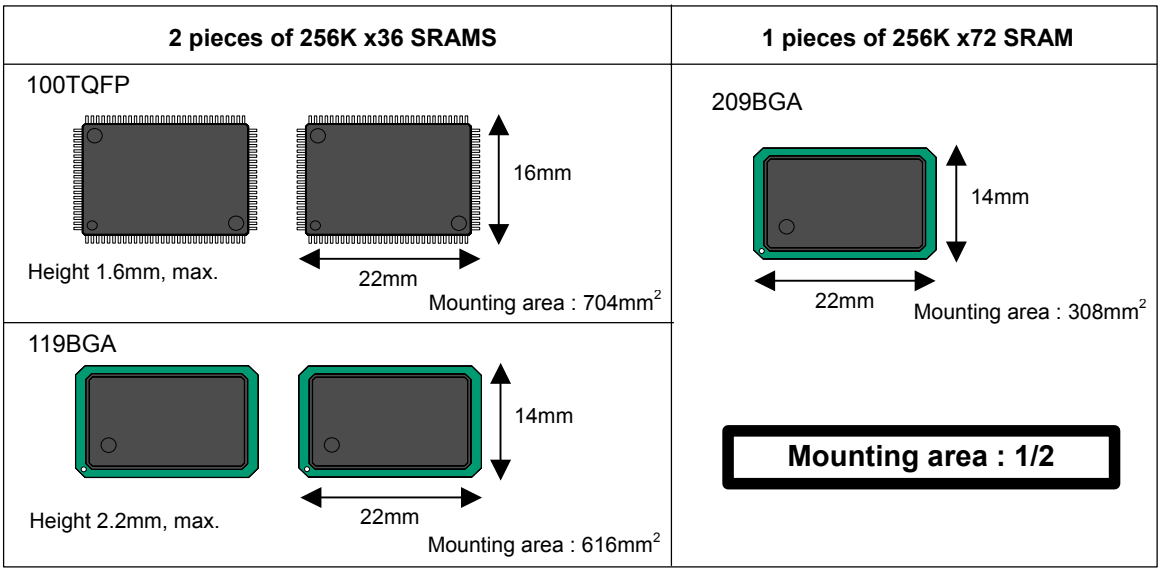

Figure 1 Comparison of Mounting Area

4. Electrical Comparison of 72-bit-wide with 36-bit-wide

4.1. Power Advantage

Similarly to the former section, let us figure out the effect of power reduction when constructing a memory system of 72-bit I/O. Total power consumption is a sum of operating current and current in deselected status. When 32-bit-wide SRAMs are used, there are always two active (operating) SRAMs. These results are summarized in Figure 2 and it shows a 72-bit-wide's advantage over 36-bit-wide.

(1) When using 256K word by 36-bit SRAM of vendor "S."

Operating power supply current: 440mA

Deselected power supply current: 250mA

Operating power supply of 2M-byte system = Operating power supply current of one chip x 2

= 440 x 2 = 880mA

Operating power supply of 4M-byte system

= Operating power supply current of one chip x 2 + Deselected power supply current of one chip x 2

= 440 x 2 + 250 x 2 = 1380mA

Operating power supply of 8M-byte system

= Operating power supply current of one chip x 2 + Deselected power supply current of one chip x 6

= 440 x 2 + 250 x 6 = 2380mA

(2) When using 256K word by 36-bit SRAM of vendor "N."

Operating power supply current: 440mA

Deselected power supply current: 130mA

Operating power supply of 2M-byte system = Operating power supply current of one chip x 2

= 440 x 2 = 880mA

Operating power supply of 4M-byte system

= Operating power supply current of one chip x 2 + Deselected power supply current of one chip x 2

= 440 x 2 + 130 x 2 = 1140mA

Operating power supply of 8M-byte system

= Operating power supply current of one chip x 2 + Deselected power supply current of one chip x 6

= 440 x 2 + 130 x 6 = 1660mA

(3) When using 256K word by 72-bit SRAM of Mitsubishi

Operating power supply current: 440mA

Deselected power supply current: 200mA

Operating power supply of 2M-byte system = Operating power supply current of one chip

= 550mA

Operating power supply of 4M-byte system

= Operating power supply current of one chip + Deselected power supply current of one chip

= 550 + 200 = 750mA

Operating power supply of 8M-byte system

= Operating power supply current of one chip + Deselected power supply current of two chips x 3

= 550 + 200 x 3 = 1150mA

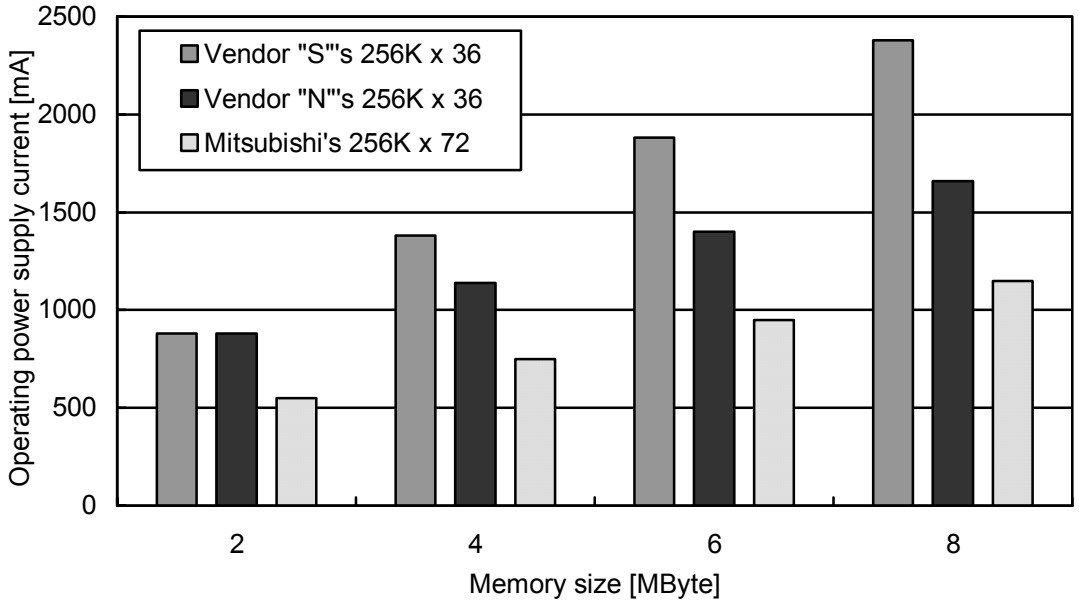

Figure 2 Operating Power Supply Current

4.2. Frequency Advantage

Data transmission rate is calculated by a multiplication of the clock frequency and the bit-width of I/O. Therefore, 72-bit-wide SRAM has substantially the advantage of higher data transmission over the less (36/18) bit-width type. From another viewpoint, the 72-bit-wide needs only a half of frequency that was necessary for 36-bit-wide type, under the condition of a same data transmission rate. Lower clock frequency not only gives a wider timing margin but also reduces an EMI (electro-magnetic interference) toward the system. See Figure 3 for its illustrative example and Table 2 for figures of merits.

Table 2 Comparison of Data Transmission Rate

Data rate	x36 (VDD: 2.5V)			x72 (VDD: 1.8V)	
	Clock	Vendor "Sa"	Vendor "So"	Clock	Mitsubishi
9Gb/s	250MHz	O	O	125MHz	x
12Gb/s	333MHz	O	O	167MHz	O
14.4Gb/s	400MHz	x	O	200MHz	O
18Gb/s	500MHz	x	x	250MHz	O
24Gb/s	666MHz	x	x	333MHz	ES (Mar, '03)

Note 3. O: product available x: no product available

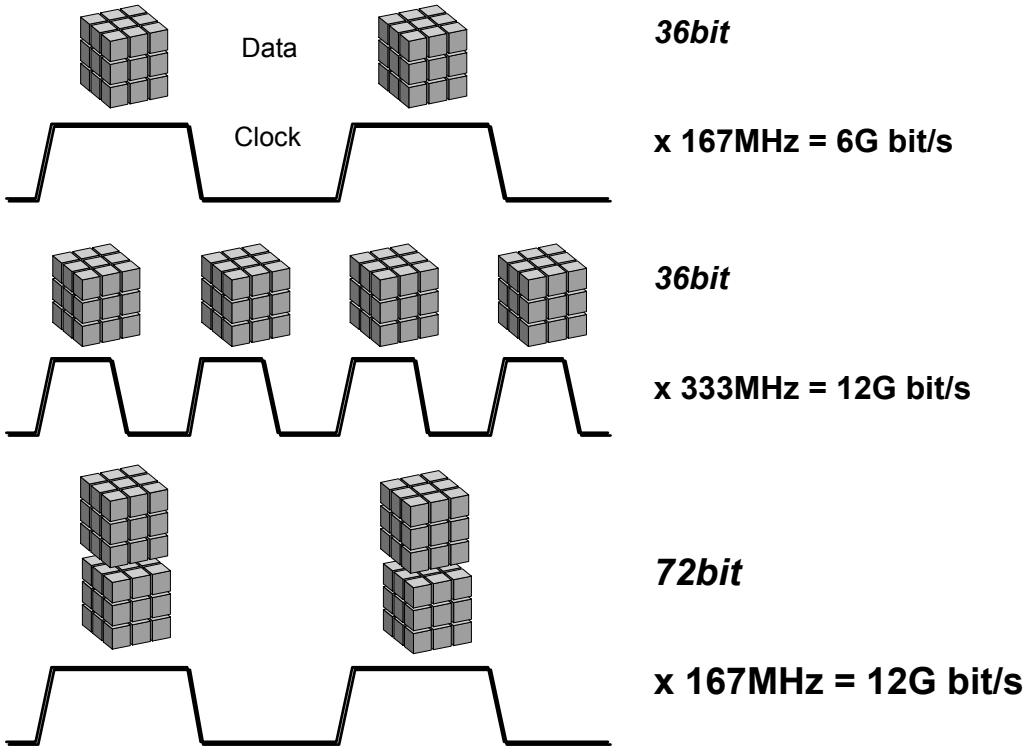

Figure 3 A Conceptual Explanation of Data Transmission Rate

4.3. Timing Advantage

This section explains how the margin of timing design is relaxed when 72-bit-wide SRAM is used, compared with 32-bit-wide one. As shown in Section 4.2, let us compare both of them on a condition of data transmission rate of 12G-bit/sec (See Figure 4). The required clock frequencies are 167MHz and 333MHz, respectively. The data setup time and hold times of 167MHz specs are 1.5ns and 0.5ns, respectively. But those of 333MHz specs are 0.7ns and 0.4ns. Thus designing with 72-bit-wide secures a wider timing window on the edge of clocks.

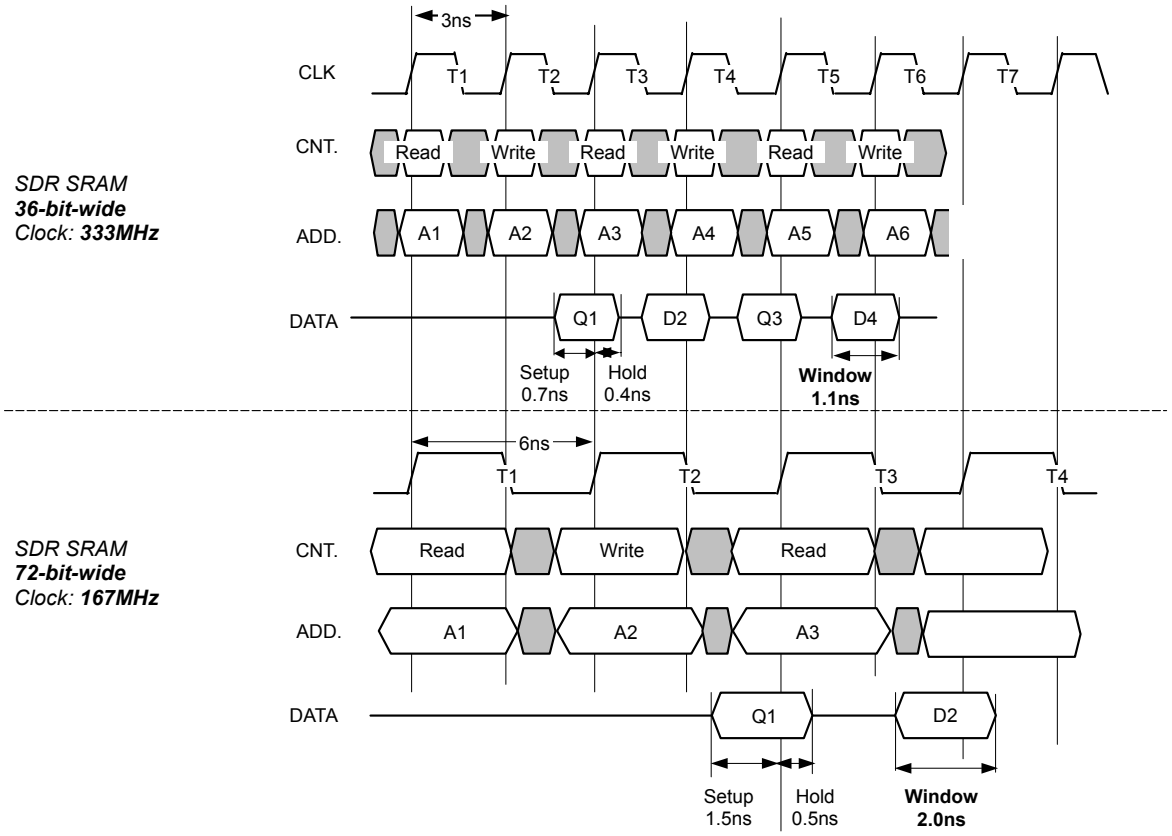

Figure 4 Timing Character of x36 and x72

5. Comparison of SDR with DDR

5.1. Power Advantage

This section compares 72-bit-wide SRAM that is implicitly presumed as Single Data Rate (SDR) type, and with Double Data Rate (DDR) type of SRAM. Since the maximum I/O bit-width offered in DDR to date is 36-bit, let us compare 72-bit-wide SDR and 36-bit-wide DDR on a condition of same data rate. Although both of type is driven by same external clock frequency, there are some differences in power consumption as shown in Table 3. The clock frequency for 18G-bit/sec is 250MHz in both SDR and DDR. But the operating current of SDR is 550mA and that of DDR is 590mA. As this example, DDR tends to specify higher power supply current assuring their internal high rate of data handling.

Table 3 Comparison of Power Supply Current

Data rate	Clock frequency		DDR (36-bit I/O)		SDR
			Vendor “N”	Vendor “S”	Mitsubishi
18Gb/s	250MHz	Operating	590mA	600mA	550mA
		Deselected	250mA	550mA	200mA
24Gb/s	333MHz	Operating	-	750mA	650mA
		Deselected	-	700mA	240mA

5.2. Timing Advantage

According to Section 5.1, let us compare on a same data rate of 18G-bit/sec. The timing constraint is basically same with regard to address and control signals. But with data inputs/outputs, DDR requires a tighter timing design from its substance. Figure 5 shows that the SDR's data window has a wider margin than DDR.

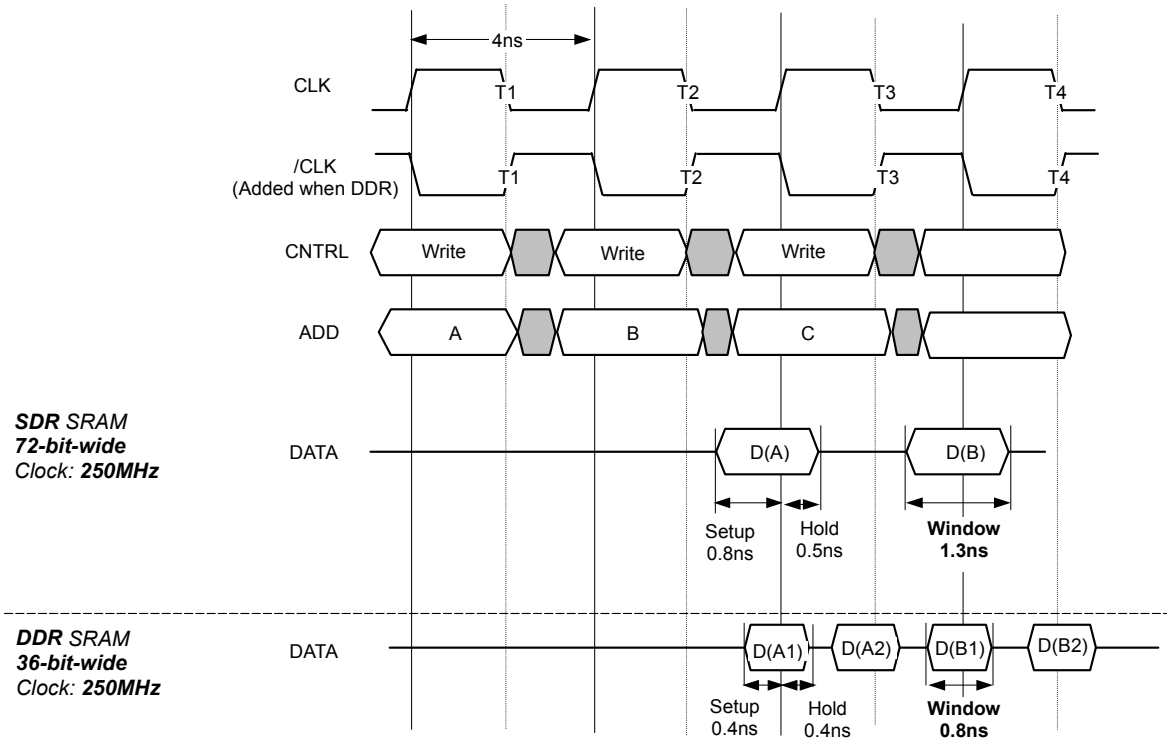

Figure 5 Timing Comparison of SDR and DDR

6. Glossary

Synchronous SRAM

This type of SRAM uses an external clock to synchronize other signals with it in order to improve the frequency of memory access. A basic synchronous SRAM internally contains a group of registers for address, control and data input signals. For more advanced, it further contains additional registers for data output and/or burst counters. By this internal combination of registers and counters, there are various types of Synchronous SRAMs such as Pipeline Burst, Flow-Through, and Late Write and so forth.

Pipeline Burst SRAM

A synchronous SRAM that has an internal registers for data output signals and also has burst counters. In the "Pipeline" read, address and control signals are latched on the first cycle and consequent data-outputs are synchronized two clocks later. This is referred to as "Read Latency of 2." Figure 6 shows a comparison between pipeline and non-pipeline SRAMs. When combined with "Burst" mode, it provides a faster data transmission.

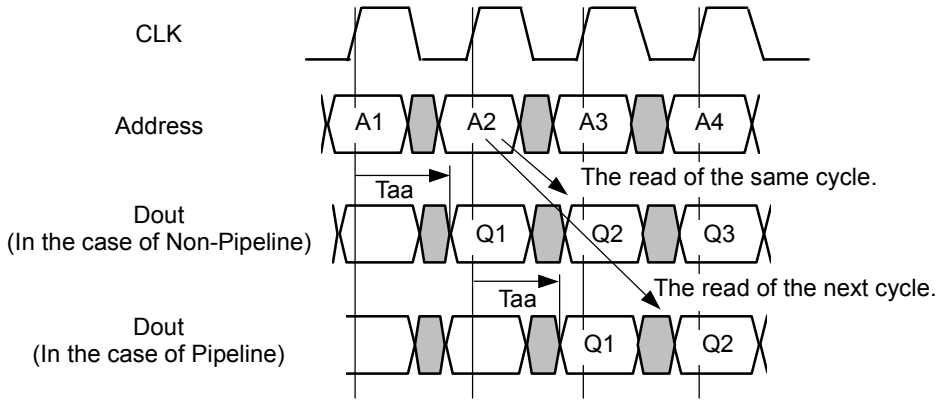

Figure 6 Operation Timing of the External Clock (CLK) in Synchronous SRAM

Burst

The burst function enables the system to receive several data with one address input and successive clock feeding. In this mode, burst counters generate internal addresses according to their predetermined bit-length. Common products use burst lengths of 2 or 4 or 8, etc. See Figure 7, which illustrates burst timing.

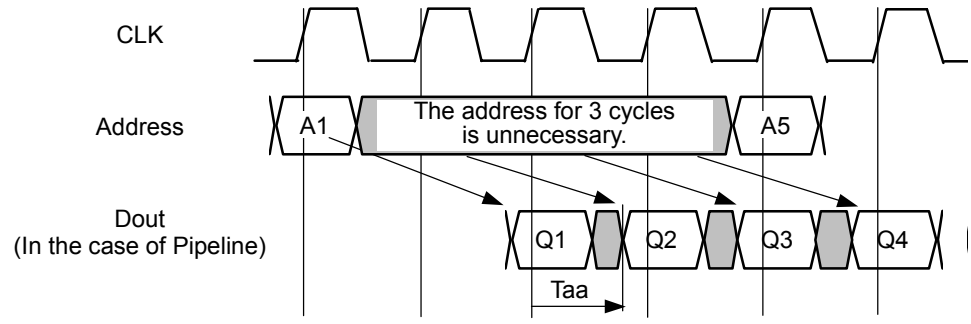

Figure 7 Burst Operation Timing (Continuous Operation by the 2-bit Address Counter)

Flow-Through
An operation mode of synchronous SRAMs. Address, control and data-input signals are synchronized with the clock, but the data output is asynchronous because it use no register for data-output. This operation mode is also known as "Non-Pipeline." The read latency is 1, less than pipeline, but clock frequency does not go as high as pipeline.

Late Write
A write operation mode of synchronous SRAMs that latches the address and control signals on the first cycle and latches write data on the next cycle. In other word, "the write latency is 1." This mode can reduce the dead cycle time when the write and read operations are continuously performed in alternating cycles. This mode is also called "Single Late Write" as opposed to "Double Late Write." (See below.)

Double Late Write
Another write operation mode of synchronous SRAMs. Address and control signal inputs are synchronized with a preceding cycle and the data write is performed after two cycles. In other word, "the write latency is 2." When combined with the pipeline read, this mode completely removes the dead cycle generated when a write operation continues after a read operation. That is referred to as "no latency bus turnaround." Almost all fast SRAM vendors support this type of memory, but confusingly, they use different product names.

Single Data Rate (SDR)
The word "SDR" defines how signals are latched on the edge of clocks. The address, control and data input signals are latched on the rising edge of clock, and data output signals are also conveyed on the rising edge of clock cycles. This concept is so common that we usually mention this term only as opposed to Double Data Rate "DDR". Pipeline Burst, Flow-Through, Late Write and Network SRAM are all categorized into SDR.

Double Data Rate (DDR)
Another definition of how signals are synchronized on the edges of clocks. The address and control signals are latched on the rising edge of clocks just as SDR, but data input and output signals are sent on both the rising and falling edges of clock cycles. Therefore, under the same conditions of external clock frequency, the data transmission rate is two times faster than SDR. But on the other hand, it requires rather complicated logics for the memory controller in order to convey double data on a single clock cycle.

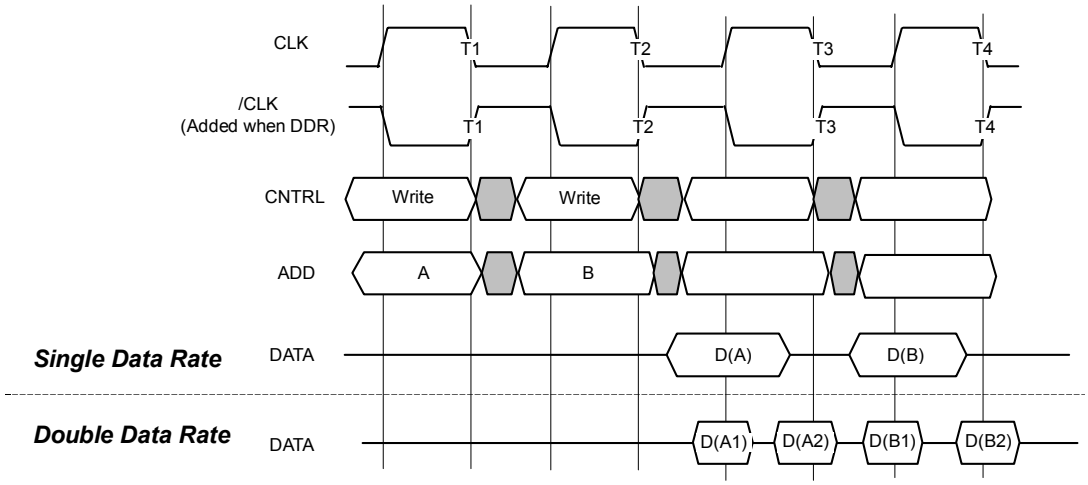

Figure 8 Comparison of SDR and DDR (in case of Data Write)