# Preliminary

Notice: This is not a final specification. Some parametric limits are subject to change.

### **Renesas LSIs**

# M5M29KB/T641AVP

67,108,864-BIT (8,388,608-WORD BY 8-BIT /4,194,304-WORD BY 16-BIT) **CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY** 

### DESCRIPTION

The M5M29KB/T641AVP are 3.3V-only high speed 67,108,864-bit CMOS boot block FLASH Memories with alternating BGO(Back Ground Operation) feature. The BGO feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank.

This BGO feature is suitable for mobile and personal computing, and communication products.

The M5M29KB/T641AVP are fabricated by CMOS technology for the peripheral circuit and DINOR IV(Divided bit-line NOR IV) architecture for the memory cell, and are available in 48pin TSOP(I) for lead free use.

M5M29KB/T641AVP provides for Software Lock Release function. Usually, all memory blocks are locked and can not be programmed or erased, when WP# is low. Using Software Lock Release function, program or erase operation can be executed.

## **FEATURES**

Package

Access time	Flash
Supply voltage	

70ns (Max.) VCC= 3.0 ~ 3.6V

Ambient temperature

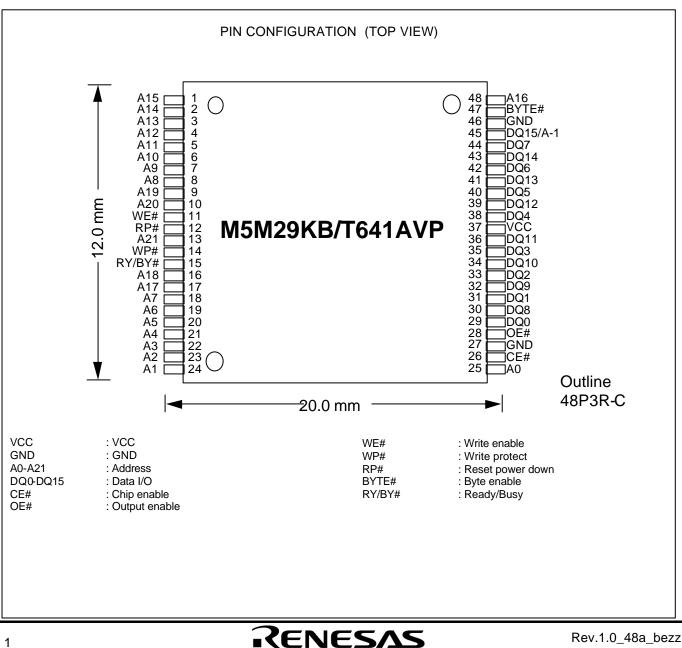
Ta=-40 ~ 85 °C

48pin TSOP(Type-I), Lead pitch 0.5mm

Outer-lead finishing : Sn-Cu

### APPLICATION

Digital Cellar Phone, Telecommunication, PDA, Car Navigation System, Video Game Machine



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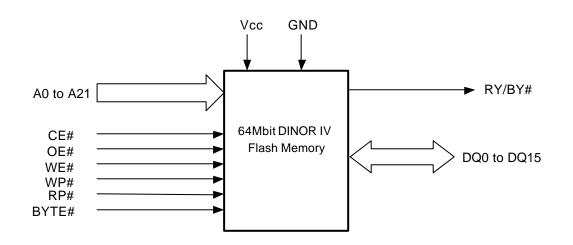
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### 64M Flash Memory Block Diagram



### Capacitance

Symbol	Parameter	Conditions	Limits			Unit	
	i urumeter		Min.	Тур.	Max.	Onit	
CIN		A21-A0, OE#, WE#, CE#, WP#,	Ta=25°C, f=1MHz, Vin=Vout=0V			12	pF
	capacitance	RP#,BYTE#					
соит	Output	DQ15-DQ0,RY/BY#				12	рF
	Capacitance					12	۲ <u>۱</u>





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